

PHILIPS

Data handbook



Electronic
components
and materials

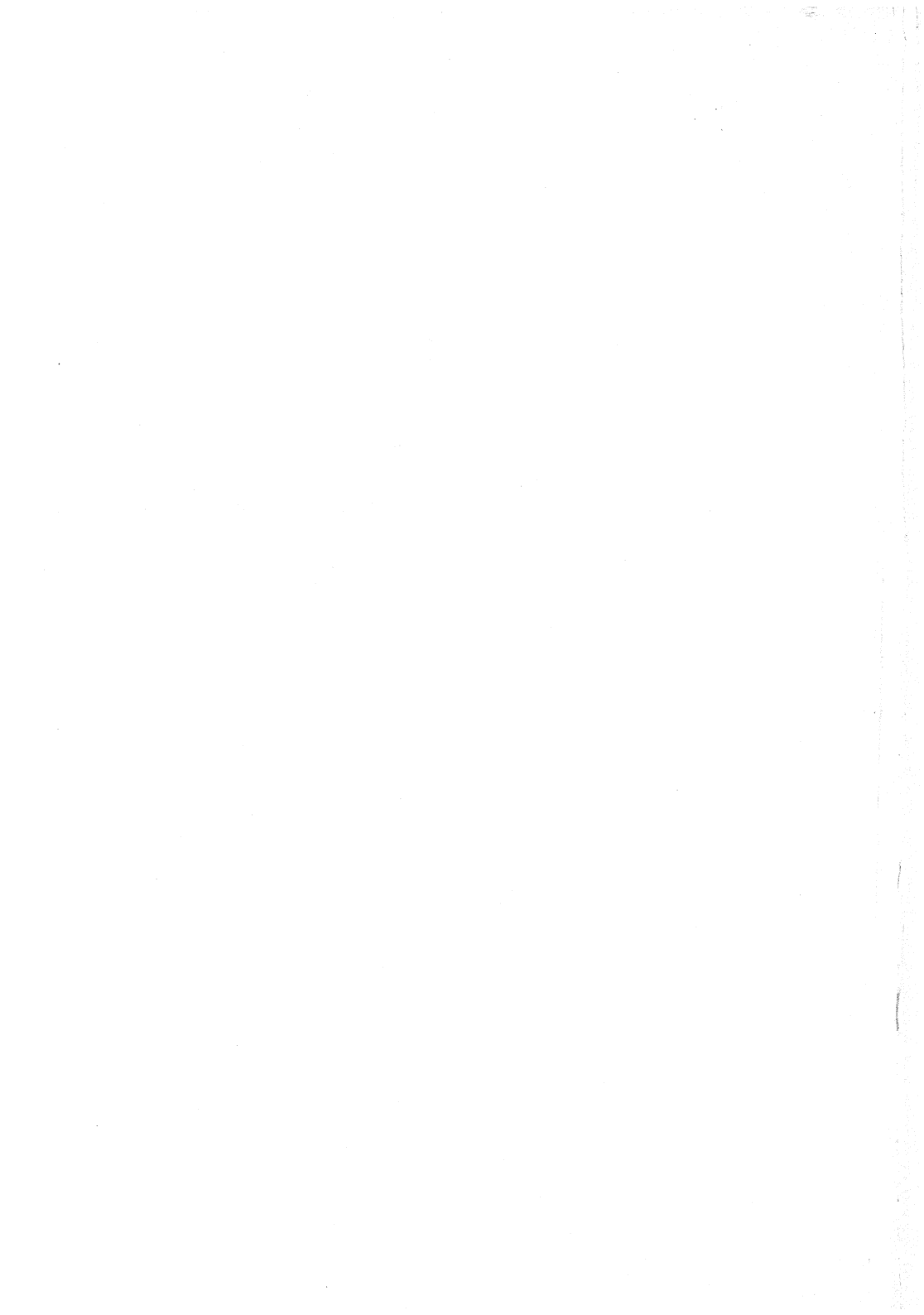
Integrated circuits

Part 4

October 1980

Digital integrated circuits

LOCMOS HE4000B family



INTEGRATED CIRCUITS

PART 4 - OCTOBER 1980

DIGITAL INTEGRATED CIRCUITS — LOC MOS

FUNCTIONAL AND NUMERICAL INDEX

GENERAL

PACKAGE OUTLINES

FUNCTIONAL DIAGRAMS

PIN DESIGNATIONS

HE4000B FAMILY - INTRODUCTION

FAMILY SPECIFICATIONS

DEVICE DATA



DATA HANDBOOK SYSTEM

Our Data Handbook System is a comprehensive source of information on electronic components, sub-assemblies and materials; it is made up of four series of handbooks each comprising several parts.

ELECTRON TUBES	BLUE
SEMICONDUCTORS	RED
INTEGRATED CIRCUITS	PURPLE
COMPONENTS AND MATERIALS	GREEN

The several parts contain all pertinent data available at the time of publication, and each is revised and reissued periodically.

Where ratings or specifications differ from those published in the preceding edition they are pointed out by arrows. Where application information is given it is advisory and does not form part of the product specification.

If you need confirmation that the published data about any of our products are the latest available, please contact our representative. He is at your service and will be glad to answer your inquiries.

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ELECTRON TUBES (BLUE SERIES)

Starting in 1980, new part numbers and corresponding codes are being introduced. The former code of the preceding issue is given in brackets under the new code.

Part 1	February 1980	T1 02-80 (ET1a 12-75)	Tubes for r. f. heating
Part 2	April 1980	T2 04-80 (ET1b 08-77)	Transmitting tubes for communications
Part 2b	May 1978	ET2b 05-78	Microwave semiconductors and components Gunn, Impatt and noise diodes, mixer and detector diodes, backward diodes, varactor diodes, Gunn oscillators, sub-assemblies, circulators and isolators.
Part 3	June 1980	T3 06-80 (ET2a 11-77)	Klystrons, travelling-wave tubes, microwave diodes
Part 3	January 1975	ET3 01-75	Special Quality tubes, miscellaneous devices
Part 4	September 1980	T4 09-80 (ET2a 11-77)	Magnetrons
Part 5a	October 1979	ET5a 10-79	Cathode-ray tubes Instrument tubes, monitor and display tubes, C.R. tubes for special applications.
Part 5b	December 1978	ET5b 12-78	Camera tubes and accessories, image intensifiers
Part 6	July 1980	T6 07-80 (ET6 01-77)	Geiger-Müller tubes
Part 7a	March 1977	ET7a 03-77	Gas-filled tubes Thyratrons, industrial rectifying tubes, ignitrons, high-voltage rectifying tubes.
Part 7b	May 1979	ET7b 05-79	Gas-filled tubes Segment indicator tubes, indicator tubes, switching diodes, dry reed contact units.
Part 8	July 1979	ET8 07-79	Picture tubes and components Colour TV picture tubes, black and white TV picture tubes, monitor tubes, components for colour television, components for black and white television.
Part 9	June 1980	T9 06-80 (ET9 03-78)	Photo and electron multipliers Photomultiplier tubes, phototubes, single channel electron multipliers, channel electron multiplier plates.

SEMICONDUCTORS (RED SERIES)

Starting in 1980, new part numbers and corresponding codes are being introduced. The former code of the preceding issue is given in brackets under the new code.

Part 1	March 1980	S1 03-80 (SC1b 05-77)	Diodes Small-signal germanium diodes, small-signal silicon diodes, special diodes, voltage regulator diodes ($< 1,5$ W), voltage reference diodes, tuner diodes, rectifier diodes
Part 2	May 1980	S2 05-80 (SC1a 08-78)	Power diodes, thyristors, triacs Rectifier diodes, voltage regulator diodes ($> 1,5$ W), rectifier stacks, thyristors, triacs
Part 2	June 1979	SC2 06-79	Low-frequency power transistors
Part 3	January 1978	SC3 01-78	High-frequency, switching and field-effect transistors*
Part 3	April 1980	S3 04-80 (SC2 11-77, partly) (SC3 01-78, partly)	Small-signal transistors
Part 4a	December 1978	SC4a 12-78	Transmitting transistors and modules
Part 4b	September 1978	SC4b 09-78	Devices for optoelectronics Photosensitive diodes and transistors, light-emitting diodes, photocouplers, infrared sensitive devices, photoconductive devices
Part 4c	July 1978	SC4c 07-78	Discrete semiconductors for hybrid thick and thin-film circuits
Part 5	October 1980	S5 10-80 (SC3 01-78)	Field-effect transistors

* Wideband transistors will be transferred to SC3c. The old book SC3 01-78 should be kept until then.

INTEGRATED CIRCUITS (PURPLE SERIES)

Starting in 1980, new part numbers and corresponding codes are being introduced. The former code of the preceding issue is given in brackets under the new code. Books with the purple cover will replace existing red covered editions as each is revised.

Part 1	May 1980	IC1 04-80 (SC5b 03-77)	Bipolar ICs for radio and audio equipment
Part 2	May 1980	IC2 04-80 (SC5b 03-77)	Bipolar ICs for video equipment
Part 5a	November 1976	SC5a 11-76	Professional analogue integrated circuits
Part 4	October 1980	IC4 10-80 (SC6 10-77)	Digital integrated circuits LOC MOS HE4000B family
Part 6b	August 1979	SC6b 08-79	ICs for digital systems in radio and television receivers
Signetics integrated circuits			Bipolar and MOS memories 1979 Bipolar and MOS microprocessors 1978 Analogue circuits 1979 Logic - TTL 1978

COMPONENTS AND MATERIALS (GREEN SERIES)

Starting in 1980, new part numbers and corresponding codes are being introduced. The former code of the preceding issue is given in brackets under the new code.

Part 1	July 1979	CM1 07-79	Assemblies for industrial use PLC modules, high noise immunity logic FZ/30 series, NORbits 60-series, 61-series, 90-series, input devices, hybrid integrated circuits, peripheral devices
Part 3a	September 1978	CM3a 09-78	FM tuners, television tuners, surface acoustic wave filters
Part 3b	October 1978	CM3b 10-78	Loudspeakers
Part 4a	November 1978	CM4a 11-78	Soft Ferrites Ferrites for radio, audio and television, beads and chokes, Ferroxcube potcores and square cores, Ferroxcube transformer cores
Part 4b	February 1979	CM4b 02-79	Piezoelectric ceramics, permanent magnet materials
Part 6	April 1977	CM6 04-77	Electric motors and accessories Small synchronous motors, stepper motors, miniature direct current motors
Part 7	September 1971	CM7 09-71	Circuit blocks Circuit blocks 100 kHz-series, circuit blocks 1-series, circuit blocks 10-series, circuit blocks for ferrite core memory drive
Part 7a	January 1979	CM7a 01-79	Assemblies Circuit blocks 40-series and CSA70 (L), counter modules 50-series, input/output devices
Part 8	June 1979	CM8 06-79	Variable mains transformers
Part 9	August 1979	CM9 08-79	Piezoelectric quartz devices Quartz crystal units, temperature compensated crystal oscillators
Part 10	October 1980	C10 10-80	Connectors
Part 11	December 1979	CM11 12-79	Non-linear resistors Voltage dependent resistors (VDR), light dependent resistors (LDR), negative temperature coefficient thermistors (NTC), positive temperature coefficient thermistors (PTC)
Part 12	November 1979	CM12 11-79	Variable resistors and test switches
Part 13	December 1979	CM13 12-79	Fixed resistors
Part 14	April 1980	C14 04-80 (CM2b 02-78)	Electrolytic and solid capacitors
Part 15	May 1980	C15 05-80 (CM2b 02-78)	Film capacitors, ceramic capacitors, variable capacitors

FUNCTIONAL AND NUMERICAL INDEX



			page
NAND gates	HEF4011B	quadruple 2-input NAND gate	139
	HEF4011UB	quadruple 2-input NAND gate; unbuffered	141
	HEF4012B	dual 4-input NAND gate	149
	HEF4023B	triple 3-input NAND gate	213
	HEF4068B	8-input NAND gate	363
AND gates	HEF4073B	triple 3-input AND gate	377
	HEF4081B	quadruple 2-input AND gate	391
	HEF4082B	dual 4-input AND gate	393
NOR gates	HEF4000B	dual 3-input NOR gate and inverter	107
	HEF4001B	quadruple 2-input NOR gate	111
	HEF4001UB	quadruple 2-input NOR gate; unbuffered	113
	HEF4002B	dual 4-input NOR gate	121
	HEF4025B	triple 3-input NOR gate	219
	HEF4078B	8-input NOR gate	389
OR gates	HEF4071B	quadruple 2-input OR gate	373
	HEF4072B	dual 4-input OR gate	375
	HEF4075B	triple 3-input OR gate	379
Inverters and buffers	HEF4007UB	dual complementary pair and inverter	127
	HEF4041B	quadruple true/complement buffer	263
	HEF4049B	hex inverting buffers	307
	HEF4050B	hex non-inverting buffers	309
	HEF4069UB	hex inverter	365
	HEF4502B	strobed hex inverter/buffer	419
	HEF40097B	3-state hex non-inverting buffer	707
	HEF40098B	3-state hex inverting buffer	711
Complex gates	HEF4030B	quadruple EXCLUSIVE-OR gate	243
	HEF4070B	quadruple EXCLUSIVE-OR gate	371
	HEF4077B	quadruple EXCLUSIVE-NOR gate	387
	HEF4085B	dual 2-wide 2-input AND-OR-invert gate	395
	HEF4086B	4-wide 2-input AND-OR-invert gate	397
Flip-flops	HEF4013B	dual D-type flip-flop	151
	HEF4027B	dual JK flip-flop	221
	HEF4076B	quadruple D-type register with 3-state outputs	381
	HEF40174B	hex D-type flip-flop	761
	HEF40175B	quadruple D-type flip-flop	765
Counters	HEF4017B	5-stage Johnson counter	175
	HEF4018B	presettable divide-by-n counter	183
	HEF4020B	14-stage binary counter	193
	HEF4022B	4-stage divide-by-8 Johnson counter	205
	HEF4024B	7-stage binary counter	215
	HEF4029B	synchronous up/down counter, binary/decade counter	231
	HEF4040B	12-stage binary counter	259

FUNCTIONAL INDEX

			page
Counters (continued)	HEF4059B	programmable divide-by-n counter	335
	HEF4060B	14-stage ripple-carry binary counter/divider and oscillator	341
	HEF4510B	BCD up/down counter	439
	HEF4516B	binary up/down counter	471
	HEF4518B	dual BCD counter	489
	HEF4520B	dual binary counter	499
	HEF4521B	24-stage frequency divider	505
	HEF4522B	programmable 4-bit BCD down counter	515
	HEF4526B	programmable 4-bit binary down counter	525
	HEF4534B	real time 5-decade counter	561
	HEF4737B; V	quadruple static decade counters	641
	HEF4751V	universal divider	679
	HEF40160B	4-bit synchronous decade counter with asynchronous reset	721
	HEF40161B	4-bit synchronous binary counter with asynchronous reset	731
	HEF40162B	4-bit synchronous decade counter with synchronous reset	741
	HEF40163B	4-bit synchronous binary counter with synchronous reset	751
	HEF40192B	4-bit up/down decade counter	769
	HEF40193B	4-bit up/down binary counter	777
	Registers	HEF4006B	18-stage static shift register
HEF4014B		8-bit static shift register	157
HEF4015B		dual 4-bit static shift register	163
HEF4021B		8-bit static shift register	199
HEF4031B		64-stage static shift register	245
HEF4035B		4-bit universal shift register	251
HEF4076B		quadruple D-type register with 3-state outputs	381
HEF4094B		8-stage shift-and-store bus register	407
HEF4517B		dual 64-bit static shift register	481
HEF4557B		1-to-64 bit variable length shift register	603
HEF4731B; V		quadruple 64-bit static shift register	637
HEF40194B		4-bit bidirectional universal shift register	785
HEF40195B	4-bit universal shift register	791	
Decoders and demultiplexers	HEF4028B	1-of-10 decoder	227
	HEF4511B	BCD to 7-segment latch/decoder/driver	449
	HEF4514B	1-of-16 decoder/demultiplexer with input latches	463
	HEF4515B	1-of-16 decoder/demultiplexer with input latches	467
	HEF4543B	BCD to 7-segment latch/decoder/driver	589
	HEF4555B	dual 1-of-4 decoder/demultiplexer	595
	HEF4556B	dual 1-of-4 decoder/demultiplexer	599
Digital multiplexers	HEF4019B	quadruple 2-input multiplexer	189
	HEF4512B	8-input multiplexer with 3-state output	457
	HEF4519B	quadruple 2-input multiplexer	495
	HEF4539B	dual 4-input multiplexer	577

			page	
Analogue switches and multiplexers/demultiplexers	HEF4016B	quadruple bilateral switches	167	
	HEF4051B	8-channel analogue multiplexer/demultiplexer	311	
	HEF4052B	dual 4-channel analogue multiplexer/demultiplexer	319	
	HEF4053B	triple 2-channel analogue multiplexer/demultiplexer	327	
	HEF4066B	quadruple bilateral switches	347	
	HEF4067B	16-channel analogue multiplexer/demultiplexer	355	
Latches	HEF4042B	quadruple D-latch	265	
	HEF4043B	quadruple R/S latch with 3-state outputs	271	
	HEF4044B	quadruple R/S latch with 3-state outputs	275	
	HEF4508B	dual 4-bit latch	431	
	HEF4724B	8-bit addressable latch	631	
	Multivibrators and timers	HEF4047B	monostable/astable multivibrator	293
HEF4528B		dual monostable multivibrator	543	
HEF4538B		dual precision monostable multivibrator	569	
HEF4541B		programmable timer	581	
HEF4753B		universal timer module	693	
Arithmetic units		HEF4008B	4-bit binary full adder	135
	HEF4531B	13-input parity checker/generator	549	
	HEF4532B	8-input priority encoder	553	
	HEF4585B	4-bit magnitude comparator	609	
	Schmitt triggers	HEF4093B	quadruple 2-input NAND Schmitt trigger	401
HEF40106B		hex Schmitt trigger	715	
Memories		HEF4505B	64-bit, 1-bit per word read/write RAM	423
	HEF4720B; V	256-bit, 1-bit per word RAM	615	
	Special functions	HEF4046B	phase-locked loop	279
HEF4104B		quadruple low-to-high voltage translator with 3-state outputs	415	
HEF4527B		BCD rate multiplier	535	
HEF4738V		IEC/IEEE bus interface	649	
HEF4739V		digital voltmeter circuit	657	
HEF4750V		frequency synthesizer	663	
HEF4752V		a.c. motor control circuit	689	
HEF4754V		18-element bar graph LCD driver	701	
Octal circuits		HEF40244B	octal buffers with 3-state outputs	799
		HEF40245B	octal bus transceiver with 3-state outputs	801
	HEF40373B	octal transparent latch with 3-state outputs	803	
	HEF40374B	octal D-type flip-flop with 3-state outputs	805	

NUMERICAL INDEX

type number	function	category	pins	suffix *	page
HEF4000B	dual 3-input NOR gate and inverter	gates	14	D, P, T	107
HEF4001B	quadruple 2-input NOR gate	gates	14	D, P, T	111
HEF4001UB	quadruple 2-input NOR gate; unbuffered	gates	14	D, P, T	113
HEF4002B	dual 4-input NOR gate	gates	14	D, P, T	121
HEF4006B	18-stage static shift register	MSI	14	D, P, T	123
HEF4007UB	dual complementary pair and inverter	gates	14	D, P, T	127
HEF4008B	4-bit binary full adder	MSI	16	D, P, T	135
HEF4011B	quadruple 2-input NAND gate	gates	14	D, P, T	139
HEF4011UB	quadruple 2-input NAND gate; unbuffered	gates	14	D, P, T	141
HEF4012B	dual 4-input NAND gate	gates	14	D, P, T	149
HEF4013B	dual D-type flip-flop	flip-flops	14	D, P, T	151
HEF4014B	8-bit static shift register	MSI	16	D, P, T	157
HEF4015B	dual 4-bit static shift register	MSI	16	D, P, T	163
HEF4016B	quadruple bilateral switches	gates	14	D, P, T	167
HEF4017B	5-stage Johnson counter	MSI	16	D, P, T	175
HEF4018B	presetable divide-by-n counter	MSI	16	D, P, T	183
HEF4019B	quadruple 2-input multiplexer	MSI	16	D, P, T	189
HEF4020B	14-stage binary counter	MSI	16	D, P, T	193
HEF4021B	8-bit static shift register	MSI	16	D, P, T	199
HEF4022B	4-stage divide-by-8 Johnson counter	MSI	16	D, P, T	205
HEF4023B	triple 3-input NAND gate	gates	14	D, P, T	213
HEF4024B	7-stage binary counter	MSI	14	D, P, T	215
HEF4025B	triple 3-input NOR gate	gates	14	D, P, T	219
HEF4027B	dual JK flip-flop	flip-flops	16	D, P, T	221
HEF4028B	1-of-10 decoder	MSI	16	D, P, T	227
HEF4029B	synchronous up/down — binary/decade counter	MSI	16	D, P, T	231
HEF4030B	quadruple EXCLUSIVE-OR gate	gates	14	D, P, T	243
HEF4031B	64-stage static shift register	LSI	16	D, P, T	245
HEF4035B	4-bit universal shift register	MSI	16	D, P, T	251
HEF4040B	12-stage binary counter	MSI	16	D, P, T	259
HEF4041B	quadruple true/complement buffer	buffers	14	D, P, T	263
HEF4042B	quadruple D-latch	MSI	16	D, P, T	265
HEF4043B	quadruple R/S latch with 3-state outputs	MSI	16	D, P, T	271
HEF4044B	quadruple R/S latch with 3-state outputs	MSI	16	D, P, T	275
HEF4046B	phase-locked loop	MSI	16	D, P, T	279
HEF4047B	monostable/astable multivibrator	MSI	14	D, P, T	293
HEF4049B	hex inverting buffers	buffers	16	D, P, T	307
HEF4050B	hex non-inverting buffers	buffers	16	D, P, T	309
HEF4051B	8-channel analogue multiplexer/demultiplexer	MSI	16	D, P, T	311
HEF4052B	dual 4-channel analogue multiplexer/demultiplexer	MSI	16	D, P, T	319

* Add the suffix to the type number on all orders.

D:ceramic package (DIL).

P:plastic package (DIL).

T:plastic flat pack (SO-package).

NUMERICAL INDEX

type number	function	category	pins	suffix *	page
HEF4053B	triple 2-channel analogue multiplexer/demultiplexer	MSI	16	D, P, T	327
HEF4059B	programmable divide-by-n counter	MSI	24	D, P	335
HEF4060B	14-stage ripple-carry binary counter/divider and oscillator	MSI	16	D, P, T	341
HEF4066B	quadruple bilateral switches	gates	14	D, P, T	347
HEF4067B	16-channel analogue multiplexer/demultiplexer	MSI	24	D, P	355
HEF4068B	8-input NAND gate	gates	14	D, P, T	363
HEF4069UB	hex inverter	gates	14	D, P, T	365
HEF4070B	quadruple EXCLUSIVE-OR gate	gates	14	D, P, T	371
HEF4071B	quadruple 2-input OR gate	gates	14	D, P, T	373
HEF4072B	dual 4-input OR gate	gates	14	D, P, T	375
HEF4073B	triple 3-input AND gate	gates	14	D, P, T	377
HEF4075B	triple 3-input OR gate	gates	14	D, P, T	379
HEF4076B	quadruple D-type register with 3-state outputs	MSI	16	D, P, T	381
HEF4077B	quadruple EXCLUSIVE-NOR gate	gates	14	D, P, T	387
HEF4078B	8-input NOR gate	gates	14	D, P, T	389
HEF4081B	quadruple 2-input AND gate	gates	14	D, P, T	391
HEF4082B	dual 4-input AND gate	gates	14	D, P, T	393
HEF4085B	dual 2-wide 2-input AND-OR-invert gate	gates	14	D, P, T	395
HEF4086B	4-wide 2-input AND-OR-invert gate	gates	14	D, P, T	397
HEF4093B	quadruple 2-input NAND Schmitt trigger	gates	14	D, P, T	401
HEF4094B	8-stage shift-and-store bus register	MSI	16	D, P, T	407
HEF4104B	quadruple low to high voltage translator	MSI	16	D, P, T	415
HEF4502B	strobed hex inverter/buffer	buffers	16	D, P, T	419
HEF4505B	64-bit static read/write RAM	LSI	14	D, P	423
HEF4508B	dual 4-bit latch	MSI	24	D, P	431
HEF4510B	BCD up/down counter	MSI	16	D, P, T	439
HEF4511B	BCD to 7-segment latch/decoder/driver	MSI	16	D, P, T	449
HEF4512B	8-input multiplexer with 3-state output	MSI	16	D, P, T	457
HEF4514B	1-of-16 decoder/demultiplexer with input latches	MSI	24	D, P	463
HEF4515B	1-of-16 decoder/demultiplexer with input latches	MSI	24	D, P	467
HEF4516B	binary up/down counter	MSI	16	D, P, T	471
HEF4517B	dual 64-bit static shift register	LSI	16	D, P	481
HEF4518B	dual BCD counter	MSI	16	D, P, T	489
HEF4519B	quadruple 2-input multiplexer	MSI	16	D, P, T	495
HEF4520B	dual binary counter	MSI	16	D, P, T	499
HEF4521B	24-stage frequency divider	MSI	16	D, P, T	505
HEF4522B	programmable 4-bit BCD down counter	MSI	16	D, P, T	515
HEF4526B	programmable 4-bit binary down counter	MSI	16	D, P, T	525
HEF4527B	BCD rate multiplier	MSI	16	D, P	535
HEF4528B	dual monostable multivibrator	MSI	16	D, P, T	543

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NUMERICAL INDEX

type number	function	category	pins	suffix *	page
HEF4531B	13-input parity checker/generator	MSI	16	D, P, T	549
HEF4532B	8-input priority encoder	MSI	16	D, P, T	553
HEF4534B	real time 5-decade counter	LSI	24	D, P	561
HEF4538B	dual precision monostable multivibrator	MSI	16	D, P, T	569
HEF4539B	dual 4-input multiplexer	MSI	16	D, P, T	577
HEF4541B	programmable timer	MSI	14	D, P, T	581
HEF4543B	BCD to 7-segment latch/decoder/driver	MSI	16	D, P, T	589
HEF4555B	dual 1-of-4 decoder/demultiplexer	MSI	16	D, P, T	595
HEF4556B	dual 1-of-4 decoder/demultiplexer	MSI	16	D, P, T	599
HEF4557B	1-to-64 bit variable length shift register	LSI	16	D, P, T	603
HEF4585B	4-bit magnitude comparator	MSI	16	D, P, T	609
HEF4720B;V	256-bit, 1-bit per word RAM	LSI	16	D, P	615
HEF4724B	8-bit addressable latch	MSI	16	D, P, T	631
HEF4731B;V	quadruple 64-bit static shift register	LSI	14	D, P	637
HEF4737B;V	quadruple static decade counters	LSI	18	D, P	641
HEF4738V	IEC/IEEE bus interface	LSI	40	P	649
HEF4739V	digital voltmeter circuit	LSI	28	P	657
HEF4750V	frequency synthesizer	LSI	28	D	663
HEF4751V	universal divider	LSI	28	D, P	679
HEF4752V	a.c. motor control circuit	LSI	28	D, P	689
HEF4753B	universal timer module	LSI	18	D, P	693
HEF4754V	18-element bar graph LCD driver	LSI	28	D, P	701
HEF40097B	3-state hex non-inverting buffer	buffers	16	D, P, T	707
HEF40098B	3-state hex inverting buffer	buffers	16	D, P, T	711
HEF40106B	hex Schmitt trigger	gates	14	D, P, T	715
HEF40160B	4-bit synchronous decade counter; asynchronous reset	MSI	16	D, P, T	721
HEF40161B	4-bit synchronous binary counter; asynchronous reset	MSI	16	D, P, T	731
HEF40162B	4-bit synchronous decade counter; synchronous reset	MSI	16	D, P, T	741
HEF40163B	4-bit synchronous binary counter; synchronous reset	MSI	16	D, P, T	751
HEF40174B	hex D-type flip-flop	MSI	16	D, P, T	761
HEF40175B	quadruple D-type flip-flop	MSI	16	D, P, T	765
HEF40192B	4-bit up/down decade counter	MSI	16	D, P, T	769
HEF40193B	4-bit up/down binary counter	MSI	16	D, P, T	777
HEF40194B	4-bit bidirectional universal shift register	MSI	16	D, P, T	785
HEF40195B	4-bit universal shift register	MSI	16	D, P, T	791
HEF40244B	octal buffers with 3-state outputs	MSI	20		799
HEF40245B	octal bus transceiver with 3-state outputs	MSI	20		801
HEF40373B	octal transparent latch with 3-state outputs	MSI	20		803
HEF40374B	octal D-type flip-flop with 3-state outputs	MSI	20		805

* Add the suffix to the type number on all orders.

D:ceramic package (DIL).

P:plastic package (DIL).

T:plastic flat pack (SO-package).

GENERAL

Rating systems

Handling MOS devices

Type number designation

Ordering information



RATING SYSTEMS

The rating systems described are those recommended by the International Electrotechnical Commission (IEC) in its Publication 134.

DEFINITIONS OF TERMS USED

Electronic device. An electronic tube or valve, transistor or other semiconductor device.

Note

This definition excludes inductors, capacitors, resistors and similar components.

Characteristic. A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic, or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

Bogey electronic device. An electronic device whose characteristics have the published nominal values for the type. A bogey electronic device for any particular application can be obtained by considering only those characteristics which are directly related to the application.

Rating. A value which establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms.

Note

Limiting conditions may be either maxima or minima.

Rating system. The set of principles upon which ratings are established and which determine their interpretation.

Note

The rating system indicates the division of responsibility between the device manufacturer and the circuit designer, with the object of ensuring that the working conditions do not exceed the ratings.

ABSOLUTE MAXIMUM RATING SYSTEM

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type as defined by its published data, which should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

The equipment manufacturer should design so that, initially and throughout life, no absolute maximum value for the intended service is exceeded with any device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices in the equipment.

DESIGN MAXIMUM RATING SYSTEM

Design maximum ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the electronic device under consideration.

The equipment manufacturer should design so that, initially and throughout life, no design maximum value for the intended service is exceeded with a bogey device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, variation in characteristics of all other devices in the equipment, equipment control adjustment, load variation, signal variation and environmental conditions.

DESIGN CENTRE RATING SYSTEM

Design centre ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under normal conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to rated supply voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in the characteristics of all electronic devices.

The equipment manufacturer should design so that, initially, no design centre value for the intended service is exceeded with a bogey electronic device in equipment operating at the stated normal supply voltage.

HANDLING MOS DEVICES

Though all our MOS integrated circuits incorporate protection against electrostatic discharges, they can nevertheless be damaged by accidental over-voltages. In storing and handling them, the following precautions are recommended.

Caution

Testing or handling and mounting call for special attention to personal safety. Personnel handling MOS devices should normally be connected to ground via a resistor.

Storage and transport

Store and transport the circuits in their original packing. Alternatively, use may be made of a conductive material or special IC carrier that either short-circuits all leads or insulates them from external contact.

Testing or handling

Work on a conductive surface (e.g. metal table top) when testing the circuits or transferring them from one carrier to another. Electrically connect the person doing the testing or handling to the conductive surface, for example by a metal bracelet and a conductive cord or chain. Connect all testing and handling equipment to the same surface.

Signals should not be applied to the inputs while the device power supply is off. All unused input leads should be connected to either the supply voltage or ground.

Mounting

Mount MOS integrated circuits on printed circuit boards *after* all other components have been mounted. Take care that the circuits themselves, metal parts of the board, mounting tools, and the person doing the mounting are kept at the same electric (ground) potential. If it is impossible to ground the printed-circuit board the person mounting the circuits should touch the board before bringing MOS circuits into contact with it.

Soldering

Soldering iron tips, including those of low-voltage irons, or soldering baths should also be kept at the same potential as the MOS circuits and the board.

Static charges

Dress personnel in clothing of non-electrostatic material (no wool, silk or synthetic fibres). After the MOS circuits have been mounted on the board proper handling precautions should still be observed. Until the sub-assemblies are inserted into a complete system in which the proper voltages are supplied, the board is no more than an extension of the leads of the devices mounted on the board. To prevent static charges from being transmitted through the board wiring to the device it is recommended that conductive clips or conductive tape be put on the circuit board terminals.

Transient voltages

To prevent permanent damage due to transient voltages, do not insert or remove MOS devices, or printed-circuit boards with MOS devices, from test sockets or systems with power on.

Voltage surges

Beware of voltage surges due to switching electrical equipment on or off, relays and d.c. lines.

**TYPE NUMBER
DESIGNATION**

**ORDERING
INFORMATION**

TYPE NUMBER DESIGNATION

HEF4XXXBX	complete type number
HE	family identification
F	operating temperature range: -40 to + 85 °C
4XXX	device number (may be 5 digits)
B	JEDEC 'B' series C-MOS specification (UB = unbuffered)
V	reduced supply voltage range
X	package code (e.g. P = plastic; D = ceramic; T = flat pack)

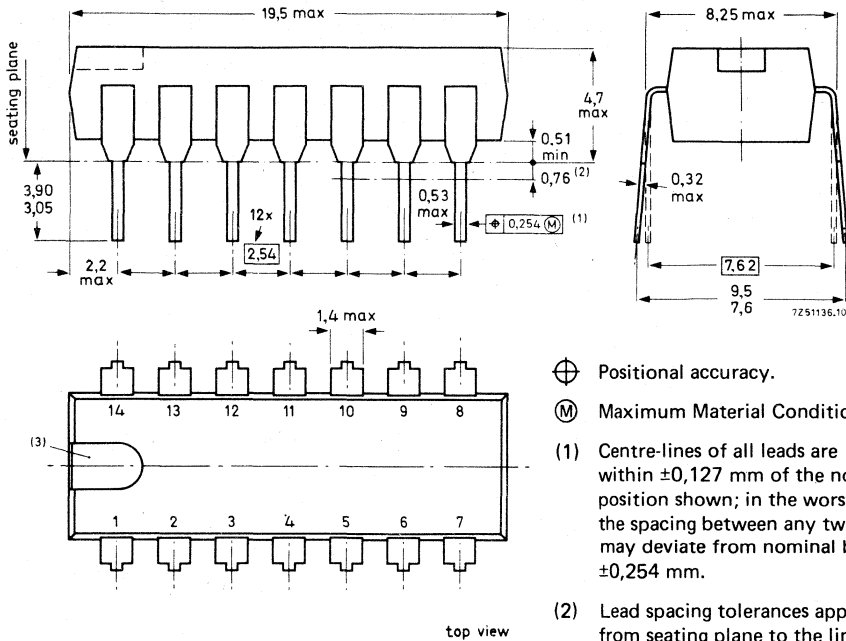
ORDERING INFORMATION

Always use the complete type number when ordering. Complete type numbers are given in the device data sheets.

PACKAGE OUTLINES



14-LEAD DUAL IN-LINE; PLASTIC (SOT-27S, T, V)



Dimensions in mm

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it).

If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

2. By dip or wave

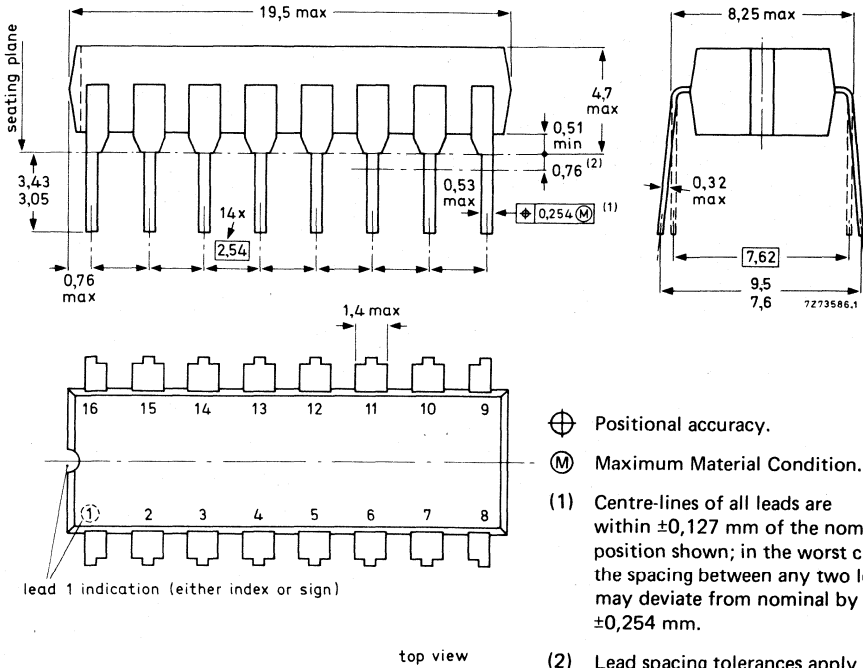
The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

16-LEAD DUAL IN-LINE; PLASTIC (SOT-38Z)



Dimensions in mm

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

2. By dip or wave

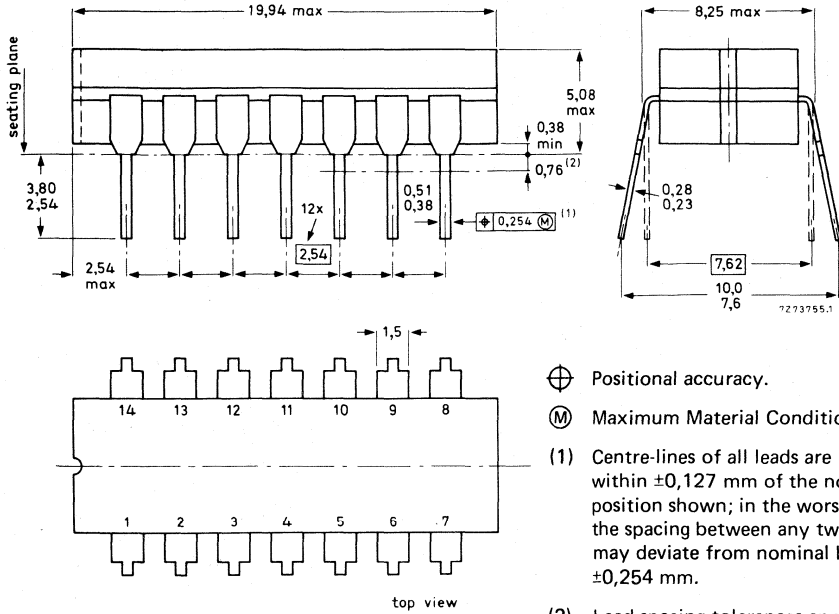
The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

14-LEAD DUAL IN-LINE; CERAMIC (SOT-73)

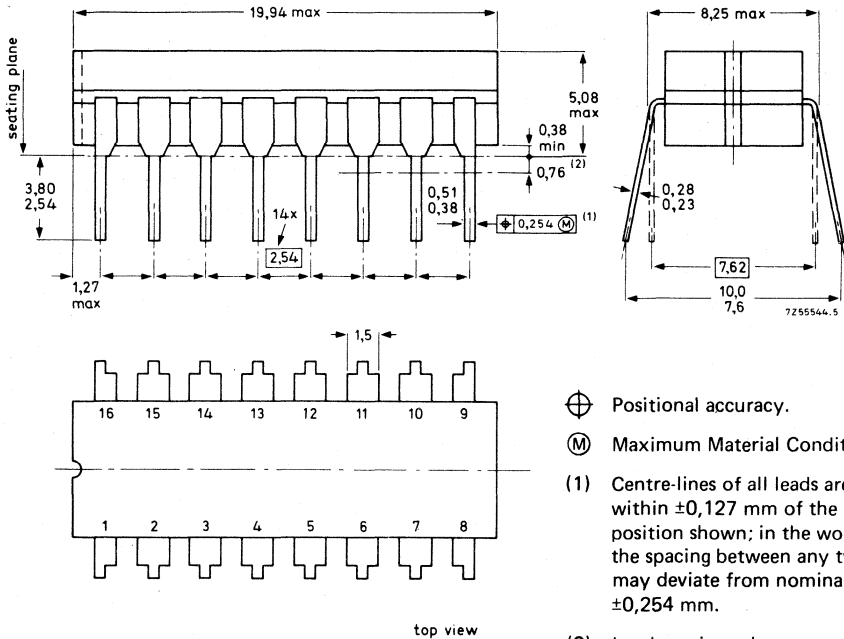


Dimensions in mm

Remarks

1. Leads are given positive misalignment so that they grip after insertion.
2. Leads are Ni-Fe, pure tin plated.

16-LEAD DUAL IN-LINE; CERAMIC (SOT-74)



Dimensions in mm

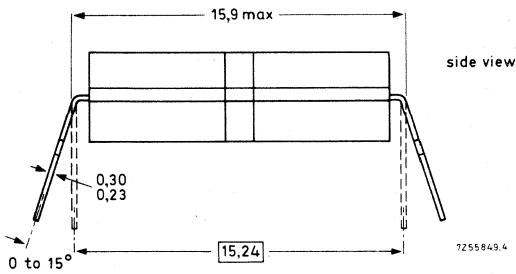
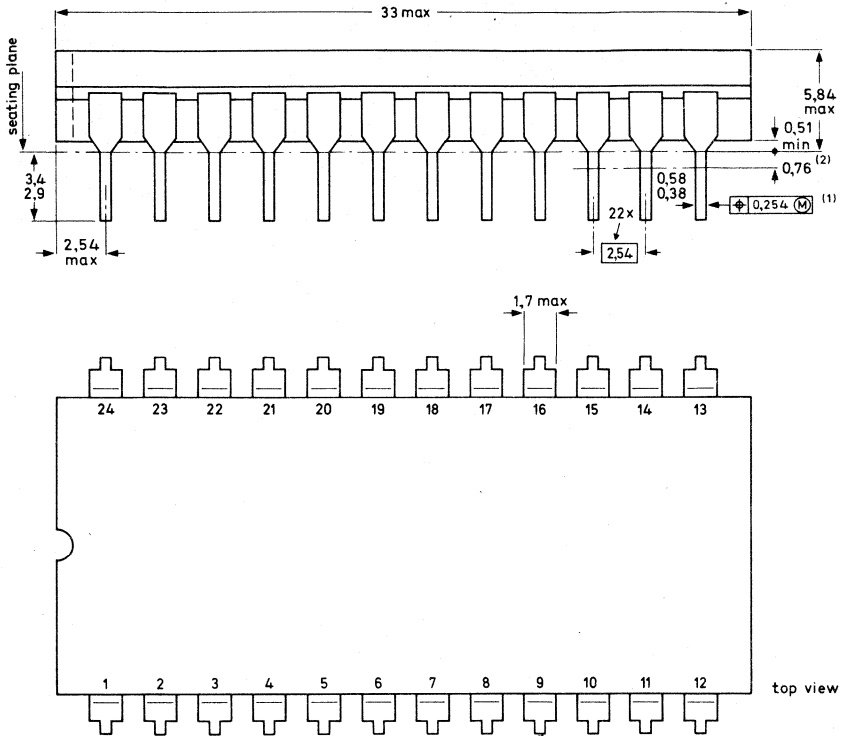
Remarks

1. Leads are given positive misalignment so that they grip after insertion.
2. Leads are Ni-Fe, pure tin plated.

- ⊕ Positional accuracy.
- Ⓜ Maximum Material Condition.

- (1) Centre-lines of all leads are within $\pm 0,127$ mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by $\pm 0,254$ mm.
- (2) Lead spacing tolerances apply from seating plane to the line indicated.

24-LEAD DUAL IN-LINE; CERAMIC (SOT-94)



⊕ Positional accuracy.

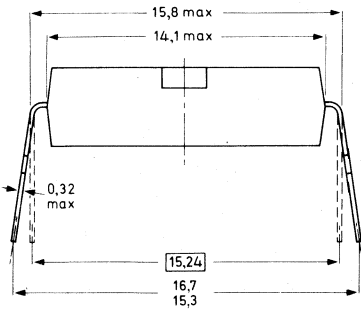
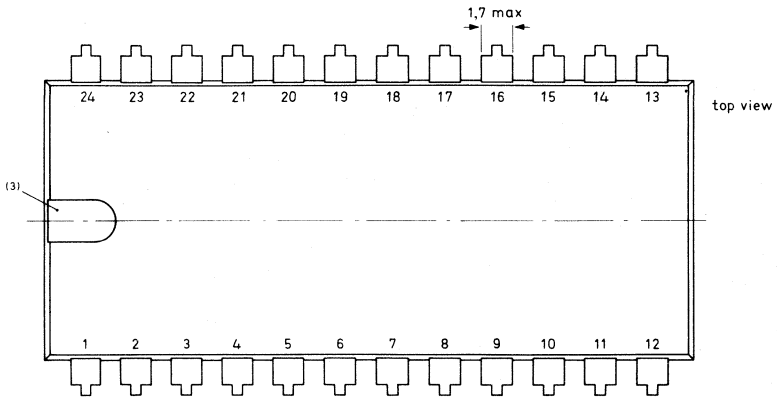
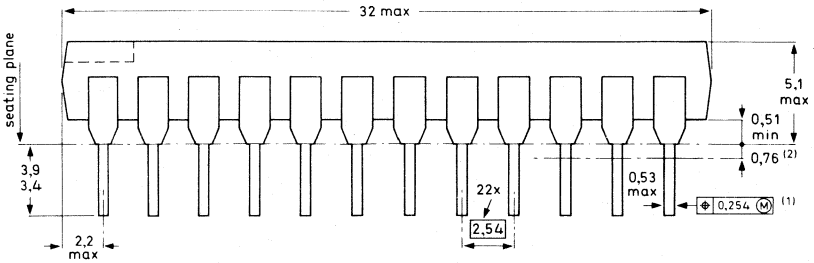
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within $\pm 0,127$ mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by $\pm 0,254$ mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

24-LEAD DUAL IN-LINE; PLASTIC (SOT-101A)



side view



Positional accuracy.



Maximum Material Condition.

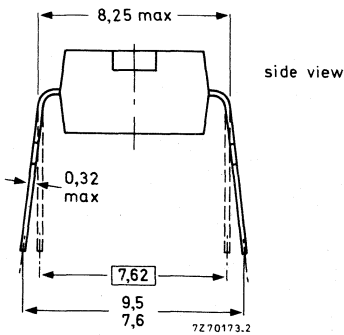
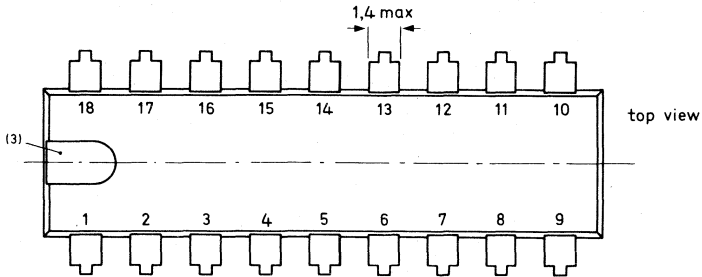
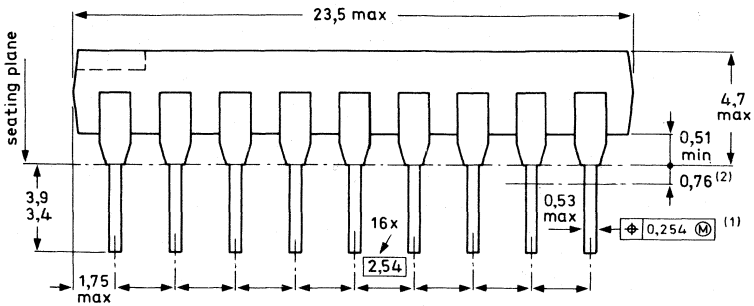
- (1) Centre-lines of all leads are within $\pm 0,127$ mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by $\pm 0,254$ mm.
- (2) Lead spacing tolerances apply from seating plane to the line indicated.
- (3) Index may be horizontal as shown, or vertical.

Dimensions in mm

SOLDERING

See SOT-38Z, for example.

18-LEAD DUAL IN-LINE; PLASTIC (SOT-102A)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

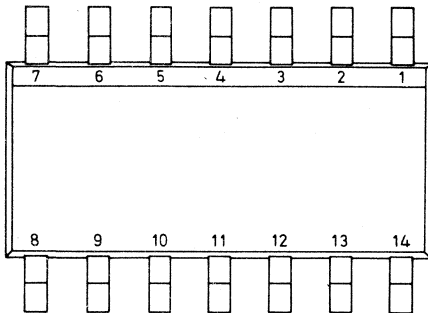
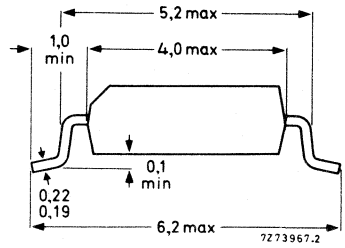
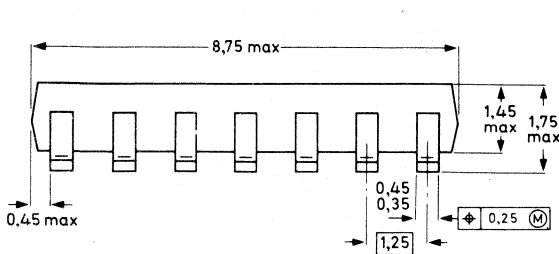
- (1) Centre-lines of all leads are within $\pm 0,127$ mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by $\pm 0,254$ mm.
- (2) Lead spacing tolerances apply from seating plane to the line indicated.
- (3) Index may be horizontal as shown, or vertical.

Dimensions in mm

SOLDERING

See SOT-38Z, for example.

14-LEAD FLAT PACK; PLASTIC (SO-14; SOT-108A)



top view

Dimensions in mm

- ⊕ Positional accuracy.
- Ⓜ Maximum Material Condition.

SOLDERING

The reflow solder technique

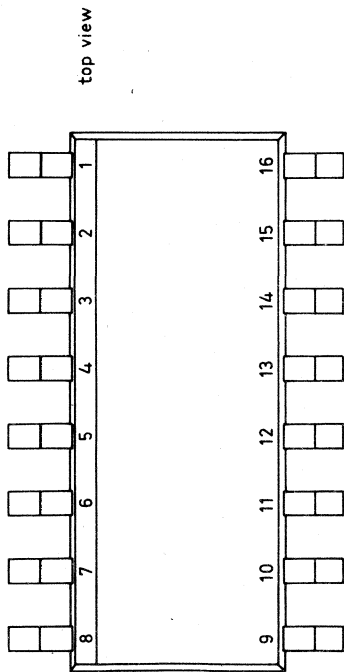
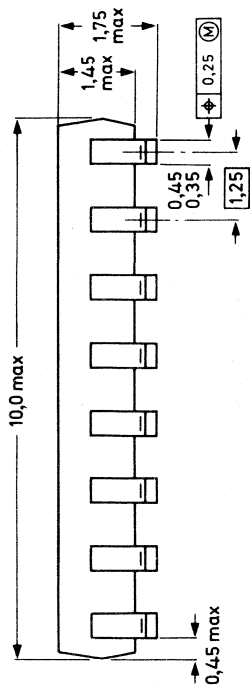
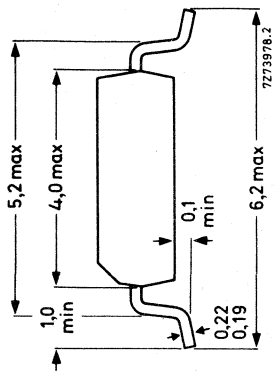
The preferred technique for mounting miniature components on hybrid thick or thin-film circuits is reflow soldering. Solder is applied to the required areas on the substrate by dipping in a solder bath or, more usually, by screen printing a solder paste. Components are put in place and the solder is reflowed by heating.

Solder pastes consist of very finely powdered solder and flux suspended in an organic liquid binder. They are available in various forms depending on the specification of the solder and the type of binder used. For hybrid circuit use, a tin-lead solder with 2 to 4% silver is recommended. The working temperature of this paste is about 220 to 230 °C when a mild flux is used.

For printing the paste onto the substrate a stainless steel screen with a mesh of 80 to 105 μm is used for which the emulsion thickness should be about 50 μm. To ensure that sufficient solder paste is applied to the substrate, the screen aperture should be slightly larger than the corresponding contact area.

The contact pins are positioned on the substrate, the slight adhesive force of the solder paste being sufficient to keep them in place. The substrate is heated to the solder working temperature preferably by means of a controlled hot plate. The soldering process should be kept as short as possible: 10 to 15 seconds is sufficient to ensure good solder joints and evaporation of the binder fluid. After soldering, the substrate must be cleaned of any remaining flux.

16-LEAD FLAT PACK; PLASTIC (SO-16; SOT-109A)



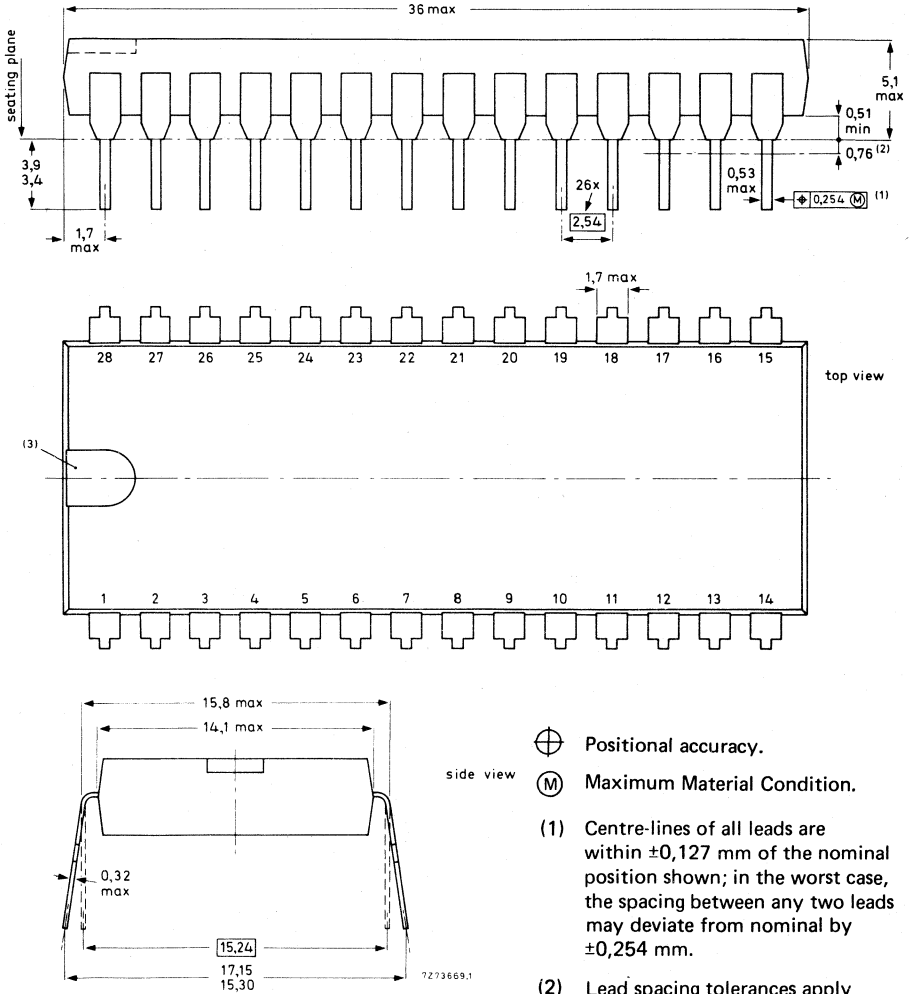
Dimensions in mm

- ⊕ Positional accuracy.
- Ⓜ Maximum Material Condition.

SOLDERING

See SOT-108A, for example.

28-LEAD DUAL IN-LINE; PLASTIC (SOT-117)



Dimensions in mm

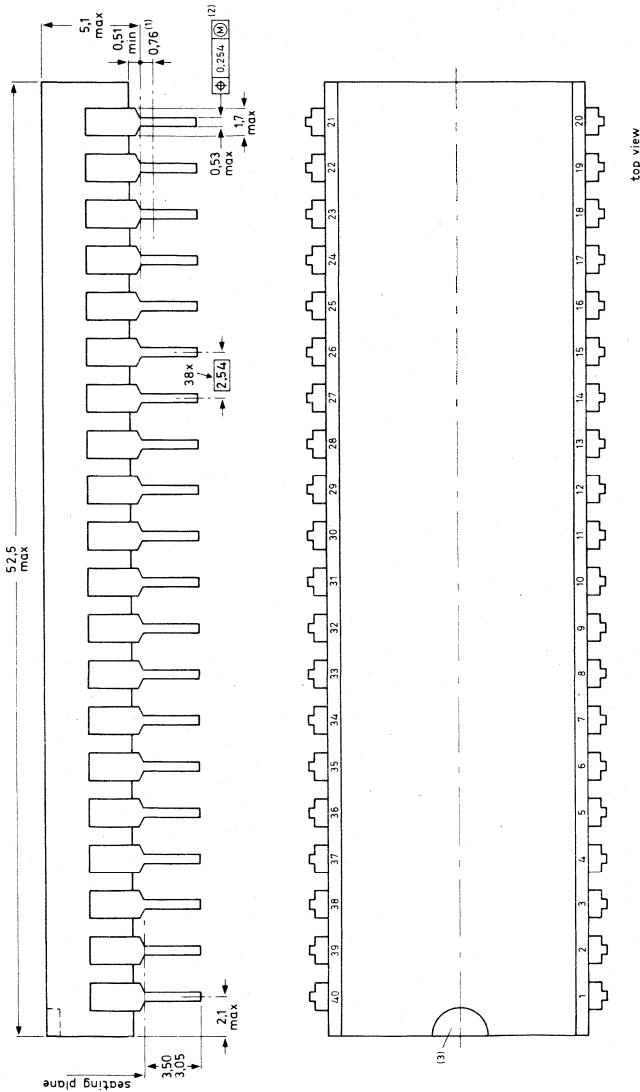
SOLDERING

See SOT-38Z, for example.

- ⊕ Positional accuracy.
- (M) Maximum Material Condition.

- (1) Centre-lines of all leads are within $\pm 0,127$ mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by $\pm 0,254$ mm.
- (2) Lead spacing tolerances apply from seating plane to the line indicated.
- (3) Index may be horizontal as shown, or vertical.

40-LEAD DUAL IN-LINE; PLASTIC (SOT-129)



Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

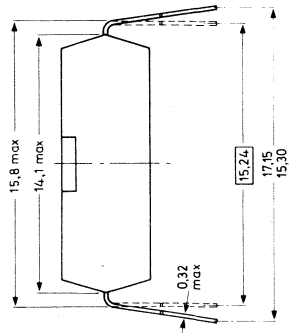
- (1) Centre-lines of all leads are within ± 0.127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ± 0.254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

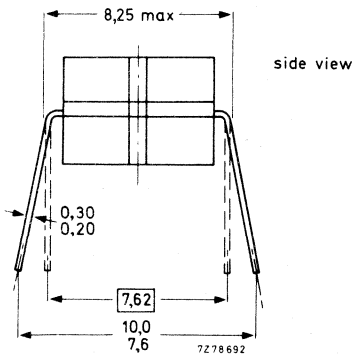
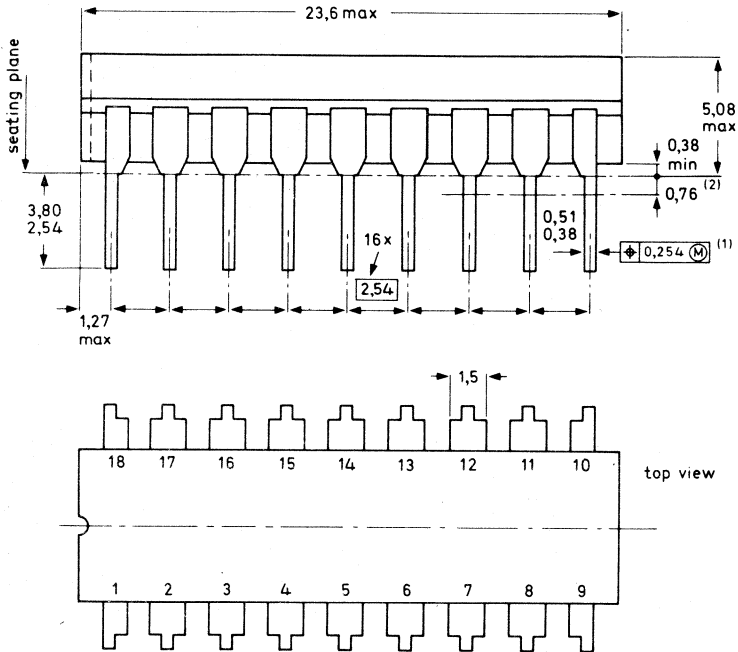
(3) Index may be horizontal as shown, or vertical.

SOLDERING

See SOT-38Z, for example.



18-LEAD DUAL IN-LINE; CERAMIC (SOT-133)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within $\pm 0,127$ mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by $\pm 0,254$ mm.

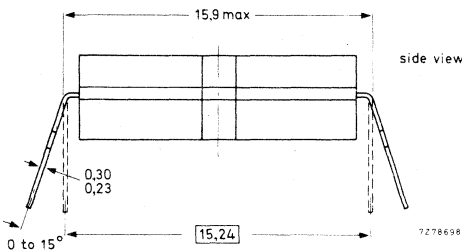
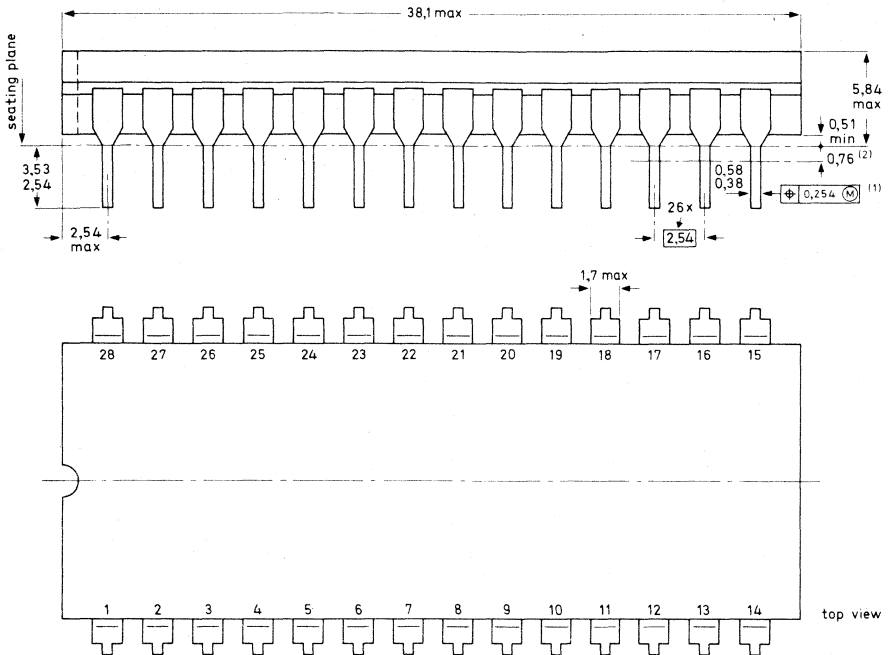
(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

Remarks

1. Leads are given positive misalignment so that they grip after insertion.
2. Leads are Ni-Fe, pure tin plated.

28-LEAD DUAL IN-LINE; CERAMIC (SOT-135)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

- (1) Centre-lines of all leads are within $\pm 0,127$ mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by $\pm 0,254$ mm.
- (2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

Remarks

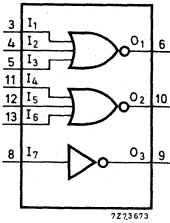
1. Leads are given positive misalignment so that they grip after insertion.
2. Leads are Ni-Fe, pure tin plated.

FUNCTIONAL DIAGRAMS



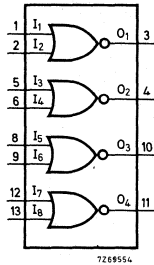
FUNCTIONAL DIAGRAMS

HEF4000B



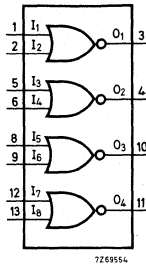
Dual 3-input NOR gate and inverter.

HEF4001B



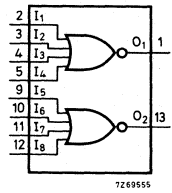
Quadruple 2-input NOR gate.

HEF4001UB



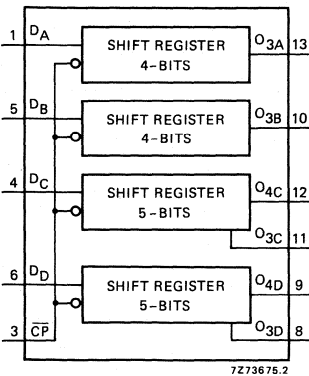
Quadruple 2-input NOR gate; unbuffered.

HEF4002B



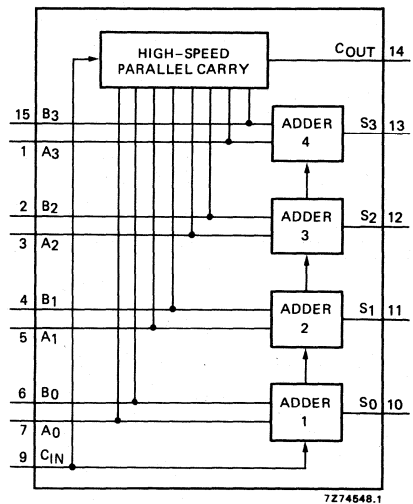
Dual 4-input NOR gate.

HEF4006B



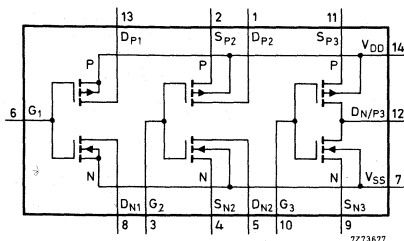
18-stage static shift register.

HEF4008B



4-bit binary full adder.

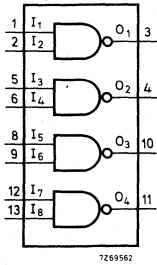
HEF4007UB



Dual complementary pair and inverter; unbuffered.

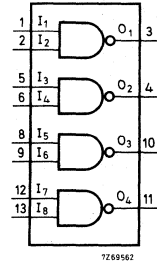
FUNCTIONAL DIAGRAMS

HEF4011B



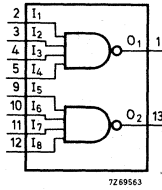
Quadrate 2-input NAND gate.

HEF4011UB



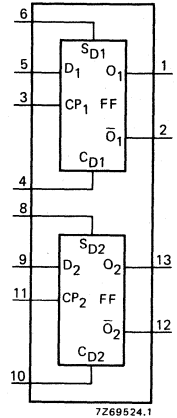
Quadrate 2-input NAND gate; unbuffered.

HEF4012B



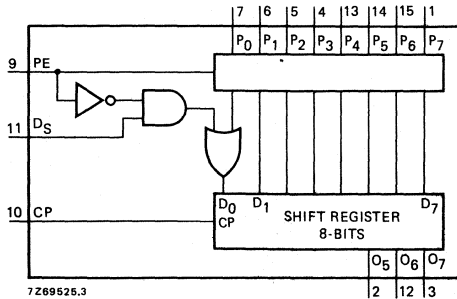
Dual 4-input NAND gate.

HEF4013B



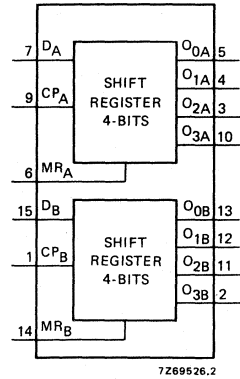
Dual D-type flip-flop.

HEF4014B



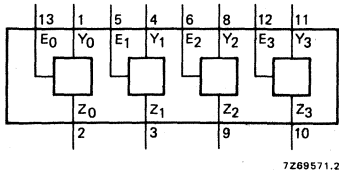
8-bit static shift register.

HEF4015B



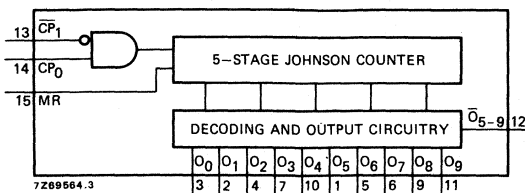
Dual 4-bit static shift register

HEF4016B



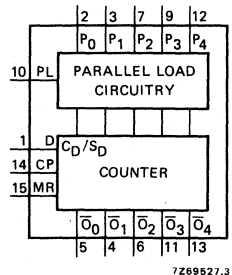
Quadrate bilateral switches.

HEF4017B



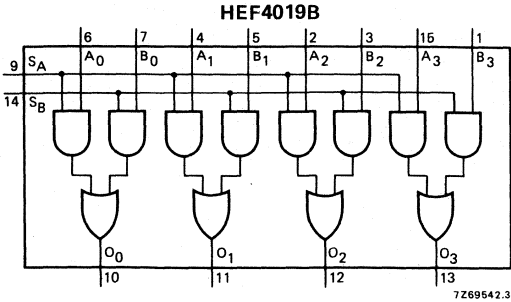
5-stage Johnson counter.

HEF4018B

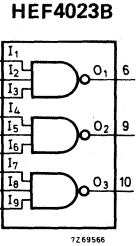


Presettable divide-by-n counter.

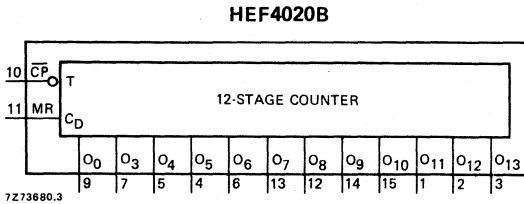
FUNCTIONAL DIAGRAMS



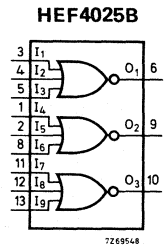
Quaduple 2-input multiplexer.



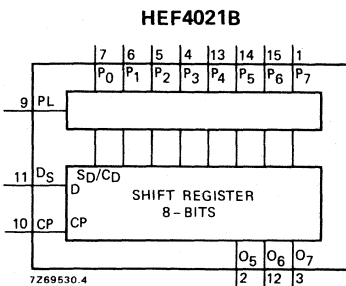
Triple 3-input NAND gate.



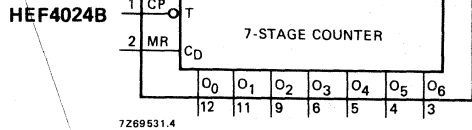
14-stage binary counter.



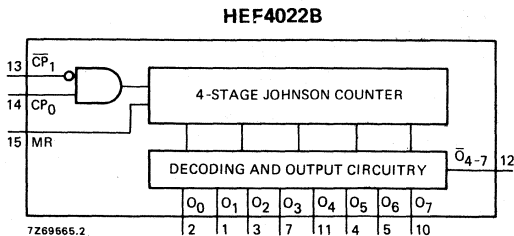
Triple 3-input NOR gate.



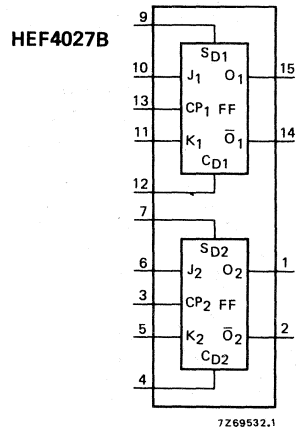
8-bit static shift register.



7-stage binary counter.



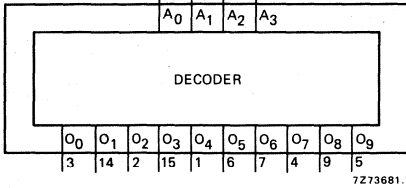
4-stage divide-by-8 Johnson counter.



Dual JK flip-flop.

FUNCTIONAL DIAGRAMS

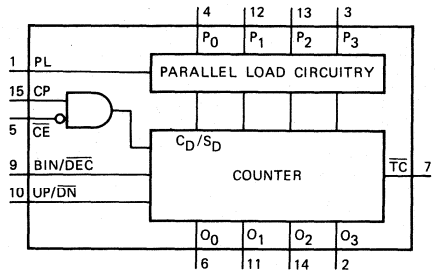
HEF4028B



1-of-10 decoder.

7273681.1

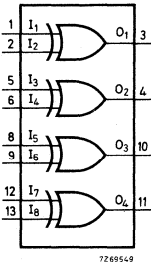
HEF4029B



Synchronous up/down counter, binary/decade counter.

7273683.2

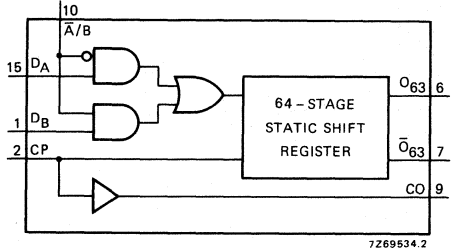
HEF4030B



Quadruple EXCLUSIVE-OR gate.

7269549

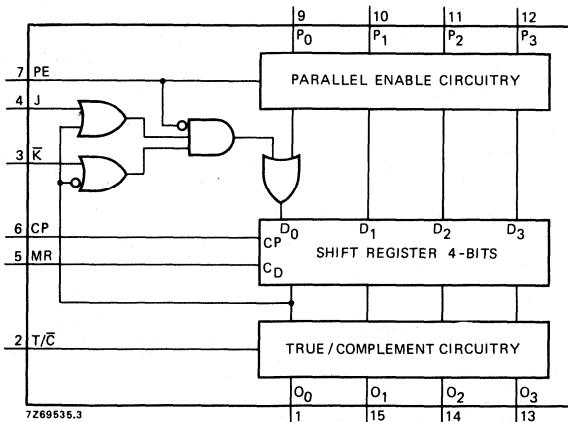
HEF4031B



64-stage static shift register.

7269534.2

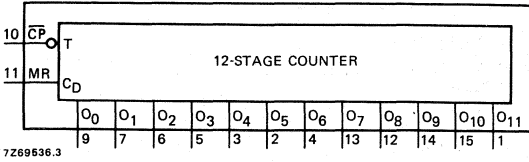
HEF4035B



4-bit universal shift register.

7269535.3

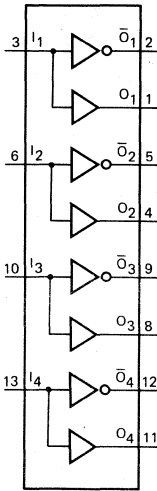
HEF4040B



7Z69536.3

12-stage binary counter.

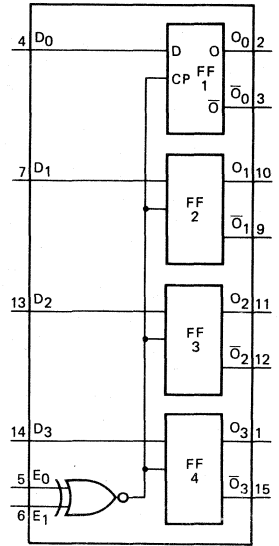
HEF4041B



7Z75422.1

Quadruple true/complement
buffer.

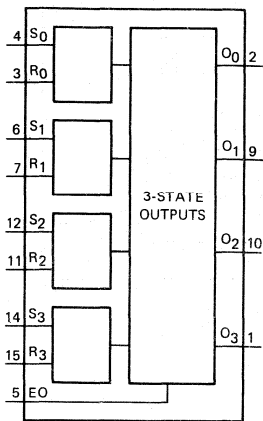
HEF4042B



7Z69550.3

Quadruple D-latch.

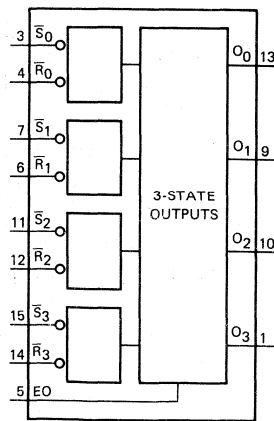
HEF4043B



7Z73687.3

Quadruple R/S latch with 3-state outputs.

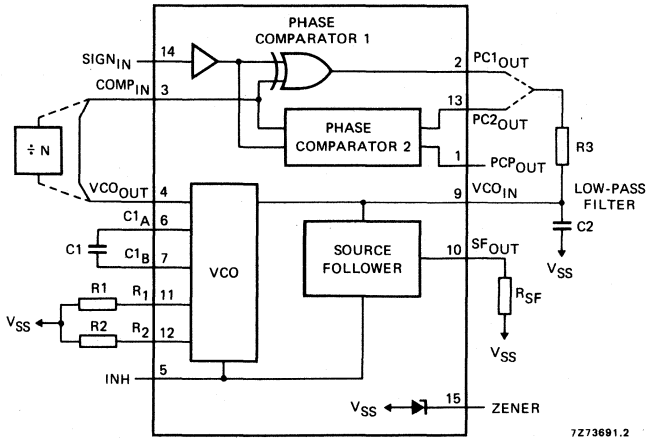
HEF4044B



7Z73689.3

Quadruple R/S latch with 3-state outputs.

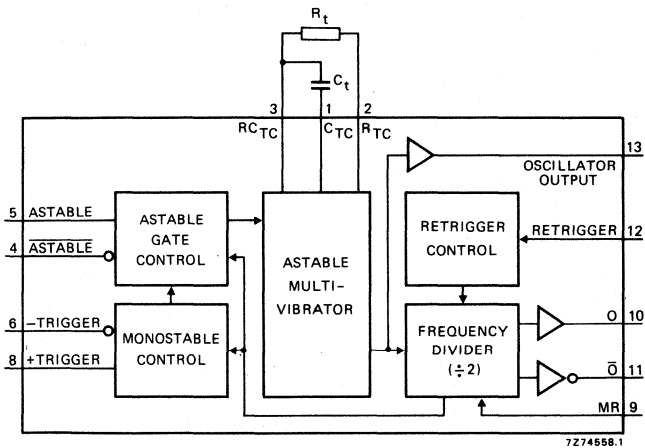
HEF4046B



7273691.2

Phase-locked loop.

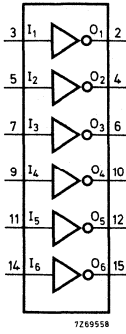
HEF4047B



7274558.1

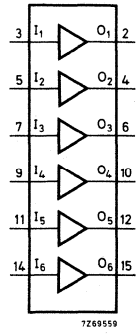
Monostable/astable multivibrator.

HEF4049B



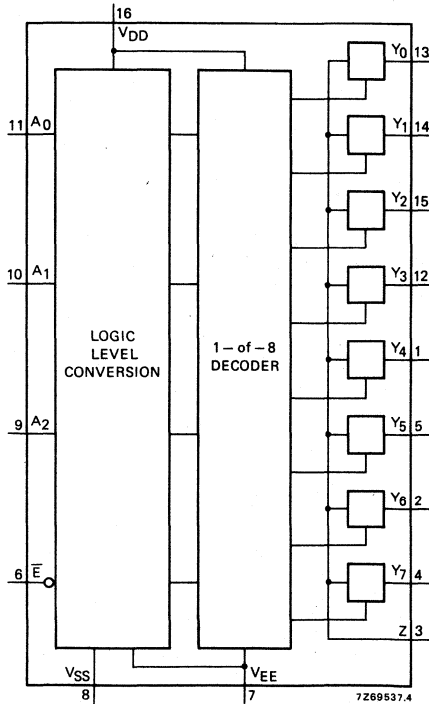
Hex inverting buffers.

HEF4050B



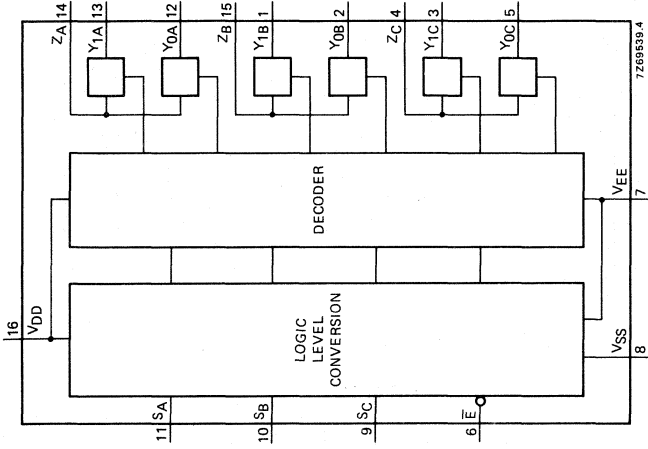
Hex non-inverting buffers.

HEF4051B



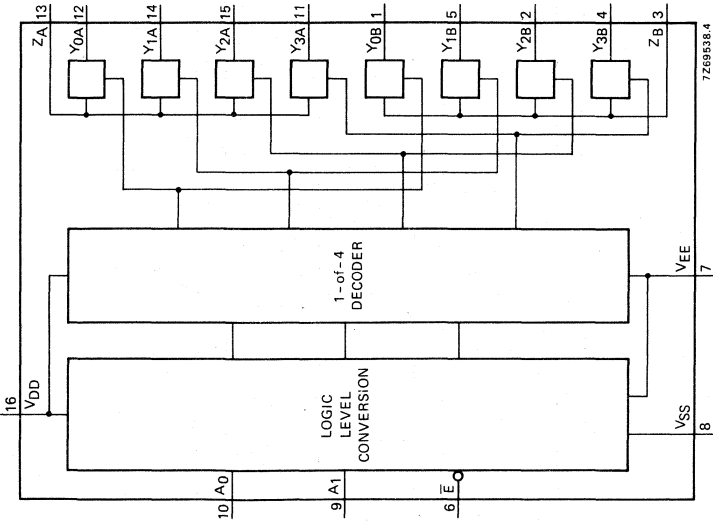
8-channel analogue multiplexer/demultiplexer.

HEF4053B



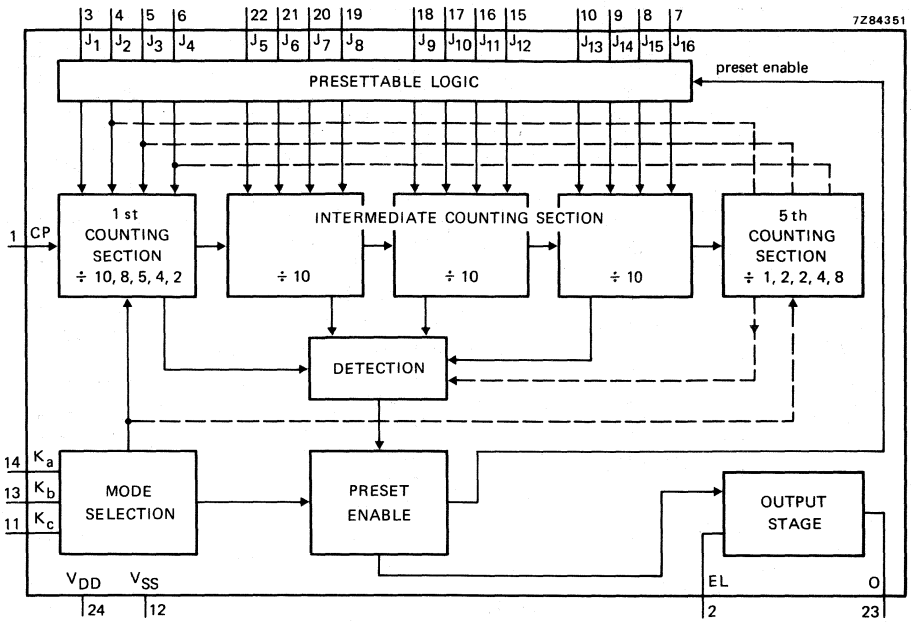
Triples 2-channel analogue multiplexer/demultiplexer.

HEF4052B



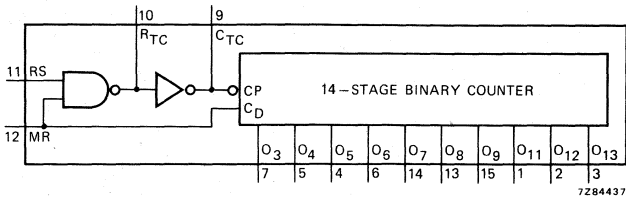
Dual 4-channel analogue multiplexer/demultiplexer.

HEF4059B



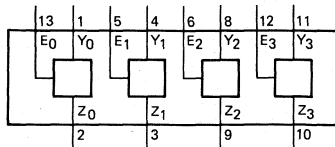
Programmable divide-by-n counter.

HEF4060B



14-stage ripple-carry binary counter/divider and oscillator.

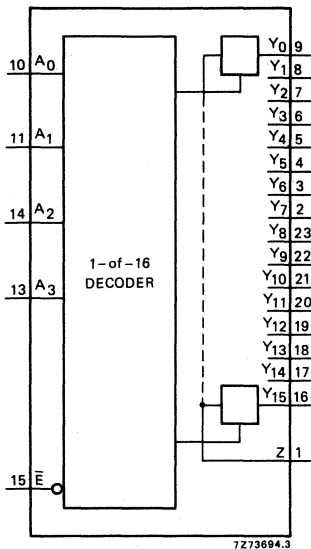
HEF4066B



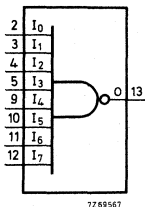
Quadruple bilateral switches.

FUNCTIONAL DIAGRAMS

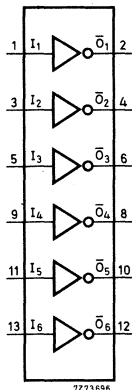
HEF4067B



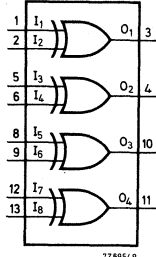
HEF4068B



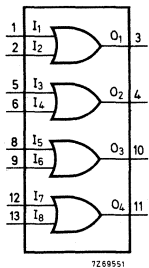
HEF4069UB



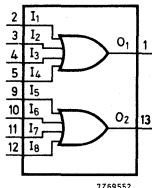
HEF4070B



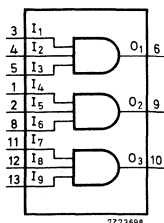
HEF4071B



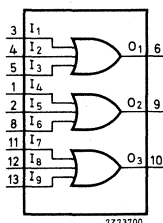
HEF4072B



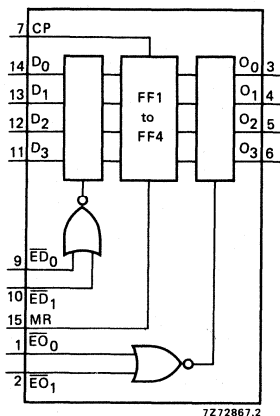
HEF4073B



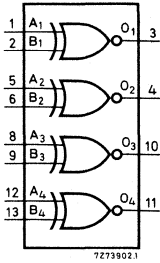
HEF4075B



HEF4076B

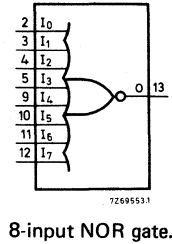


HEF4077B



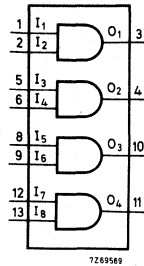
Quadruple EXCLUSIVE-NOR gate.

HEF4078B



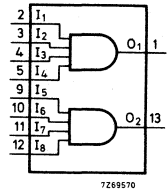
8-input NOR gate.

HEF4081B



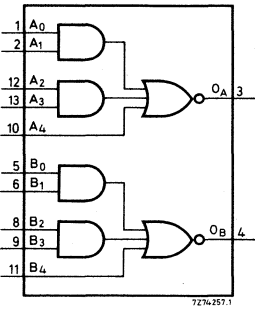
Quadruple 2-input AND gate.

HEF4082B



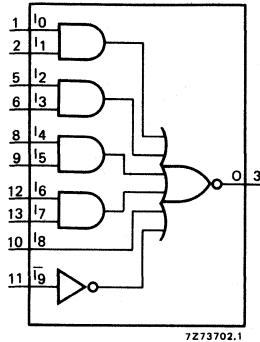
Dual 4-input AND gate.

HEF4085B



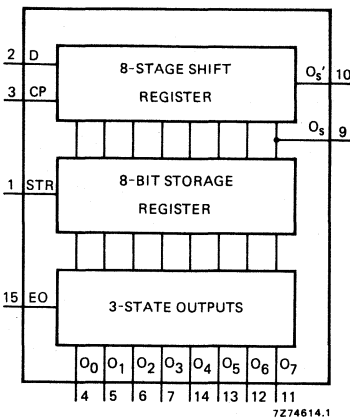
Dual 2-wide 2-input AND-OR-INVERT gate.

HEF4086B



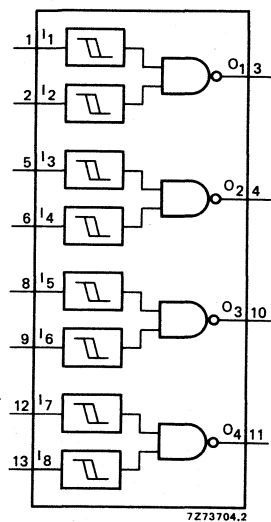
4-wide 2-input AND-OR-INVERT gate.

HEF4094B



8-stage shift-and-store bus register.

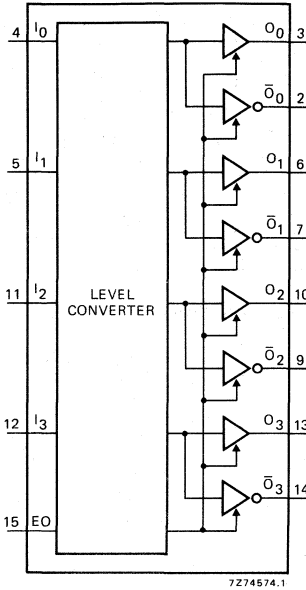
HEF4093B



Quadruple 2-input NAND Schmitt trigger.

FUNCTIONAL DIAGRAMS

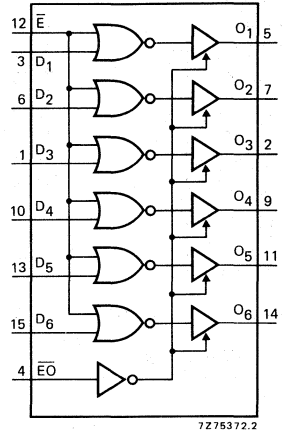
HEF4104B



Quadruple low-to-high
voltage translator
with 3-state outputs.

7274574.1

HEF4502B

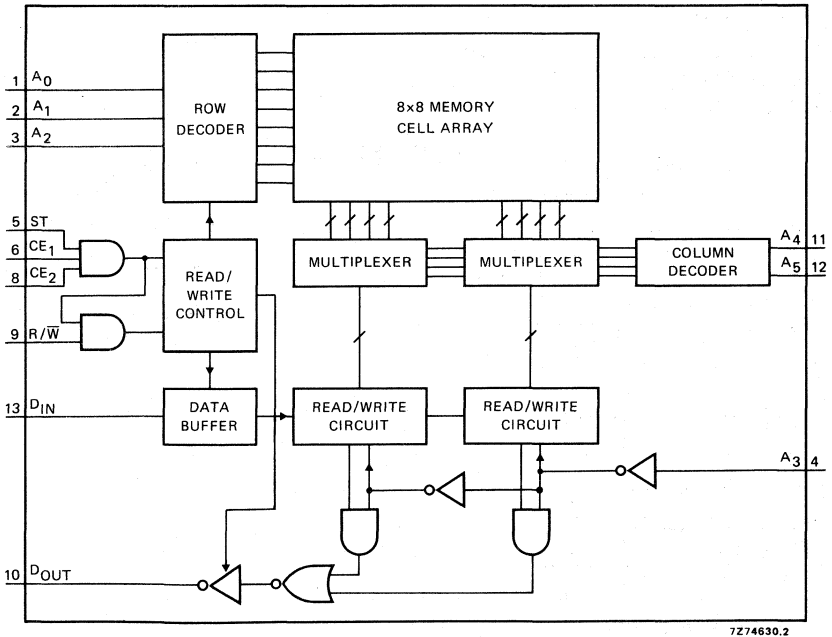


Strobed hex inverter/buffer.

7275372.2

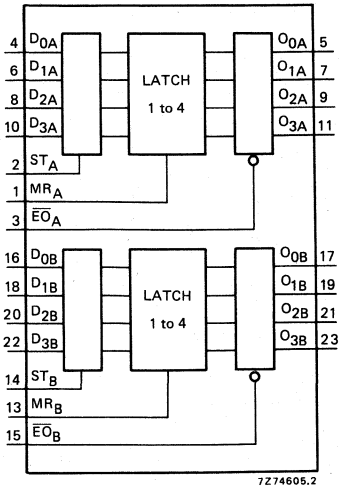
HEF4505B

64-bit, 1-bit per word random
access read/write memory.



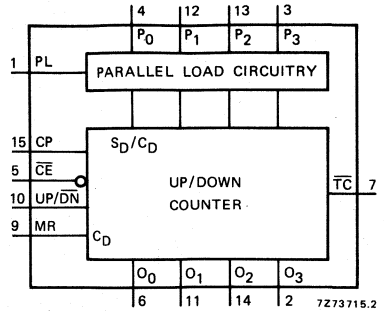
7274630.2

HEF4508B



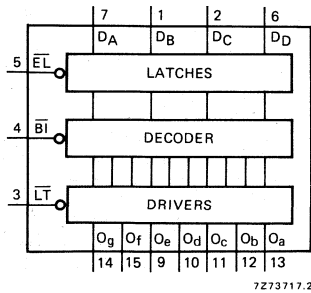
Dual 4-bit latch.

HEF4510B



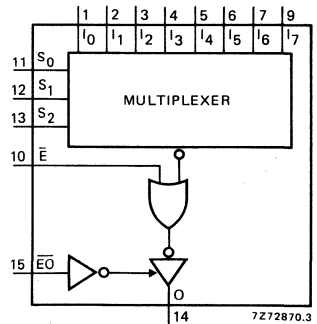
BCD up/down counter.

HEF4511B



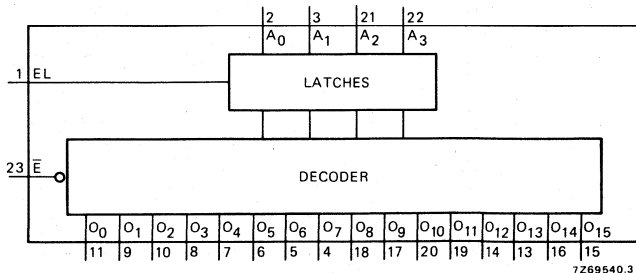
BCD to 7-segment latch/decoder/driver.

HEF4512B



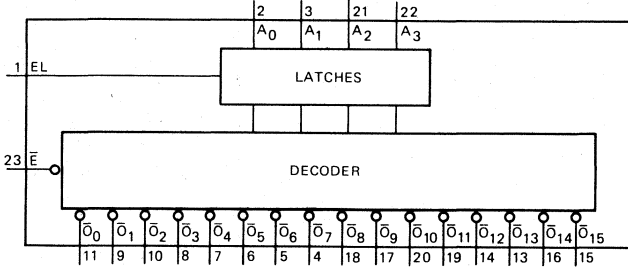
8-input multiplexer with 3-state output.

HEF4514B



1-of-16 decoder/demultiplexer with input latches.

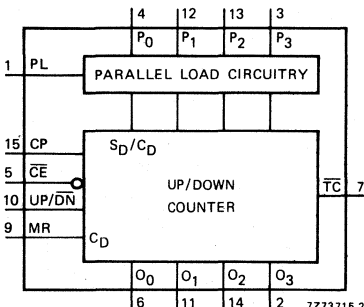
HEF4515B



1-of-16 decoder/demultiplexer with input latches.

7284275

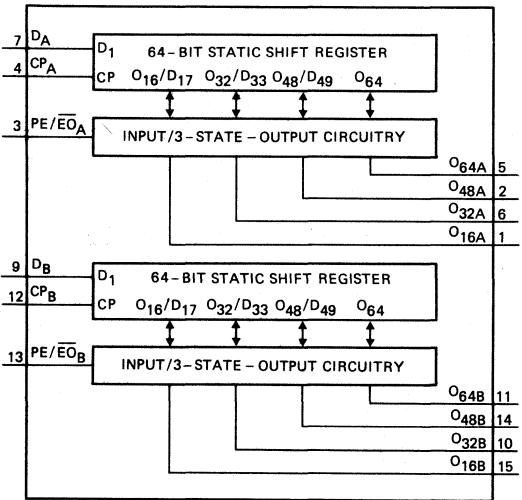
HEF4516B



Binary up/down counter.

7273715.2

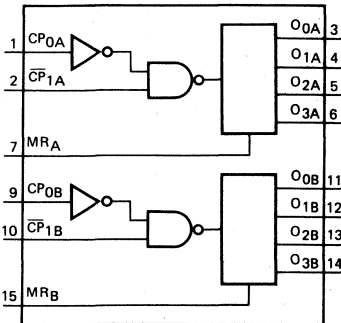
HEF4517B



Dual 64-bit static shift register.

7274689.1

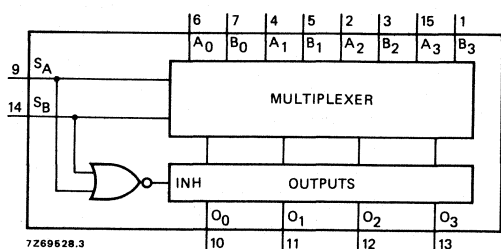
HEF4518B



Dual BCD counter.

7269556.1

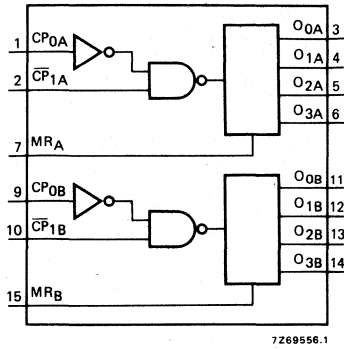
HEF4519B



Quadruple 2-input multiplexer.

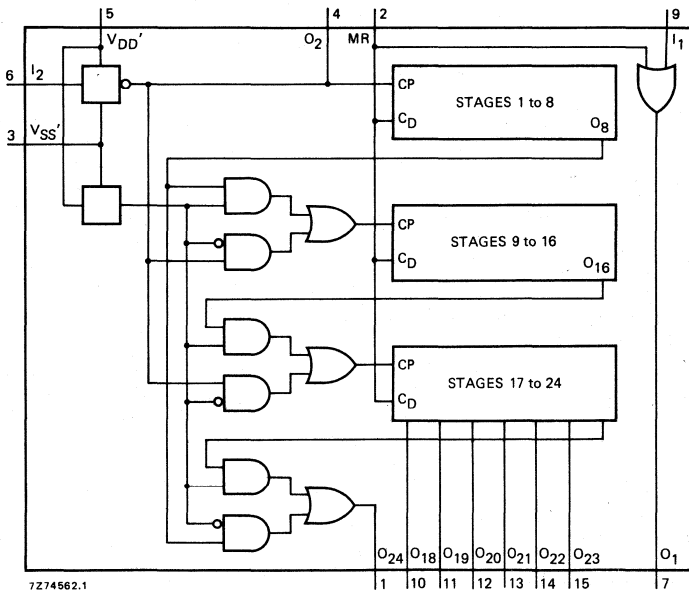
7269528.3

HEF4520B



Dual binary counter.

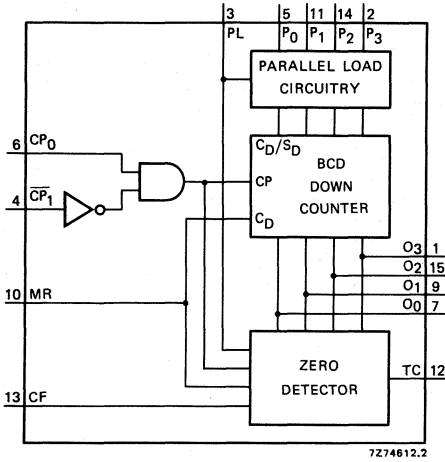
HEF4521B



24-stage frequency divider.

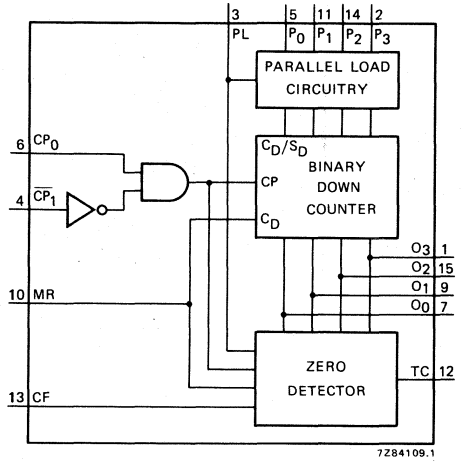
FUNCTIONAL DIAGRAMS

HEF4522B



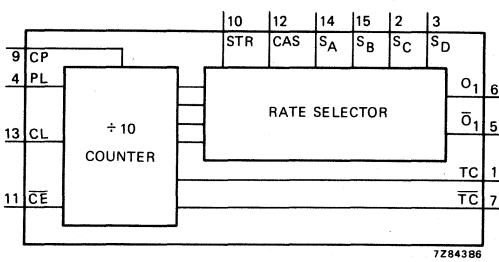
Programmable 4-bit BCD down counter.

HEF4526B



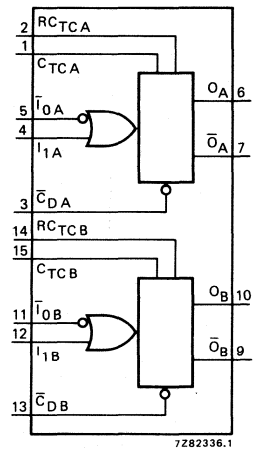
Programmable 4-bit binary down counter.

HEF4527B



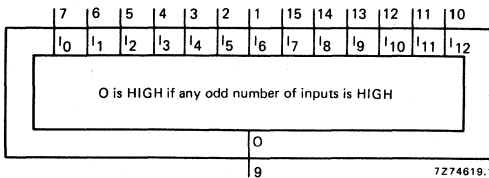
BCD rate multiplier.

HEF4528B



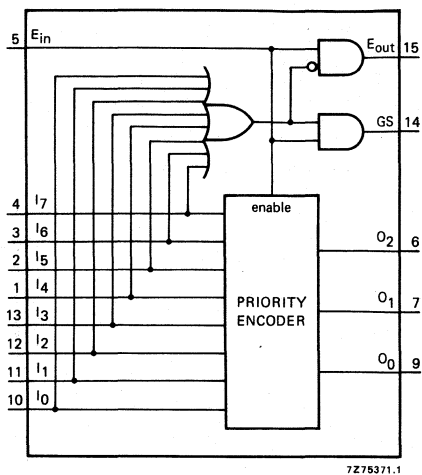
Dual monostable multivibrator.

HEF4531B



13-input parity checker/generator.

HEF4532B

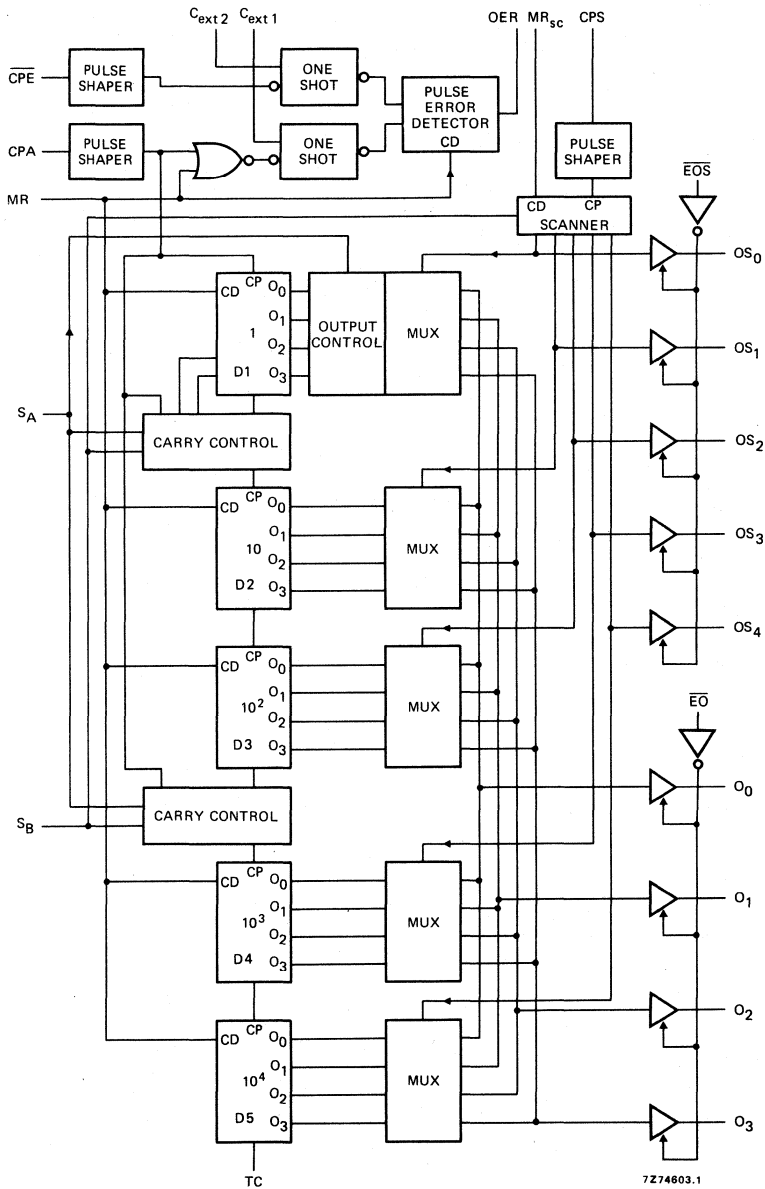


8-input priority encoder.



FUNCTIONAL DIAGRAMS

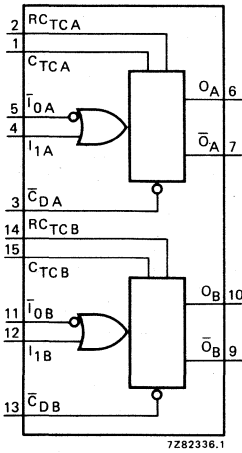
HEF4534B



7274603.1

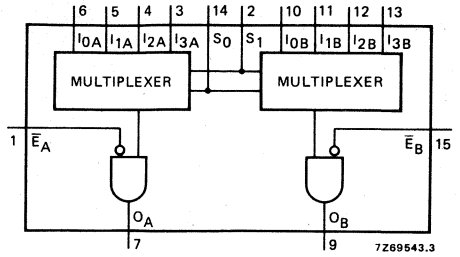
Real time 5-decade counter.

HEF4538B



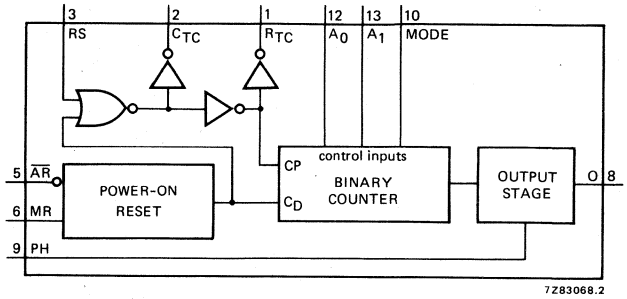
Dual precision monostable multivibrator.

HEF4539B



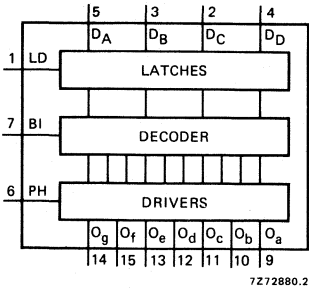
Dual 4-input multiplexer.

HEF4541B



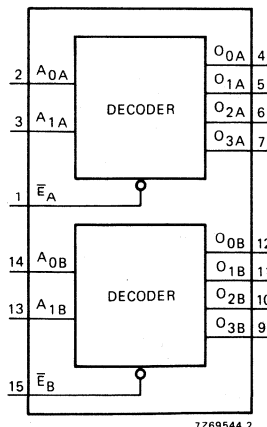
Programmable timer.

HEF4543B



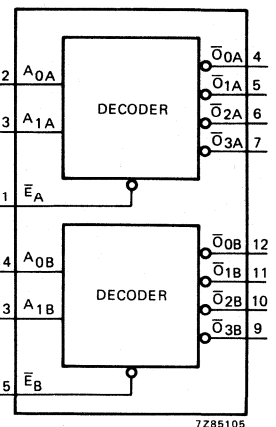
BCD to 7-segment latch/decoder/driver.

HEF4555B



Dual 1-of-4 decoder/demultiplexer.

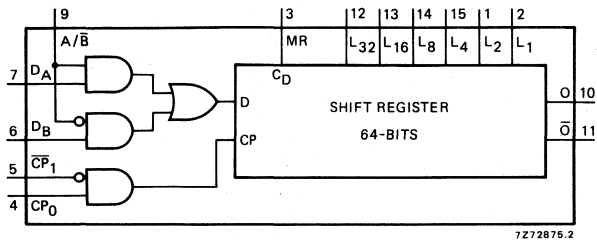
HEF4556B



Dual 1-of-4 decoder/demultiplexer.

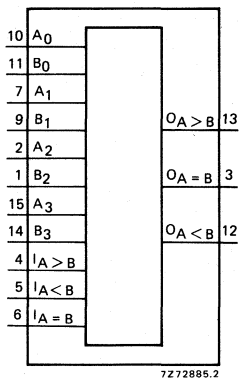
FUNCTIONAL DIAGRAMS

HEF4557B



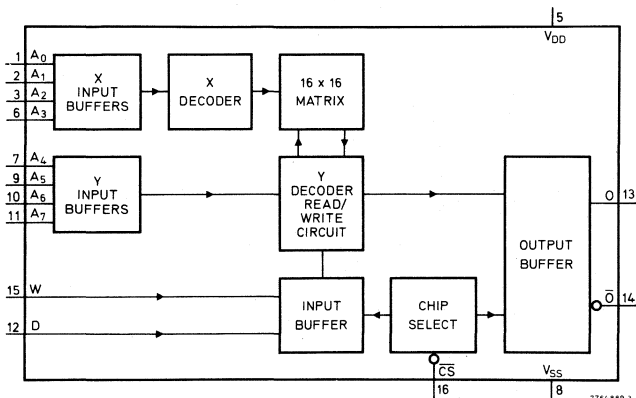
1-to-16 bit variable length shift register.

HEF4585B



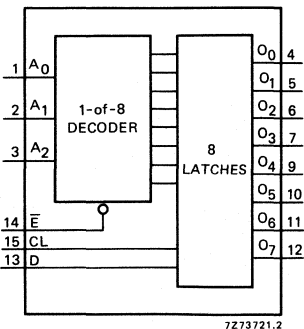
4-bit magnitude comparator.

HEF4720B; V



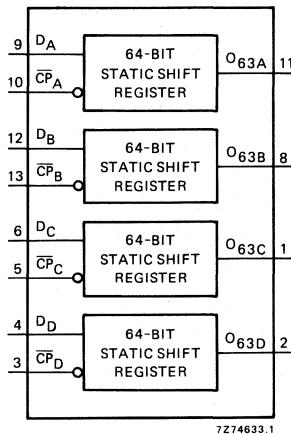
256-bit, 1-bit per word RAM.

HEF4724B



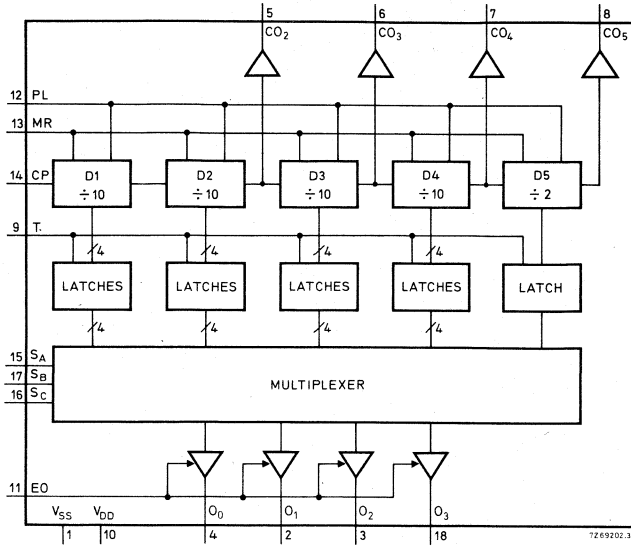
8-bit addressable latch.

HEF4731B; V



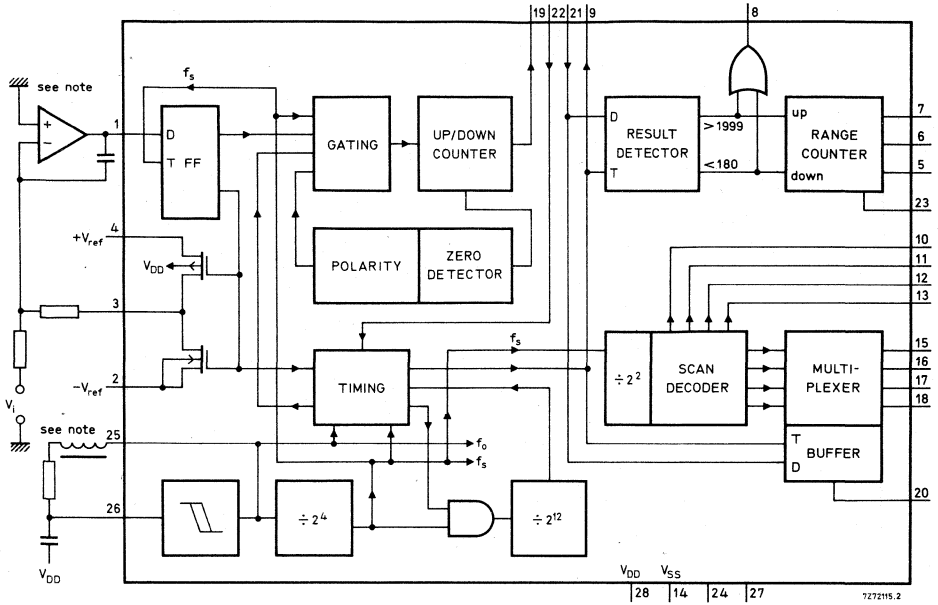
Quadruple 64-bit static shift register.

HEF4737B; V



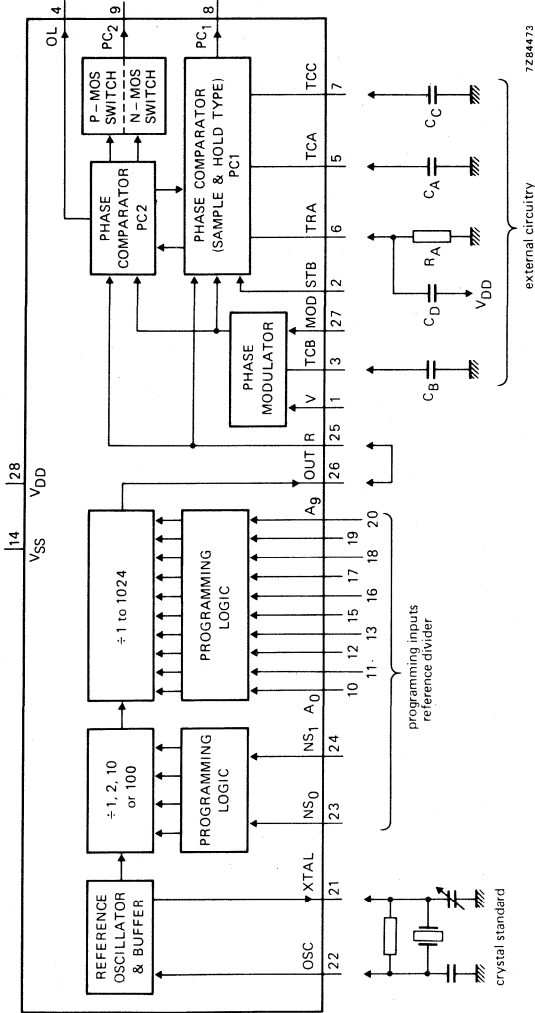
Quadruple static decade counter.

HEF4739V



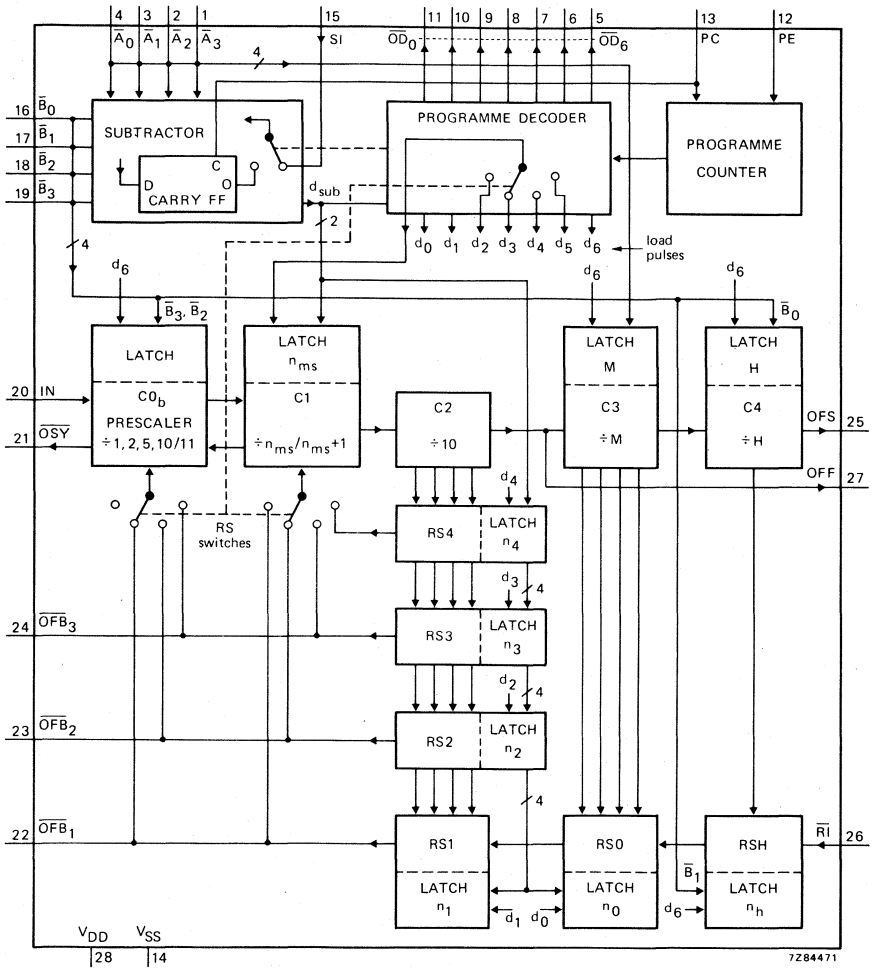
Digital voltmeter circuit.

HEF4750V



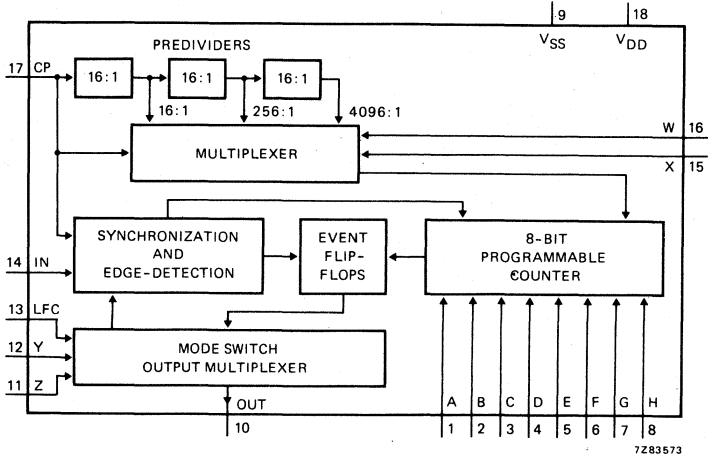
Frequency synthesizer.

HEF4751V



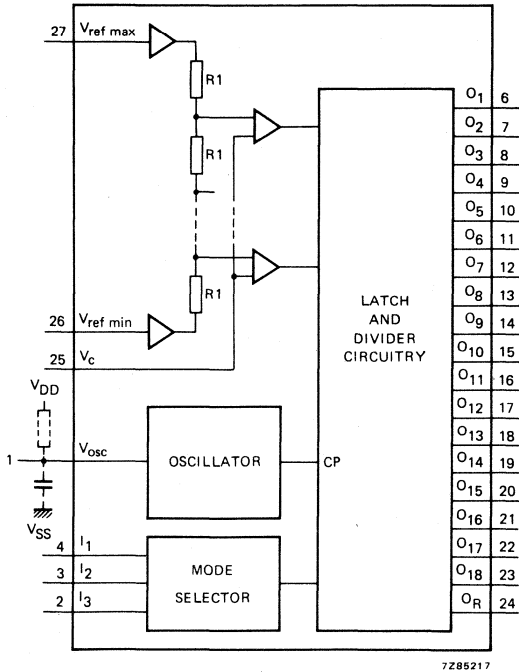
Universal divider.

HEF4753B



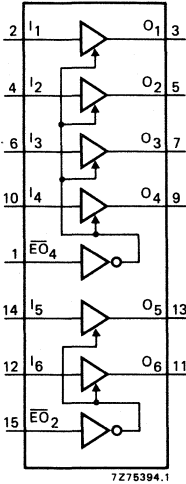
Universal timer module.

HEF4754V



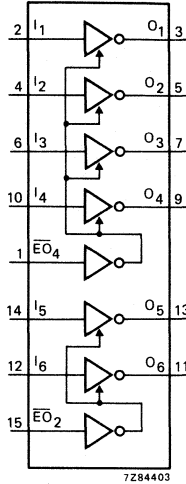
18-element bargraph LCD driver.

HEF40097B



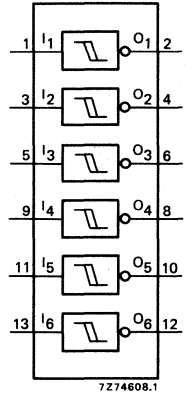
3-state hex non-inverting
buffer.

HEF40098B



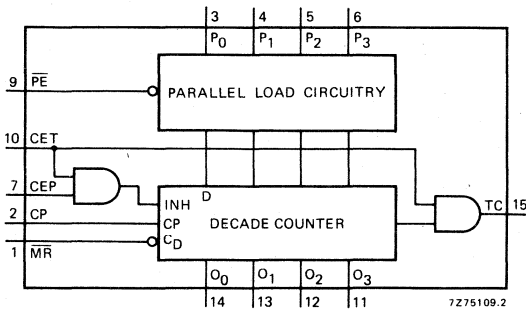
3-state hex inverting
buffer.

HEF40106B



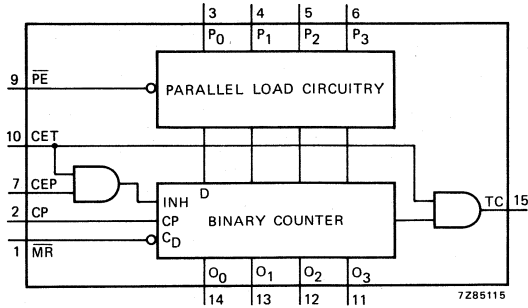
Hex Schmitt trigger.

HEF40160B



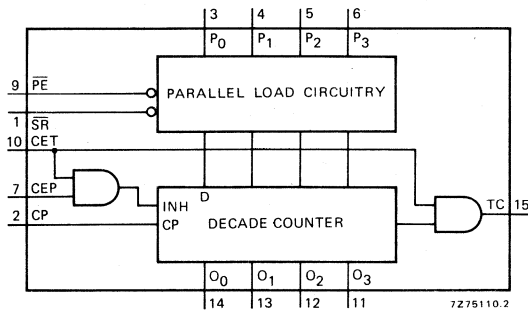
4-bit synchronous decade counter
with asynchronous reset.

HEF40161B



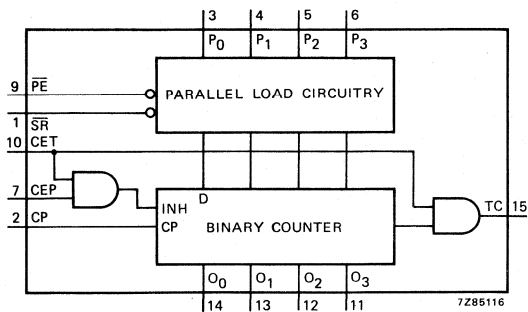
4-bit synchronous binary counter
with asynchronous reset.

HEF40162B



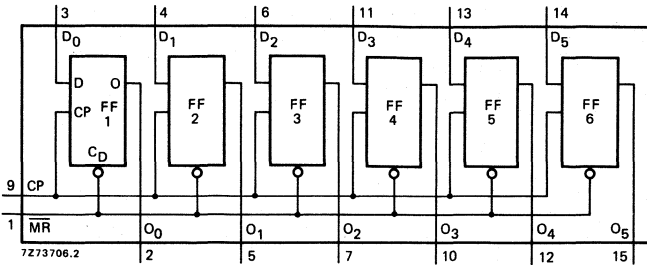
4-bit synchronous decade counter
with synchronous reset.

HEF40163B



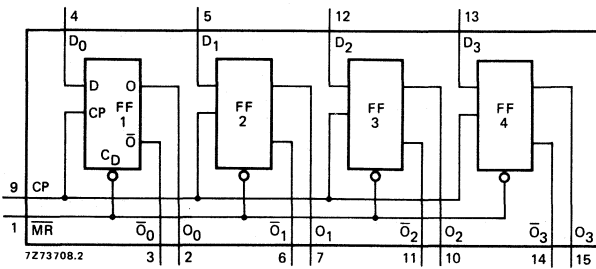
4-bit synchronous binary counter
with synchronous reset.

HEF40174B



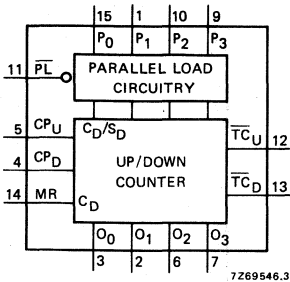
Hex D-type flip-flop.

HEF40175B



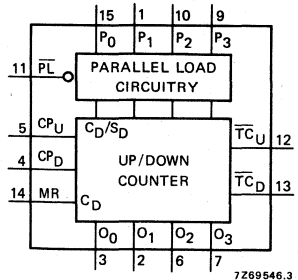
Quadruple D-type flip-flop.

HEF40192B



4-bit up/down decade counter.

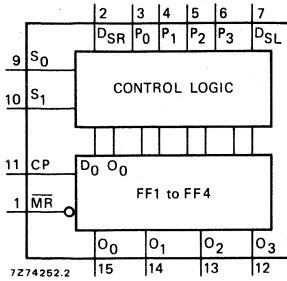
HEF40193B



4-bit up/down binary counter.

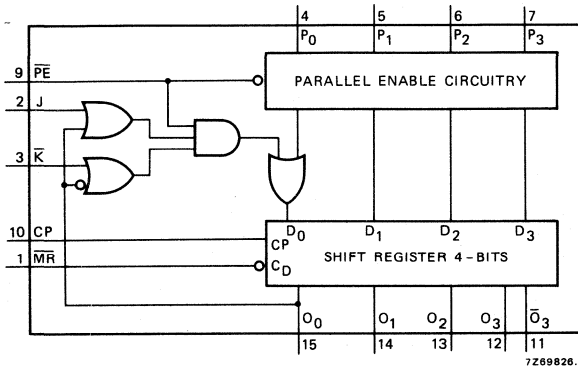
FUNCTIONAL DIAGRAMS

HEF40194B



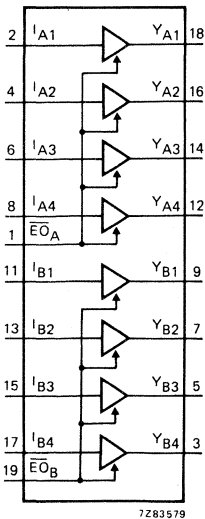
4-bit bidirectional universal shift register.

HEF40195B



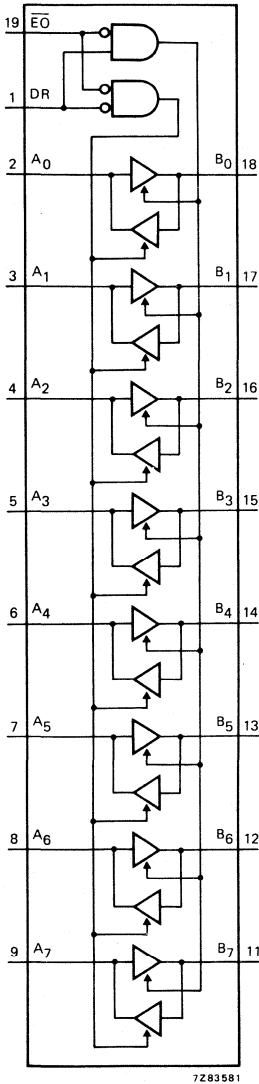
4-bit universal shift register.

HEF40244B



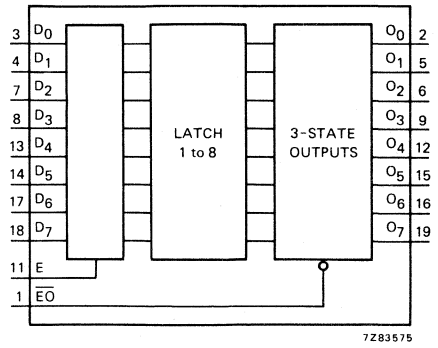
Octal buffers with 3-state outputs.

HEF40245B



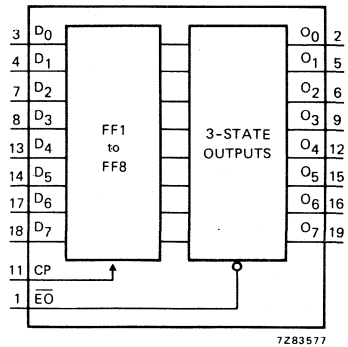
Octal bus transceiver with
3-state outputs.

HEF40373B



Octal transparent latch with 3-state outputs.

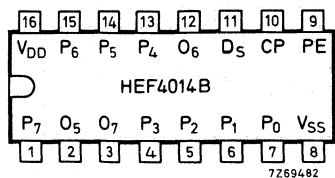
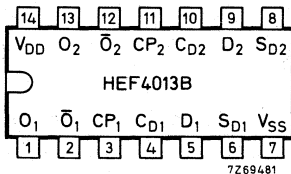
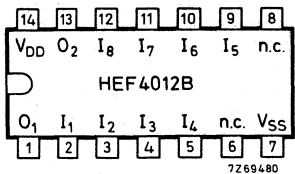
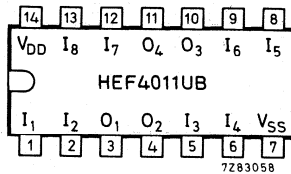
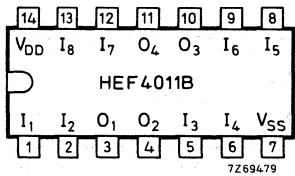
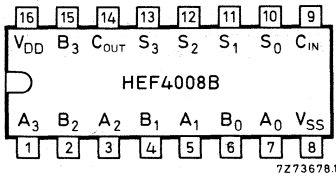
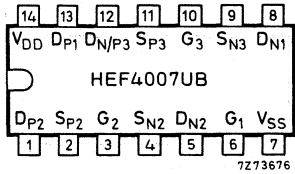
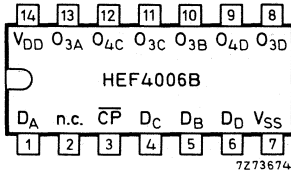
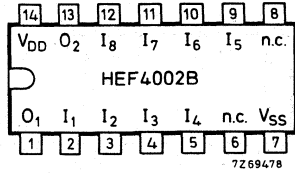
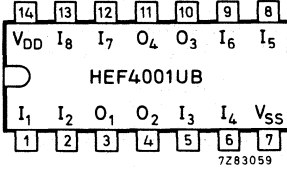
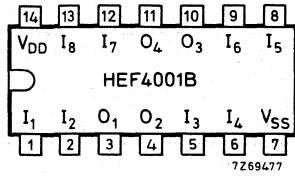
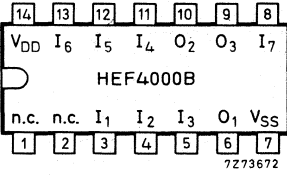
HEF40374B



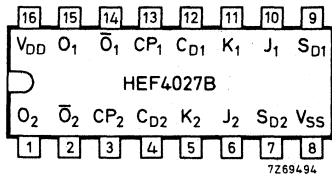
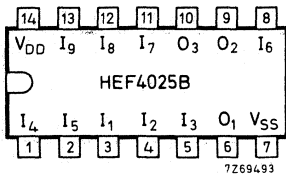
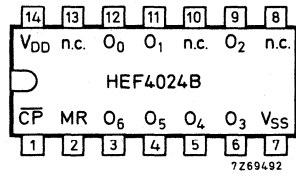
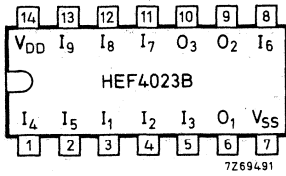
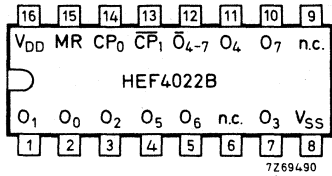
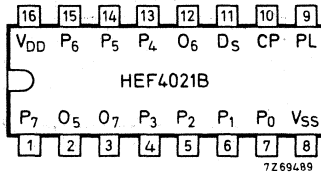
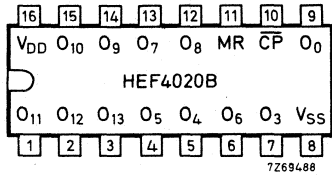
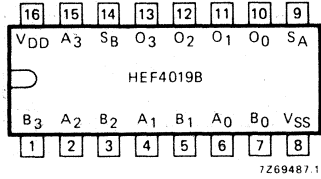
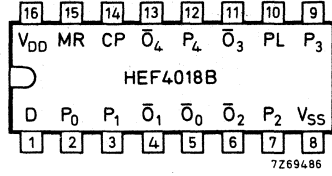
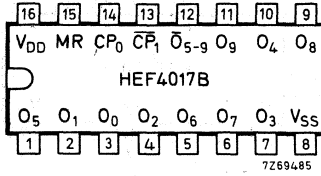
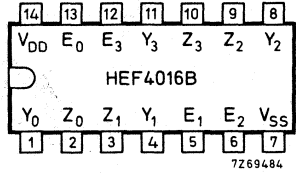
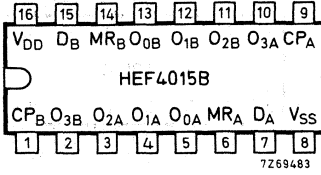
Octal D-type flip-flop with 3-state outputs.

PIN DESIGNATIONS

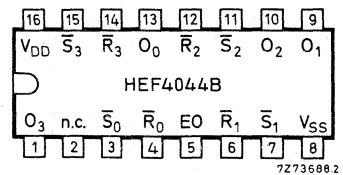
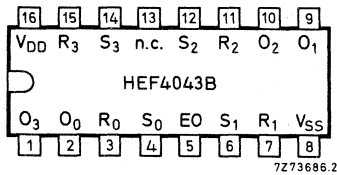
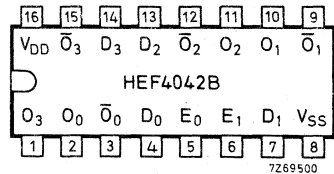
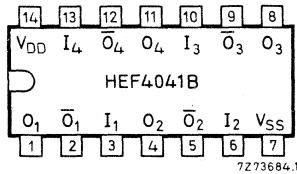
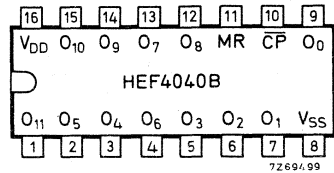
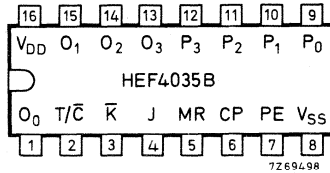
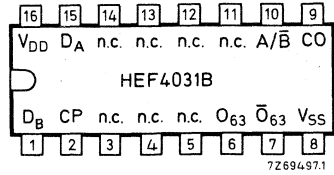
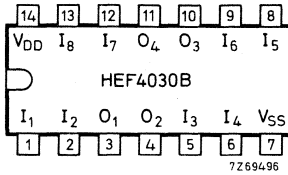
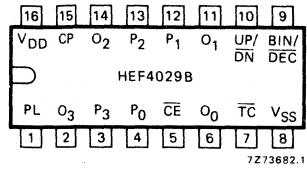




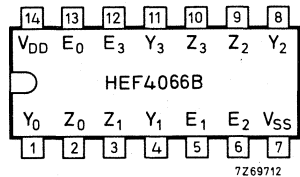
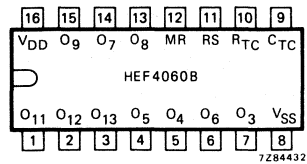
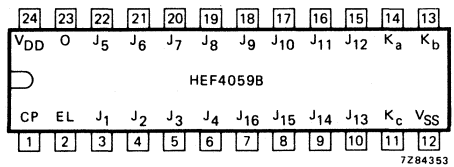
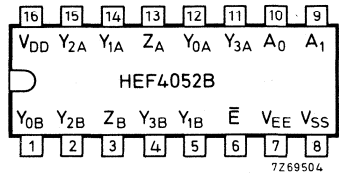
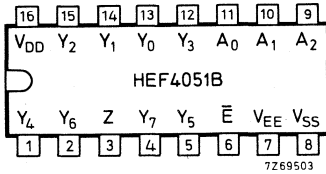
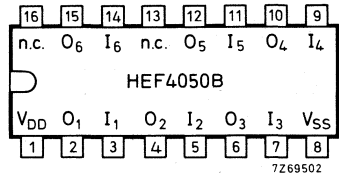
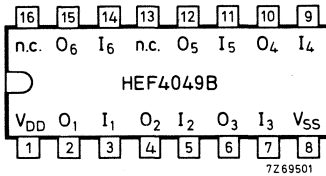
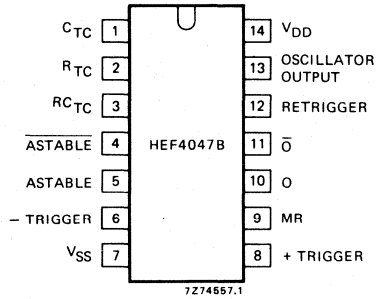
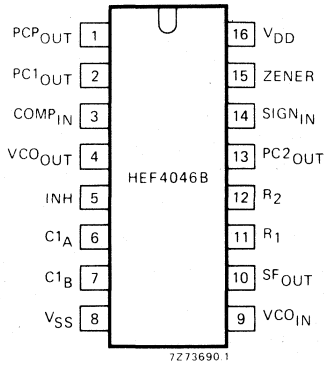
PIN DESIGNATIONS



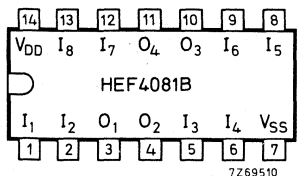
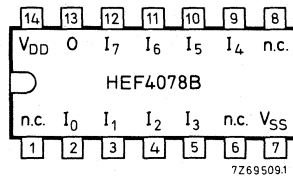
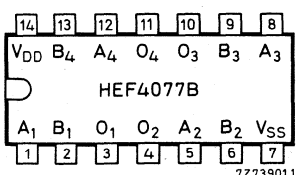
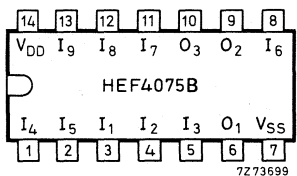
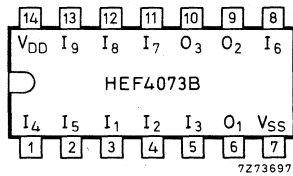
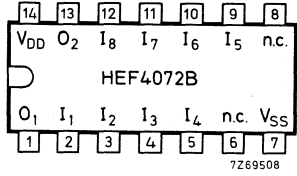
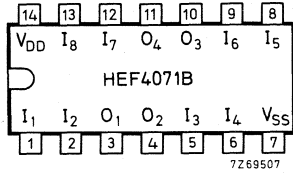
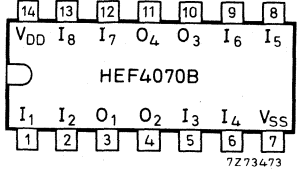
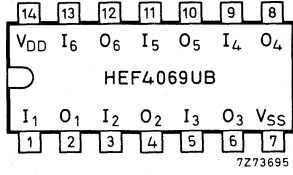
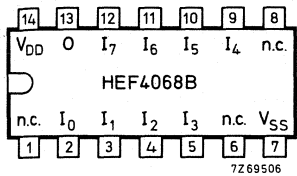
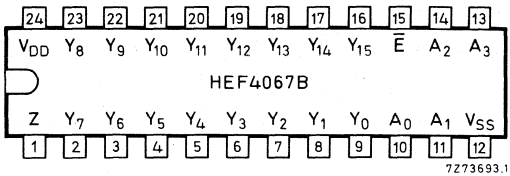
PIN DESIGNATIONS



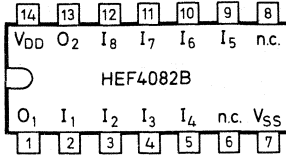
PIN DESIGNATIONS



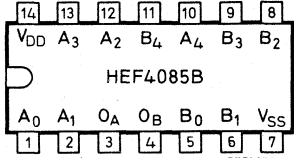
PIN DESIGNATIONS



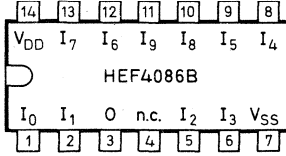
PIN DESIGNATIONS



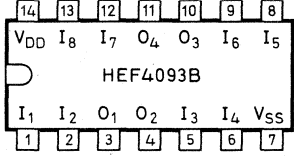
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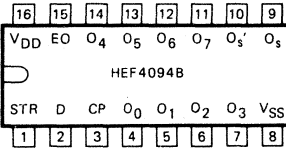
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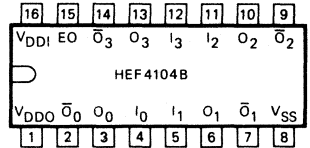
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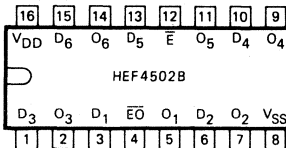
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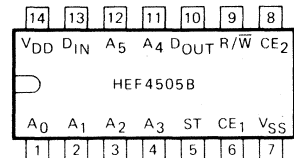
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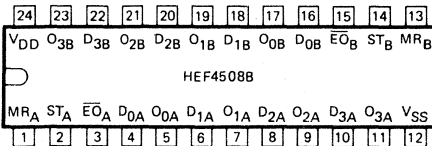
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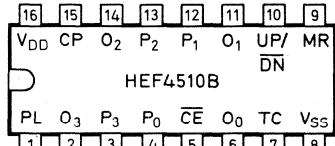
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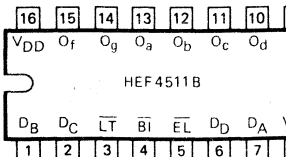
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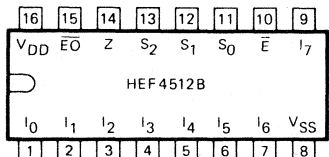
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7273713

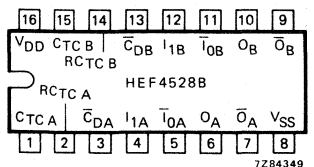
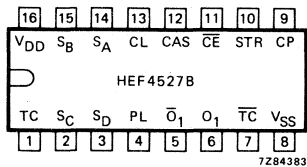
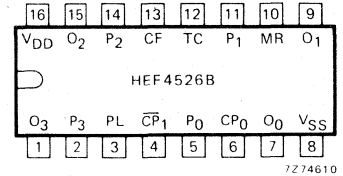
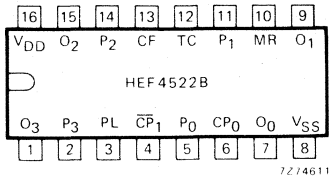
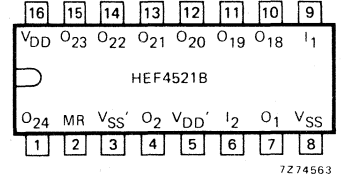
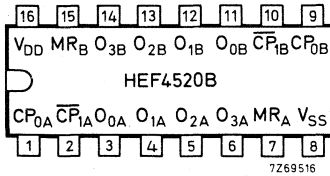
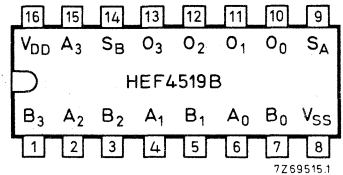
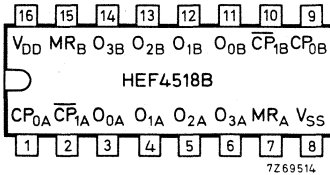
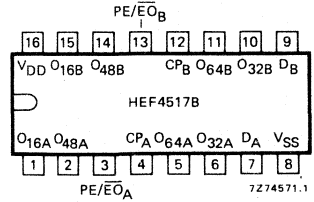
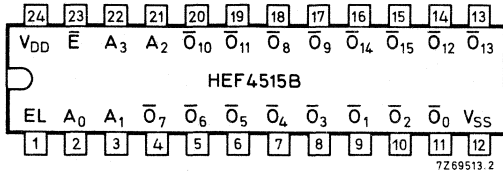
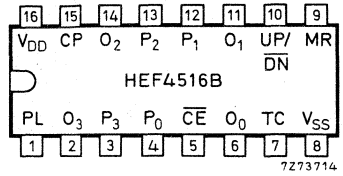
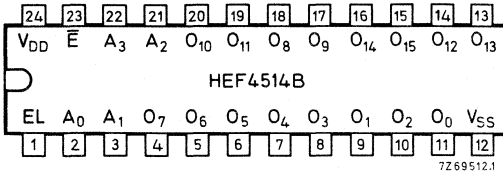


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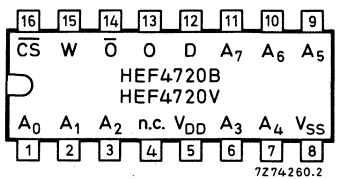
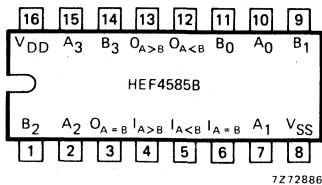
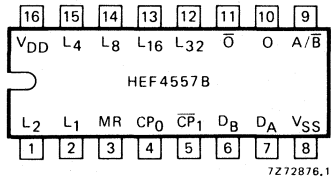
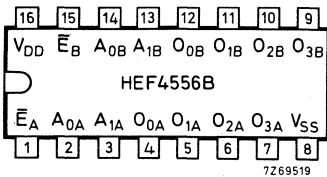
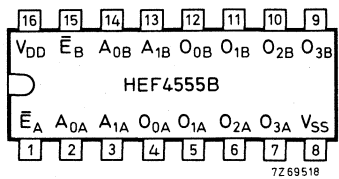
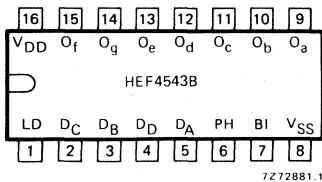
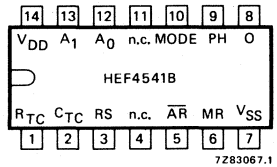
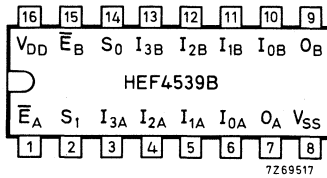
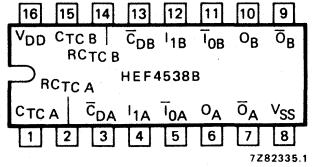
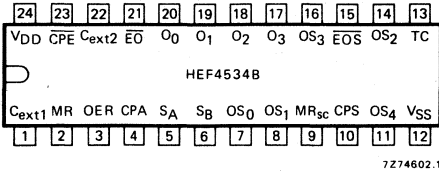
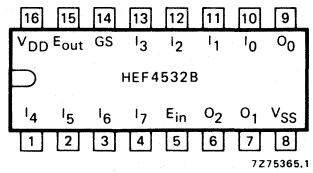
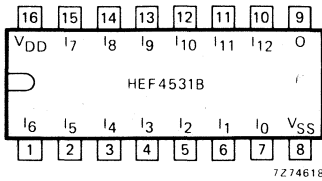


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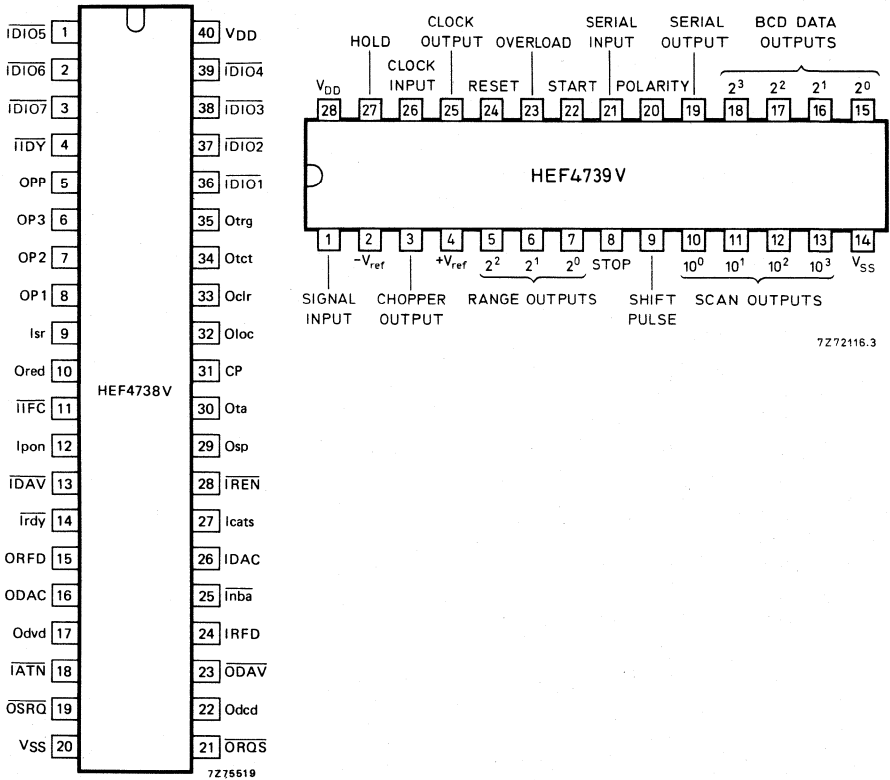
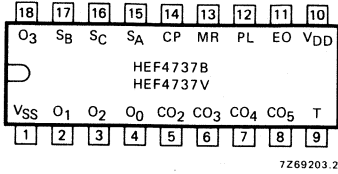
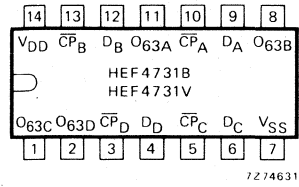
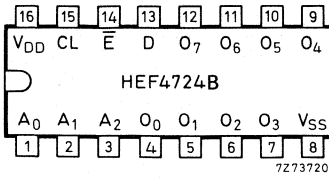
PIN DESIGNATIONS



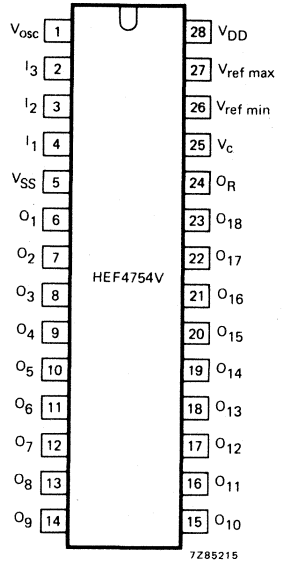
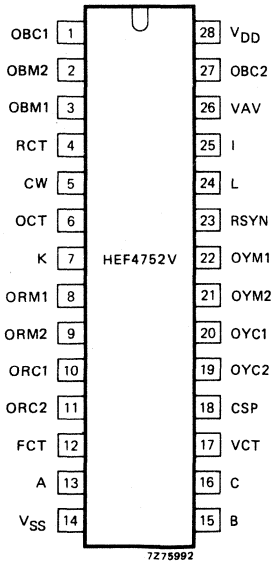
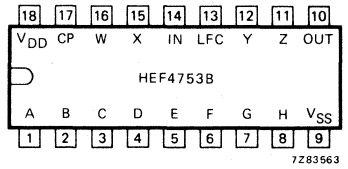
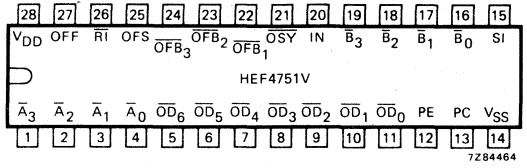
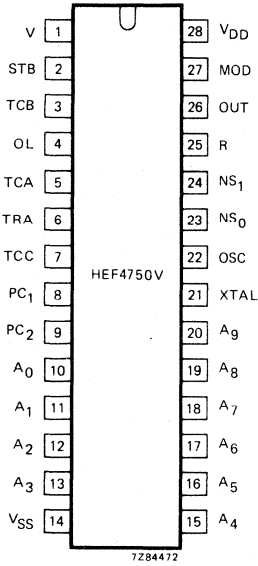
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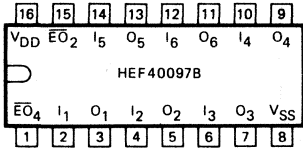
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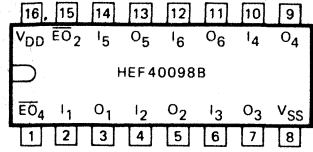
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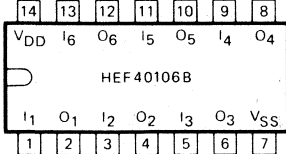
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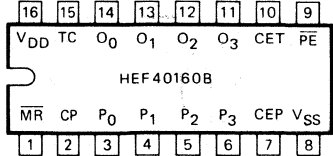
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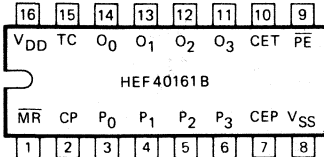
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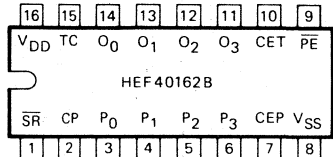
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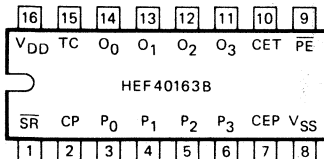
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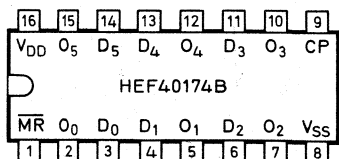
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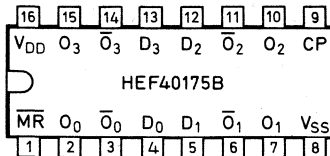
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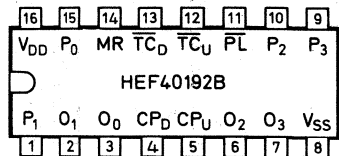
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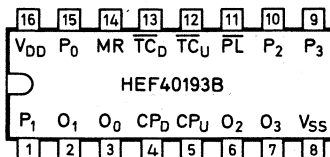
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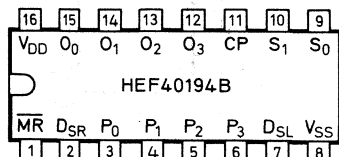
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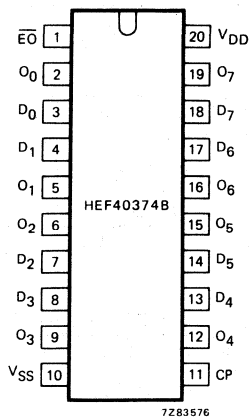
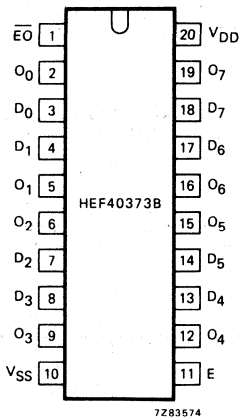
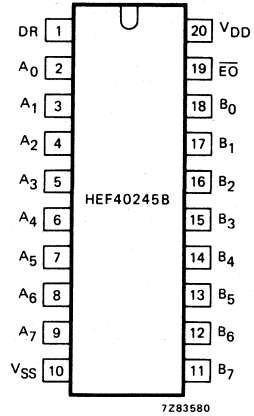
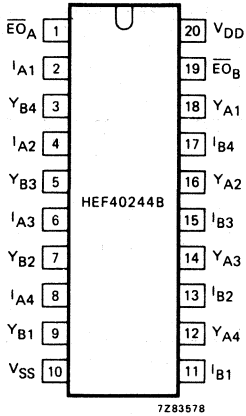
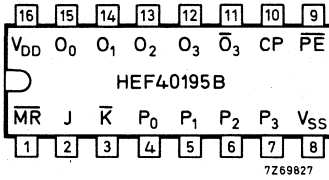


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PIN DESIGNATIONS



HE4000B FAMILY - INTRODUCTION



INTRODUCTION TO THE HE4000B FAMILY DATA SHEETS

The LOCMOS HE4000B range is a fully buffered digital integrated circuit family which meets the Jedec-B specification. The members of this family are pin-compatible with the well-known C-MOS 4000 and 14500 ranges. The HE family has the same advantages as conventional C-MOS circuits, plus the additional LOCMOS advantages.

LOCMOS means: Local Oxidation Complementary MOS.

The main effect of LOCMOS is a considerable reduction in the chip area required for a given function. Also important is the reduction in stray capacitance due to the smaller contact areas - hence the higher switching speed. Another benefit, brought about by the manufacturing process, is the self-alignment of the source and drain diffusions. This means that tolerance margins in the diffusions are unnecessary, thus further reducing the stray capacitances.

Advantages of C-MOS:

- low power dissipation - typically 10 nW per gate (static);
- wide operating supply voltage range;
- wide operating temperature range - -40 to $+85$ °C;
- high d.c. fan-out;
- inputs and outputs are protected against electrostatic voltages.

In addition to these, the LOCMOS HE4000B range has:

- buffered outputs on all circuits;
- higher speed;
- higher packing density - essential for MSI/LSI;
- excellent noise immunity.

The HE family is designed with standardized output drive characteristics which, combined with relative insensitivity to output capacitance loading, simplify system design.

Note

On page 1 of most of the device data sheets are shown a pinning diagram together with a functional diagram. In addition to this functional diagram, a more detailed logic diagram is given, which also shows the buffered outputs.

BUFFERED OUTPUTS

To minimize any pattern sensitivity of propagation delay, and to standardize delay and output drive, all HE family devices have an output buffer stage (see Fig. 1). Buffering improves the static noise immunity because the increased voltage gain gives nearly ideal transfer characteristics and the low output impedance gives significant improvement of the dynamic noise immunity. Significant pulse shaping is obtained because output transitions are virtually independent of input rise and fall times.

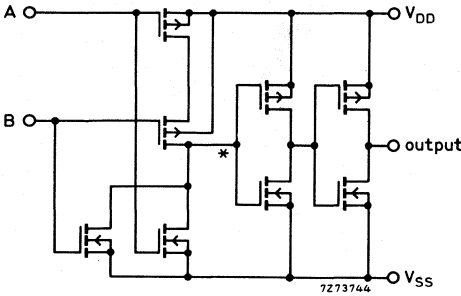


Fig. 1 Two-input NOR gate with fully buffered output; a typical LOCMOS circuit. In an unbuffered device the output would be taken from the point marked*.

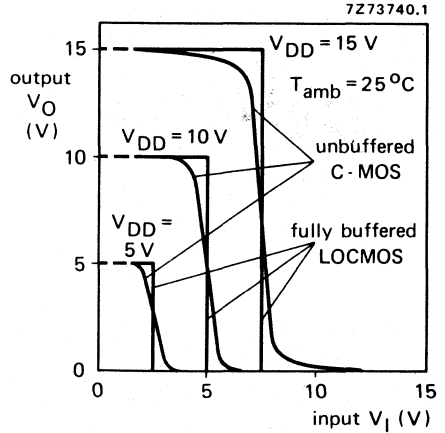
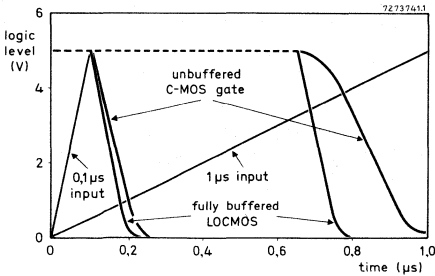
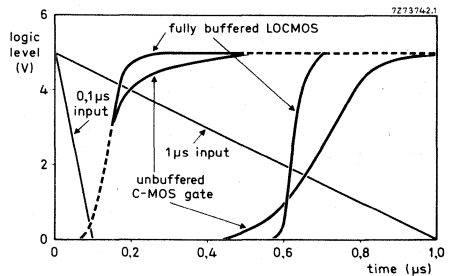


Fig. 2 Typical transfer characteristic showing improvement in buffered LOCMOS device as compared with unbuffered C-MOS device.



(a)



(b)

Fig. 3 The two graphs show how the output transitions are independent of input rise time (a) and fall time (b).

DESIGN CONSIDERATIONS

General

Local Oxidation Complementary MOS digital integrated circuits of SSI and MSI complexity have been hailed as the ideal logic family. A few LOCMOS devices, such as bidirectional analogue switches, exploit the unique feature of C-MOS technology; some take advantage of the smaller device size and higher potential packing density to achieve true LSI complexity, and perform logic functions that have been available in TTL for many years. Therefore, it is both helpful and practical to compare the performance of LOCMOS with that of the more familiar TTL (see table below).

LOCMOS speed is about three to six times lower than TTL or low-power Schottky (LS-TTL). Static noise immunity and fan-out are almost ideal, supply voltage is non-critical, and the quiescent power consumption is close to zero — several orders of magnitude lower than for any competing technology. For dynamic noise immunity, see NOISE IMMUNITY.

	standard TTL	low-power Schottky	4000 LOCMOS 5 V	4000 LOCMOS 10 V	4000 LOCMOS 15 V
propagation delay $C_L = 15 \text{ pF}$	10 ns	10 ns	40 ns	20 ns	15 ns
flip-flop clock frequency	35 MHz	45 MHz	8 MHz	16 MHz	20 MHz
quiescent power	10 mW	2 mW	10 nW	10 nW	10 nW
noise immunity	1 V	0,8 V	2,25 V	4,5 V	6,75 V
fan-out	10	10	50 *	50 *	50 *

* Or as determined by permissible propagation delay.

Supply voltage range

LOCMOS is guaranteed to function over the unprecedented range of 3 to 15 V supply voltage. Characteristics are guaranteed for 5, 10 and 15 V operation and can be extrapolated for any voltage in between. Operation below 4,5 V is not very meaningful because of the increase in delay (loss of speed), the increase in output impedance and the loss of noise immunity. Operation above 15 V is not recommended because of high dynamic power consumption and risk of noise spikes on the power supply exceeding the breakdown voltage (typ. > 20 V), causing SCR-latch-up and destroying the device unless the current is externally limited.

The lower limit of power supply voltage, including ripple, is determined by the required noise immunity, propagation delay or interface to TTL. The upper limit of supply voltage, including ripple and transients, is determined by power dissipation or direct interface to other logic. The HEF4049B, HEF4050B and HEF4104B provide level transition between TTL and LOCMOS when LOCMOS supply voltages over 5 V are used.

Low static power consumption combined with wide supply voltage range make LOCMOS the ideal logic family for battery-operated equipment.

Power consumption

Under static conditions, the p-channel and the n-channel transistors are not conducting simultaneously, thus only leakage current flows from the positive (V_{DD}) to the negative (V_{SS}) supply connection. This leakage current is typically 0,5 nA per gate, resulting in a very attractive low power consumption of 2,5 nW per gate (at 5 V).

Whenever a LOC MOS circuit is exercised, when data or clock inputs change, additional power is consumed to charge and discharge capacitances (on-chip parasitic capacitances as well as load capacitances). Moreover, there is a short time during the transition when both the p-channel and n-channel transistors are partially conducting. This dynamic power consumption is obviously proportional to the frequency at which the circuit is exercised, to the load capacitance and to the square of the supply voltage.

As shown in Fig. 4, the power consumption of a LOC MOS gate exceeds that of a low-power Schottky gate somewhere between 500 kHz and 2 MHz of actual output frequency. Comparing the power consumption of more complex devices (MSI) in various technologies may show a different result.

In any complex design, only a small fraction of the gates actually switch at the full clock frequency, most gates operate at a much lower average rate and therefore consume much less power. A realistic comparison of power consumption between different technologies involves a thorough analysis of the average switching speed of each gate in the circuit.

The maximum values of the quiescent device current (I_{DD}) are given in the Family Specifications, the typical dynamic power dissipation is given in the individual data sheets. The total device power dissipation is the sum of the quiescent and dynamic power dissipation.

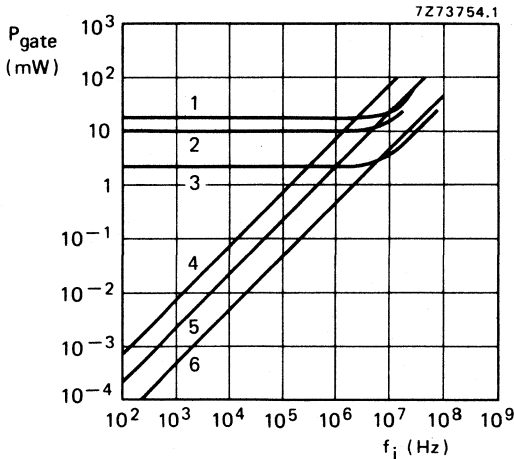


Fig. 4 Typical power dissipation per gate as a function of input frequency for several logic families.

- 1 Schottky TTL
- 2 Standard TTL
- 3 Low-power Schottky
- 4 LOC MOS ($V_{DD} = 15\text{ V}$)
- 5 LOC MOS ($V_{DD} = 10\text{ V}$)
- 6 LOC MOS ($V_{DD} = 5\text{ V}$)

Additional power consumption (due to slow input rise and fall times)

As long as the input voltage of a LOC MOS circuit is below the N-transistor threshold voltage, or higher than the supply voltage minus the P-transistor threshold voltage, one of the input transistors is always in the OFF-state and no 'through' current flows in the input stage.

When the input voltage equals the N-transistor threshold voltage (typ. 1.5 V), the N-transistor starts conducting and a drain current starts to flow.

Figure 5 shows the drain current as a function of the input voltage for a typical LOC MOS input.

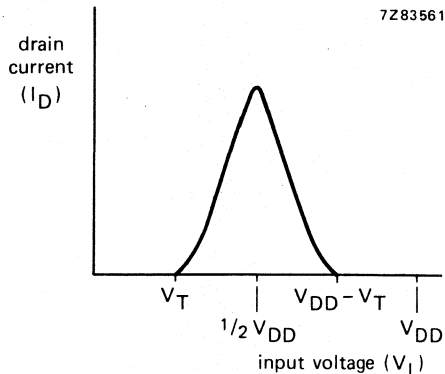


Fig. 5 Drain current as a function of input voltage.

This drain current reaches a maximum at $1/2 V_{DD}$ and the peak value depends on the geometrics of the transistors used. This current is proportional to V_{DD}^n , in which $n > 2$.

For Schmitt triggers, unbuffered types, and circuits comprising a single stage inverter, typical current transfer characteristics are given in the device data sheets.

When squaring up slow pulses by means of Schmitt triggers, the through current gives additional power consumption.

By applying RC-oscillators, or oscillators constructed with Schmitt triggers, the phenomenon described gives a frequency-independent power consumption.

Propagation delay

Compared to TTL and LS-TTL, all C-MOS devices are slow and very sensitive to capacitance loading (see Fig. 6).

The HE family uses both advanced processing (LOCMOS) and improved circuit design (buffered gates) to achieve propagation delays and output transition times that are superior to any other junction-isolated C-MOS design.

LOCMOS processing achieves lower parasitic capacitances which reduce the on-chip delay and increase the maximum clock frequency of flip-flops, registers and counters. Buffering all outputs, even on gates, results in lower output impedance and thus reduces the effect of capacitive loading.

Propagation delay is affected by three parameters: capacitive loading, supply voltage, and temperature.

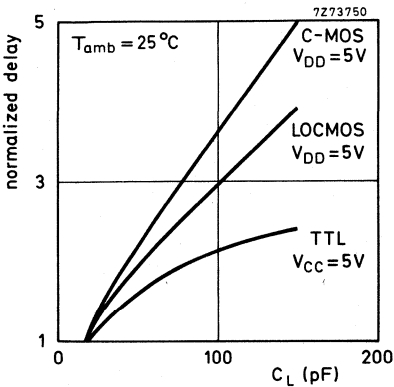


Fig. 6 Normalized propagation delay as a function of load capacitance for TTL, C-MOS and LOCMOS.

Capacitive loading effect

Historically, semiconductor manufacturers have always specified the propagation delay at an output load of 15 pF, not because this was considered a representative systems environment, but rather because it was the lowest practical test-jig capacitance. It also generated the most impressive specifications. For example, TTL with an output impedance in the LOW state of typically 25Ω is little affected by an increase in capacitive loading. LOCMOS, however, with an output impedance of typically 250Ω (at 5 V) is 10 times more sensitive to capacitive loading. As an example Fig. 7 shows the positive and negative-going delays as functions of load capacitance for the HEF4011B and Fig. 8 shows the output transition times for standard output stages. For detailed information see Family Specifications and the individual data sheets. It should be noted that most unbuffered gates have an even higher output impedance, a larger dependence on output loading, and do not show the same symmetry.

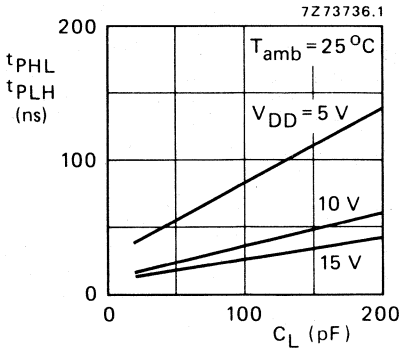


Fig. 7 Positive and negative-going propagation delay as functions of load capacitance for the HEF4011B.

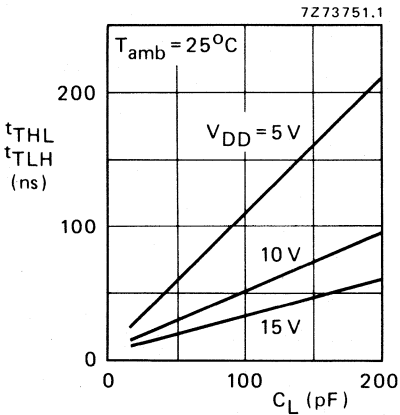


Fig. 8 Output transition times as functions of load capacitance.

Supply voltage effect.

1. Speed; Fig. 9 shows propagation delays as functions of supply voltage. The best choice for slow applications is 5 V. For reasonably fast systems, choose 10 or 12 V. Any application requiring 15 V to achieve short delays and fast operation should be investigated for excessive power dissipation and should be weighed against an LS-TTL approach.
2. Noise immunity; improves with higher supply voltage (see NOISE IMMUNITY).

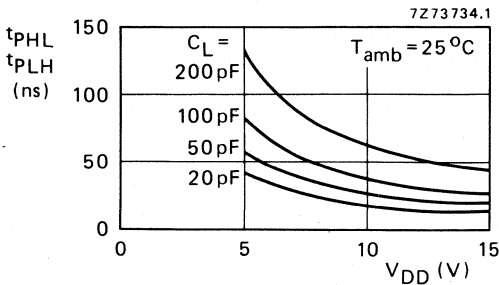


Fig. 9 Propagation delays (symmetrical) as functions of power supply voltage for the HEF4011B.

Temperature effect

The temperature dependence of LOC MOS is much simpler than with TTL, where three factors contribute: increase of beta with temperature, increase of resistor value with temperature, and decrease of junction forward voltage drop with increasing temperature. In LOC MOS, essentially only the carrier mobility changes, thus increasing the impedance, and hence the delay, with temperature. For more details see Family Specifications and the individual data sheets, for example see Fig. 10.

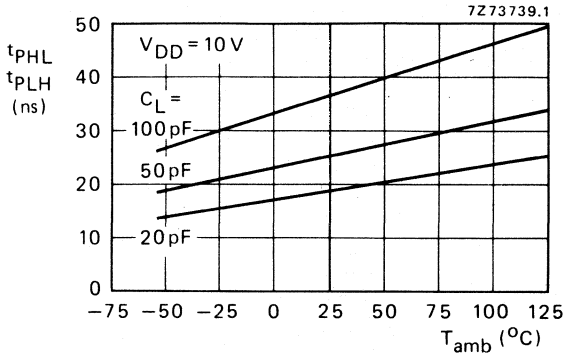


Fig. 10 Propagation delays as functions of ambient temperature, with $V_{DD} = 10$ V for HEF4011B.

Noise immunity

One of the most advertised and also misunderstood C-MOS features is noise immunity. The input threshold of a C-MOS gate is approximately 50% of the supply voltage and the voltage transfer curve is almost ideal. As a result, LOC MOS can claim very good voltage noise immunity, typically 45% of the supply voltage, i.e., 2,25 V in a 5 V system, 4,5 V in a 10 V system and 6,75 V in a 15 V system. Compare this with the TTL transfer curve in Fig. 11 and its resultant 1 V noise immunity in a lightly loaded system and only 0,4 V worst case. Fig. 12 shows the transfer characteristic between -55 and $+125$ °C.

Since LOC MOS output impedance, output voltage and input threshold are symmetrical with respect to the supply voltage, the LOW and HIGH level noise immunities are practically equal. Therefore, a LOC MOS system can tolerate ground or V_{DD} drops and noise on these supply lines of more than 1 V, even in a 5 V system. Moreover, the inherent LOC MOS delays act as a noise filter; 10 ns spikes tend to disappear in a chain of LOC MOS gates, but are amplified in a chain of TTL gates. Because of these features, LOC MOS is very popular with designers of industrial control equipment that must operate in an electrically and electromagnetically 'polluted' environment.

Unfortunately these impressive noise margin specifications disregard one important fact: the output impedance of LOC MOS is 3 to 10 times higher than that of TTL. C-MOS interconnections are therefore less 'stiff' and more susceptible to capacitively coupled noise. In terms of such current-injected crosstalk from high noise voltages through small coupling capacitances, the tables on the next page give a comparison between LOC MOS and TTL/LS-TTL.

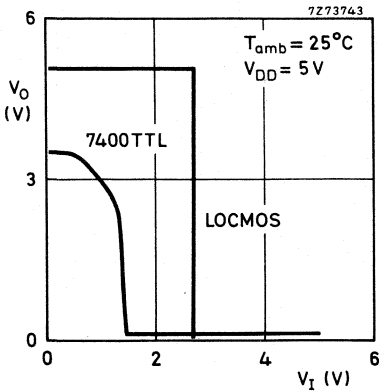


Fig. 11 Typical transfer characteristic for TTL and LOCMOS.

LOCMOS/TTL (normalized to TTL)

V_{DD}	5 V	10 V	15 V
factor	0,5	1	2

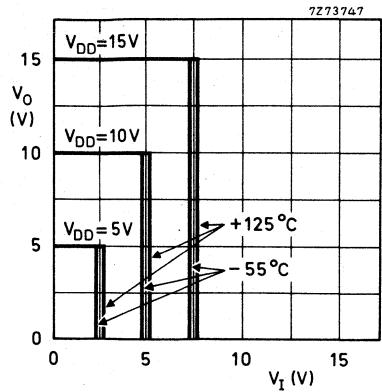


Fig. 12 Voltage transfer characteristic over -55 to $+125$ °C range.

LOCMOS/LS-TTL (normalized to LS-TTL)

V_{DD}	5 V	10 V	15 V
factor	1	3	5

From the tables can be seen that LOCMOS operating at $V_{DD} = 10$ V has a dynamic noise immunity which is comparable with TTL and 3 times as good as LS-TTL.

In terms of voltage injected noise the nearly ideal transfer characteristic and the relatively slow response of LOCMOS circuits make them at least 5 times less sensitive to magnetically coupled noise than TTL/LS-TTL.

Input protection

The gate input to any MOS transistor appears like a small value (< 1 pF), very low leakage (< 1 pA) capacitor. Without special precautions, such inputs could be electrostatically charged to a high voltage, causing a destructive breakdown of the dielectric and permanently damaging the device. Therefore, all LOCMOS inputs are protected by a combination of series resistor and shunt diodes. Different manufacturers have different approaches; some use a single diode, others use two diodes, and some use a resistor with a parasitic substrate diode.

With the exception of a few devices, each member of the HE family utilizes a series resistor, nominally 400Ω , and two diodes, one to V_{DD} , and the other to V_{SS} (see Fig. 13). The resistor is a polysilicon 'true resistor' without a parasitic substrate diode. This ensures that the input impedance is always at least 400Ω under all biasing conditions, even when V_{DD} is short-circuited to V_{SS} . A parasitic substrate diode would represent a poorly defined shunt to V_{SS} in this particular case.

The diodes exhibit typical forward voltage drops of 0.9 V at 1 mA and reverse breakdown voltages of 20 V. For certain special applications such as oscillators, the diodes actually conduct during normal operation, in this case the current should be limited to 1 mA. Input currents averaging 10 mA or more may destroy the device.

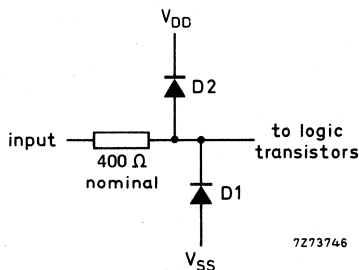


Fig. 13 Standard HE family LOCMOS input protection circuit.

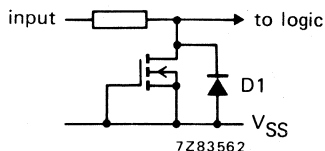


Fig. 14 The input protection for the HEF4049B and HEF4050B.

Figure 14 shows the input protection for the types HEF4049B and HEF4050B. Diode D1 is the inherent drain to V_{SS} diode of the protection device. Under operational conditions, this input may exceed the supply voltage V_{DD} .

Power supply regulation and decoupling

The LOCMOS technology suggests that any supply voltage between 3 and 15 V will do, thus rendering supply voltage regulation unnecessary. However, it must be realized that the supply voltage has influence on the system speed (see Fig. 9), noise immunity (see Figs 11 and 12) and dissipation (see Fig. 4) and see text concerning all these Figures.

Any dynamic system generates voltage spikes on the supply line. These spikes influence the noise immunity, they may damage the circuit, or may have a negative influence on proper operation of the circuit. Therefore a matched decoupling of the supply line is necessary. Generally an electrolytic capacitor of $3 \mu\text{F}$ per 10 devices is sufficient. However, some circuits require special attention:

1. HEF4511B: BCD to 7-segment latch/decoder/driver; an electrolytic capacitor of $3 \mu\text{F}$ should be added to each device to avoid excessive voltage spikes due to high di/dt .
2. HEF4528B: dual retriggerable/resettable monostable multivibrator; for circuits of this nature it is recommended to use proper decoupling to avoid pulse length variations due to supply line ripple.
3. Circuits that operate in the linear mode, such as RC or crystal oscillators, a minimum supply voltage of at least 4 V is recommended.

3-state outputs

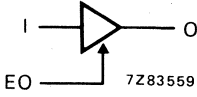


Fig. 15 Logic symbol of a 3-state output.

Function table

inputs		output
I	EO	O
X	L	Z
L	H	L
H	H	H

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

X = state is immaterial

Z = high impedance OFF-state

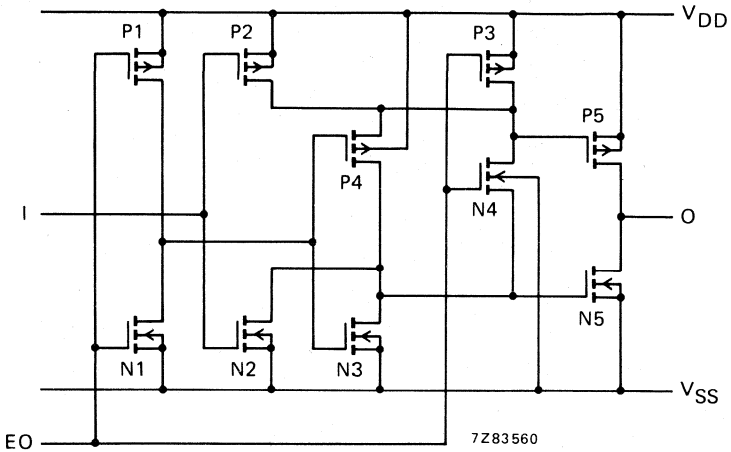


Fig. 16 Circuit diagram of 3-state output.

When EO is HIGH, the output is enabled and the transistors P4 and N4 act as a transmission gate, and they connect the gates of the output transistors together. A LOW level at EO puts the output in the high impedance OFF-state; transistors P3 and N3 function as pull-up and pull-down transistors respectively.

FAMILY SPECIFICATIONS



These specifications cover the common electrical characteristics of the entire HE4000B family, unless otherwise specified in the individual device data sheet.

The LOCMOS HE4000B family devices will operate over a recommended V_{DD} power supply range of 3 to 15 V, as referenced to V_{SS} (usually ground). Parametric limits are guaranteed for V_{DD} of 5, 10 and 15 V. Because of the wide operating voltage range, power supply regulation is less critical than with other types of logic. The lower limit of the supply voltage is 3 V, or as determined by required system speed and/or noise immunity or interface to other logic. The recommended upper limit is 15 V or as determined by power dissipation constraints or interface to other logic. Unused inputs must be connected to V_{DD} , V_{SS} or another input. Inputs and outputs are protected against electrostatic effects in a wide variety of device-handling situations. However, to be totally safe, it is desirable to take handling precautions into account.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{DD}	-0,5 to + 18 V
Voltage on any input	V_I	-0,5 to $V_{DD} + 0,5$ V
D.C. current into any input or output	$\pm I$	max. 10 mA
Power dissipation per package (for plastic and ceramic DIL) for $T_{amb} = -40$ to + 60 °C	P_{tot}	max. 400 mW
for $T_{amb} = + 60$ to + 85 °C		derate linearly with 8 mW/°C to 200 mW
Power dissipation per package (for plastic flat pack) for $T_{amb} = -40$ to + 70 °C	P_{tot}	max. 200 mW
for $T_{amb} = + 70$ to + 85 °C		derate linearly with 5 mW/°C to 125 mW
Power dissipation per output	P	max. 100 mW
Storage temperature	T_{stg}	-65 to + 150 °C
Operating ambient temperature	T_{amb}	-40 to + 85 °C

FAMILY SPECIFICATIONS

D.C. CHARACTERISTICS $V_{SS} = 0\text{ V}$; for all devices unless otherwise specified

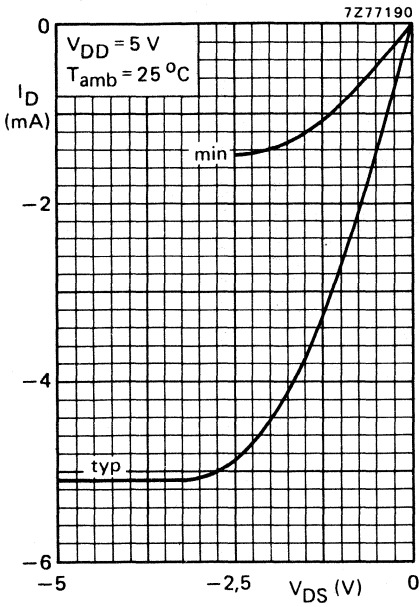
parameter	V_{DD} V	symbol	T_{amb} (°C)			unit	conditions
			-40 min.	+25 min.	+85 max.		
Quiescent device current							
gates	5	I_{DD}	1,0	1,0	7,5	μA	all valid input combinations; $V_I = V_{SS}$ or V_{DD}
	10		2,0	2,0	15,0	μA	
	15		4,0	4,0	30,0	μA	
buffers, flip-flops	5	I_{DD}	4,0	4,0	30	μA	
	10		8,0	8,0	60	μA	
	15		16,0	16,0	120	μA	
MSI	5	I_{DD}	20	20	150	μA	
	10		40	40	300	μA	
	15		80	80	600	μA	
LSI	5	I_{DD}	50	50	375	μA	
	10		100	100	750	μA	
	15		200	200	1500	μA	
Output voltage LOW	5	VOL	0,05	0,05	0,05	V	$V_I = V_{SS}$ or V_{DD} ; $ I_O < 1\ \mu\text{A}$
	10		0,05	0,05	0,05	V	
	15		0,05	0,05	0,05	V	
Output voltage HIGH	5	VOH	4,95	4,95	4,95	V	$V_I = V_{SS}$ or V_{DD} ; $ I_O < 1\ \mu\text{A}$
	10		9,95	9,95	9,95	V	
	15		14,95	14,95	14,95	V	
Input voltage LOW (buffered stages only)	5	V _{IL}	1,5	1,5	1,5	V	$V_O = 0,5\text{ V or }4,5\text{ V}$ $V_O = 1,0\text{ V or }9,0\text{ V}$ $V_O = 1,5\text{ V or }13,5\text{ V}$
	10		3,0	3,0	3,0	V	
	15		4,0	4,0	4,0	V	
Input voltage HIGH (buffered stages only)	5	V _{IH}	3,5	3,5	3,5	V	$V_O = 0,5\text{ V or }4,5\text{ V}$ $V_O = 1,0\text{ V or }9,0\text{ V}$ $V_O = 1,5\text{ V or }13,5\text{ V}$
	10		7,0	7,0	7,0	V	
	15		11,0	11,0	11,0	V	

D.C. CHARACTERISTICS (continued) $V_{SS} = 0\text{ V}$; for all devices unless otherwise specified

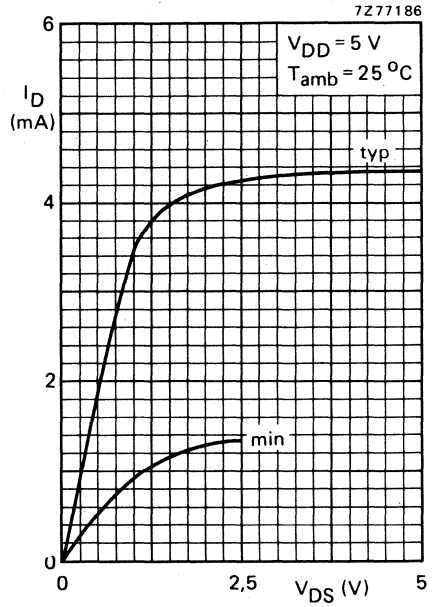
parameter	V_{DD} V	symbol	T_{amb} (°C)						unit	conditions
			-40		+25		+85			
			min.	max.	min.	max.	min.	max.		
Input voltage LOW (unbuffered stages only)	5	V_{IL}	1	1	—	1	—	V	$V_O = 0,5\text{ V or } 4,5\text{ V}$ $V_O = 1,0\text{ V or } 9,0\text{ V}$ $V_O = 1,5\text{ V or } 13,5\text{ V}$ $ I_O < 1\ \mu\text{A}$	
	10		2	2	—	2	—	V		
	15		2,5	2,5	—	2,5	—	V		
Input voltage HIGH (unbuffered stages only)	5	V_{IH}	4	4	4	4	4	V	$V_O = 0,5\text{ V or } 4,5\text{ V}$ $V_O = 1,0\text{ V or } 9,0\text{ V}$ $V_O = 1,5\text{ V or } 13,5\text{ V}$ $ I_O < 1\ \mu\text{A}$	
	10		8	8	8	8	8	V		
	15		12,5	12,5	12,5	12,5	12,5	V		
Output (sink) current LOW	5	I_{OL}	0,52	0,44	0,44	0,36	0,36	mA	$V_O = 0,4\text{ V}; V_I = 0\text{ or } 5\text{ V}$ $V_O = 0,5\text{ V}; V_I = 0\text{ or } 10\text{ V}$ $V_O = 1,5\text{ V}; V_I = 0\text{ or } 15\text{ V}$	
	10		1,3	1,1	0,9	0,9	0,9	mA		
	15		3,6	3,0	2,4	2,4	2,4	mA		
Output (source) current HIGH	5	$-I_{OH}$	0,52	0,44	0,44	0,36	0,36	mA	$V_O = 4,6\text{ V}; V_I = 0\text{ or } 5\text{ V}$ $V_O = 9,5\text{ V}; V_I = 0\text{ or } 10\text{ V}$ $V_O = 13,5\text{ V}; V_I = 0\text{ or } 15\text{ V}$	
	10		1,3	1,1	0,9	0,9	0,9	mA		
	15		3,6	3,0	2,4	2,4	2,4	mA		
Output (source) current HIGH	5	$-I_{OH}$	1,7	1,4	1,4	1,1	1,1	mA	$V_O = 2,5\text{ V}; V_I = 0\text{ or } 5\text{ V}$ $V_I = 0\text{ or } 15\text{ V}$	
	15		0,3	0,3	0,3	—	1,0	μA		
Input leakage current	15	$\pm I_{IN}$	—	0,3	—	0,3	—	μA	output returned to V_{DD}	
3-state output leakage current; HIGH	15	I_{OZH}	—	1,6	—	1,6	—	μA	output returned to V_{SS}	
3-state output leakage current; LOW	15	$-I_{OZL}$	—	1,6	—	1,6	—	μA		



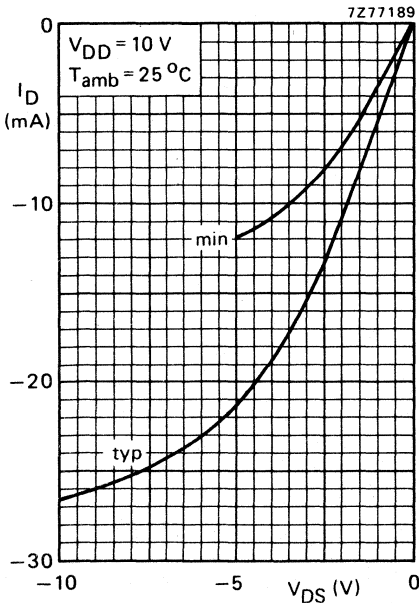
FAMILY SPECIFICATIONS



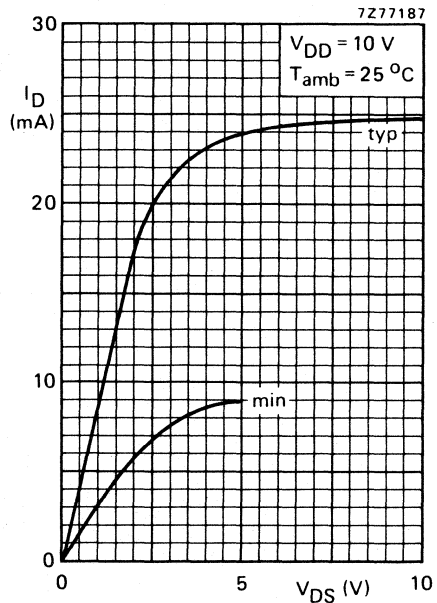
P-channel drain characteristics (source)



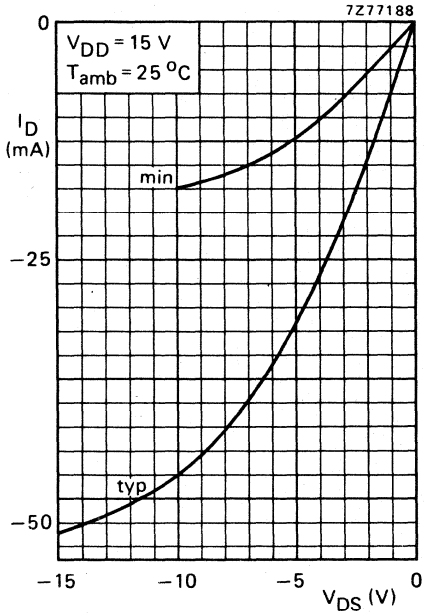
N-channel drain characteristics (sink)



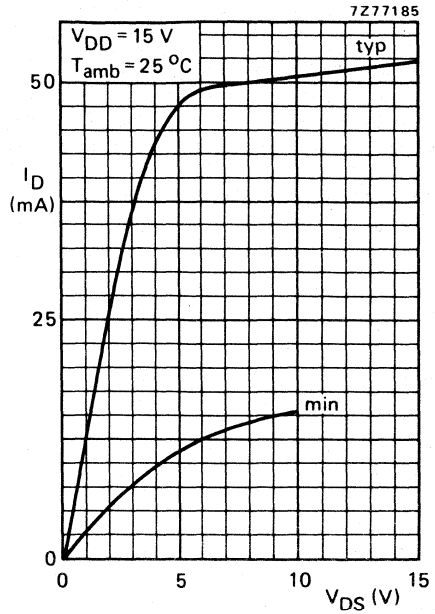
P-channel drain characteristics (source)



N-channel drain characteristics (sink)



P-channel drain characteristics (source)



N-channel drain characteristics (sink)

Note

Temperature coefficient: $-0,4\%/^{\circ}\text{C}$.



A.C. CHARACTERISTICS

Clock input rise and fall times (t_r , t_f)

The upper limits on t_r and t_f vary widely from device to device and with supply voltage. Unless otherwise specified in the individual data sheets it is recommended that input rise and fall times be less than 15 μ s for $V_{DD} = 5$ V; 4 μ s for $V_{DD} = 10$ V; 1 μ s for $V_{DD} = 15$ V.

Output transition times (t_{TLH} , t_{THL})

$V_{SS} = 0$ V; $T_{amb} = 25$ °C; $C_L = 50$ pF; input transition times ≤ 20 ns

	V_{DD} V	symbol	min.	typ.	max.	typical extrapolation formula	
Output transition times HIGH to LOW	5	t_{THL}		60	120	ns	10 ns + (1,0 ns/pF) C_L
	10		30	60	ns	9 ns + (0,42 ns/pF) C_L	
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L	
LOW to HIGH	5	t_{TLH}		60	120	ns	10 ns + (1,0 ns/pF) C_L
	10		30	60	ns	9 ns + (0,42 ns/pF) C_L	
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L	

Temperature coefficient (typical values)

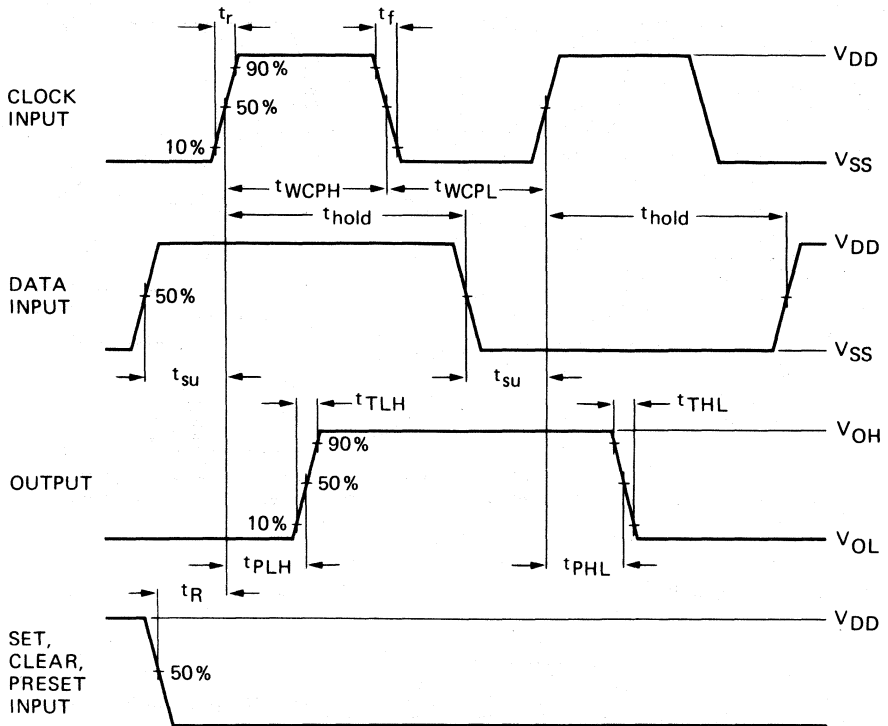
Propagation delays +0,35%/°C

Output transition times +0,35%/°C

Input capacitance (digital inputs)

Maximum input capacitance $C_I = 7,5$ pF.

Set-up times, hold times, recovery times and propagation delays for sequential logic circuits.



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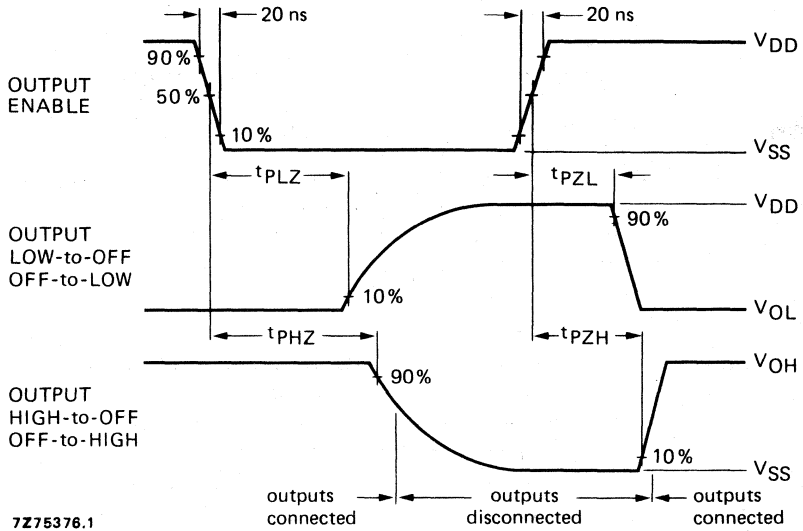
Note

In the waveforms above the active transition of the clock input is going from LOW to HIGH and the active level of the forcing signals (SET, CLEAR and PRESET) is HIGH.

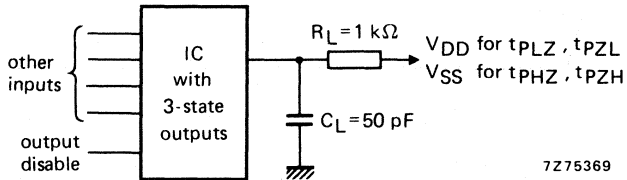
The actual direction of the active transition of the clock input and the actual active levels of the forcing signals are specified in the individual device data sheet.

FAMILY SPECIFICATIONS

Propagation delays of 3-state outputs.



Test circuit of 3-state output ICs.



DEFINITION OF SYMBOLS AND TERMS USED IN DATA SHEETS

Currents

Positive current is defined as conventional current flow into a device. Negative current is defined as conventional current flow out of a device.

- I_{IN} Input current; the current flowing into a device at specified input voltage and V_{DD} .
- I_{OH} Output current HIGH; the drive current flowing out of the device at specified HIGH output voltage and V_{DD} .
- I_{OL} Output current LOW; the drive current flowing into a device at specified LOW output voltage and V_{DD} .
- I_{DD} Quiescent power supply current; the current flowing into the V_{DD} lead at specified input and V_{DD} conditions.
- I_{OZ} Output OFF current; the leakage current flowing into or out of the output of a 3-state device in the OFF state when the output is connected to V_{DD} or V_{SS} .
- I_{IL} Input current LOW; the current flowing into a device at a specified LOW level input voltage and a specified V_{DD} .
- I_{IH} Input current HIGH; the current flowing into a device at a specified HIGH level input voltage and a specified V_{DD} .
- I_{DDL} Quiescent power supply current LOW; the current flowing into the V_{DD} lead with a specified LOW level input voltage on all inputs and specified V_{DD} conditions.
- I_{DDH} Quiescent power supply current HIGH; the current flowing into the V_{DD} lead with a specified HIGH level input voltage on all inputs and specified V_{DD} conditions.
- I_Z OFF state leakage current; the leakage current flowing into the output of a 3-state device in the OFF state at a specified output voltage and V_{DD} .

Voltages

All voltages are referenced to V_{SS} , which is the most negative potential applied to the device.

- V_{DD} Supply voltage; the most positive potential on the device.
- V_{SS} Supply voltage; for a device with a single negative power supply, the most negative power supply, used as the reference level for other voltages; typically ground.
- V_{EE} Supply voltage; one of two (V_{SS} and V_{EE}) negative power supplies. For a device with dual negative power supply, the most negative power supply as a reference level for other voltages.
- V_{IH} Input voltage HIGH; the range of input voltages that represents a logic HIGH level in the system.
- V_{IL} Input voltage LOW; the range of input voltages that represents a logic LOW level in the system.
- V_{OH} Output voltage HIGH; the range of voltages at an output terminal with specified output loading and supply voltage. Device inputs are conditioned to establish a HIGH level at the output.
- V_{OL} Output voltage LOW; the range of voltages at an output terminal with specified output loading and supply voltage. Device inputs are conditioned to establish a LOW level at the output.

Analogue terms

- R_{ON} ON resistance; the effective ON state resistance of an analogue transmission gate, at specified input voltage, output load and V_{DD} .
- ΔR_{ON} Δ ON resistance; the difference in effective ON resistance between any two transmission gates of an analogue device at specified input voltage, output load and V_{DD} .

A.C. switching parameters

f_i	Input frequency; for combinatorial logic devices the maximum number of inputs and outputs switching in accordance with the device truth table. For sequential logic devices the clock frequency using alternate HIGH and LOW for data input or using the toggle mode, whichever is applicable.
f_o	Output frequency; each output.
f_{max}	Clock frequency; clock input waveform should have a 50% duty cycle and be such as to cause the outputs to be switching from 10% V_{DD} to 90% V_{DD} in accordance with the device truth table.
t_r, t_f	Clock input rise and fall times; 10% to 90% value.
t_{PLH}	Propagation delay time; the time between the specified reference points, normally 50% points on the input and output waveforms, with the output changing from the defined LOW level to the defined HIGH level.
t_{PHL}	Propagation delay time; the time between the specified reference points, normally 50% points on the input and output waveforms, with the output changing from the defined HIGH level to the defined LOW level.
t_{TLH}	Transition time, LOW-to-HIGH; the time between two specified reference points on a waveform, normally 10% and 90% points, that is changing from LOW to HIGH.
t_{THL}	Transition time, HIGH-to-LOW; the time between two specified reference points on a waveform, normally 90% and 10% points, that is changing from HIGH to LOW.
t_W	Pulse width; the time between 50% amplitude points on the leading and trailing edges of pulse.
t_{hold}	Hold time; the interval immediately following the active transition of the timing pulse (usually the clock pulse) or following the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure their continued recognition. A negative hold time indicates that the correct logic level may be released prior to the timing pulse and still be recognized.
t_{su}	Set-up time; the interval immediately preceding the active transition of the timing pulse (usually the clock pulse) or preceding the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure their recognition. A negative set-up time indicates that the correct logic level may be initiated sometime after the active transition of the timing pulse and still be recognized.
t_{PHZ}	3-state output disable time, HIGH to Z; the time between the specified reference points, normally the 50% point on the output enable input voltage waveform and a point representing a 0,1 V_{OH} drop on the output voltage waveform of a 3-state device, with the output changing from the output HIGH level (V_{OH}) to a high impedance OFF-state.
t_{PLZ}	3-state output disable time, LOW to Z; the time between the specified reference points, normally the 50% point on the output enable input voltage waveform and a point representing a 0,1 ($V_{DD}-V_{OL}$) rise on the output voltage waveform of a 3-state device, with the output changing from the output LOW level (V_{OL}) to a high impedance OFF-state.
t_{PZH}	3-state output enable time, Z to HIGH; the time between the specified reference points, normally 50% point on the output enable input voltage waveform and a point representing 0,1 V_{OH} voltage rise on the output voltage waveform of a 3-state device, with the output changing from a high impedance OFF-state to the output HIGH level (V_{OH}).
t_{PZL}	3-state output enable time, Z to LOW; the time between the specified reference points, normally the 50% point on the output enable input voltage waveform and a point representing 0,1 ($V_{DD}-V_{OL}$) voltage drop on the output voltage waveform of a 3-state device, with the output changing from a high impedance OFF-state to the output LOW level (V_{OL}).
t_R	Recovery time; the time between the end of an overriding asynchronous input, typically a clear or reset input, and the earliest permissible beginning of a synchronous control input, typically a clock input, normally measured at 50% points on both input voltage waveforms.

DEVICE DATA



DUAL 3-INPUT NOR GATE AND INVERTER



The HEF4000B provides the positive dual 3-input NOR function. A single stage inverting function with standard output performance is also accomplished. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

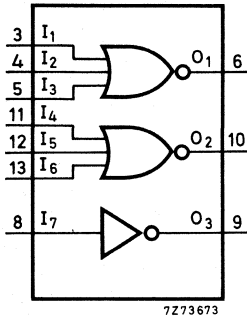


Fig. 1 Functional diagram.

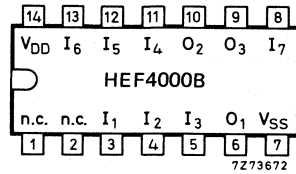


Fig. 2 Pinning diagram.

HEF4000BP: 14-lead DIL; plastic (SOT-27S, T, V).
 HEF4000BD: 14-lead DIL; ceramic (SOT-73).
 HEF4000BT: 14-lead flat pack; plastic (SO-14; SOT-108A).

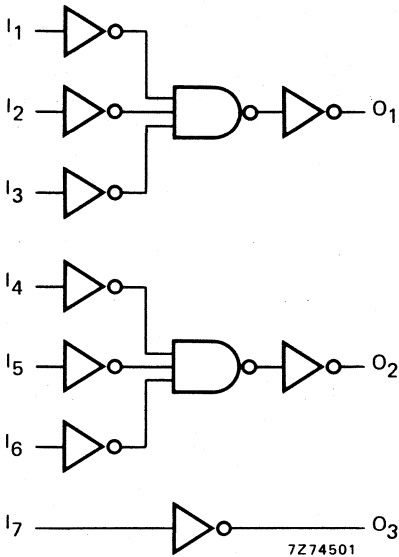


Fig. 3 Logic diagram.

FAMILY DATA

I_{DD} LIMITS category GATES

see Family Specifications

D.C. CHARACTERISTICS

For the single inverter stage (I_7/O_3):

see Family Specifications for input voltages HIGH and LOW (unbuffered stages only).

A.C. CHARACTERISTICS

 $V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^\circ\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	symbol	typ.	max.		typical extrapolation formula
Propagation delays I_1 to $I_6 \rightarrow O_1, O_2$	5	$t_{PHL}; t_{PLH}$	70	140	ns	$43\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10		35	70	ns	$24\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15		30	55	ns	$22\text{ ns} + (0,16\text{ ns/pF}) C_L$
$I_7 \rightarrow O_3$ (unbuffered output)	5	$t_{PHL}; t_{PLH}$	45	90	ns	$18\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10		25	50	ns	$14\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15		20	40	ns	$12\text{ ns} + (0,16\text{ ns/pF}) C_L$
Output transition times HIGH to LOW	5	t_{THL}	60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$
	10		30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$
	15		20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$
LOW to HIGH	5	t_{TLH}	60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$
	10		30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$
	15		20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$

	V_{DD} V	typical formula for P (μW)	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
Dynamic power dissipation per package (P)	5	$1\,000 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	10	$7\,700 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$28\,700 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

APPLICATION INFORMATION

The following information (Figs 4 to 7) is only for the single inverter stage (I₇/O₃).

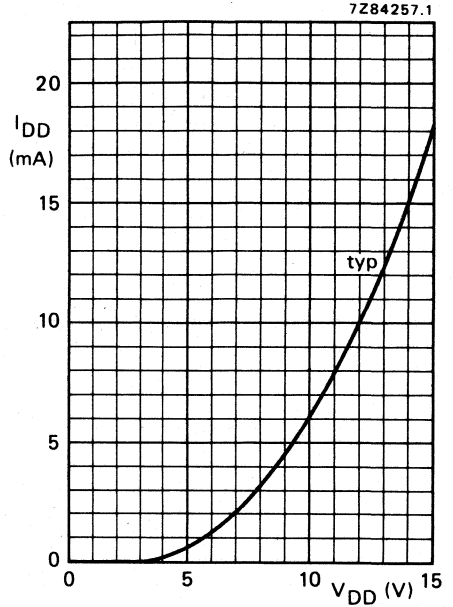
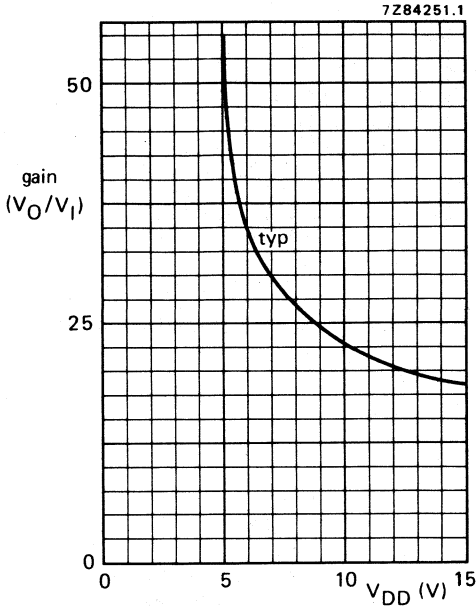


Fig. 4 Voltage gain (V_O/V_I) as a function of supply voltage.

Fig. 5 Supply current as a function of supply voltage.

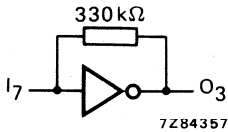


Fig. 6 Test set-up for measuring graphs of Figs 4 and 5.

This is also an example of an analogue amplifier using the single inverter stage (I₇/O₃) of the HEF4000B.

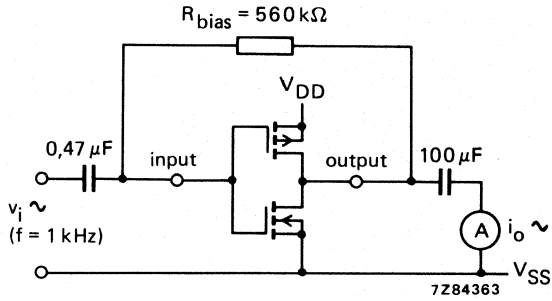
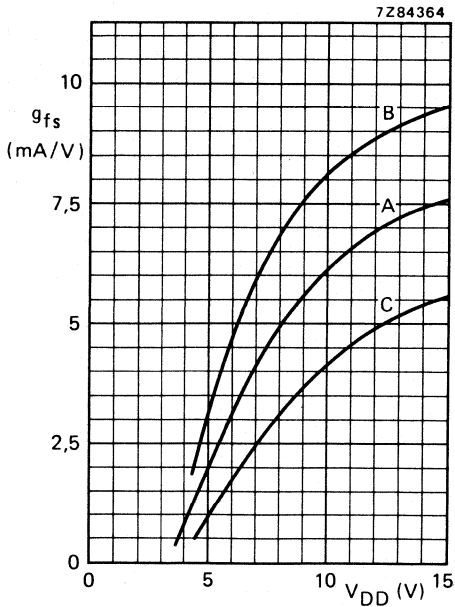


Fig. 7 Test set-up for measuring forward transconductance $g_{fs} = di_o/dv_i$ at v_o is constant (see also graph Fig. 8).



Curves in Fig. 8:

A: average

B: average + 2 s,

C: average - 2 s, in where:

's' is the observed standard deviation.

Fig. 8 Typical forward transconductance g_{fs} as a function of the supply voltage at $T_{amb} = 25\text{ }^{\circ}\text{C}$.



QUADRUPLE 2-INPUT NOR GATE

The HEF4001B provides the positive quadruple 2-input NOR function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

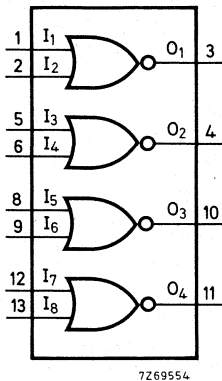


Fig. 1 Functional diagram.

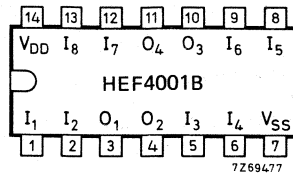


Fig. 2 Pinning diagram.

HEF4001BP: 14-lead DIL; plastic (SOT-27S, T, V).
HEF4001BD: 14-lead DIL; ceramic (SOT-73).
HEF4001BT: 14-lead flat pack; plastic (SO-14; SOT-108A).

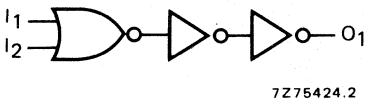


Fig. 3 Logic diagram (one gate).

FAMILY DATA

I_{DD} LIMITS category GATES

see Family Specifications

A.C. CHARACTERISTICS

 $V_{SS} = 0 \text{ V}; T_{amb} = 25 \text{ }^\circ\text{C}; C_L = 50 \text{ pF};$ input transition times $\leq 20 \text{ ns}$

	V_{DD} V	symbol	typ	max		typical extrapolation formula
Propagation delays $I_n \rightarrow O_n$ HIGH to LOW	5	t_{PHL}	60	120	ns	$33 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
	10		25	50	ns	$14 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
	15		20	40	ns	$12 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
LOW to HIGH	5	t_{PLH}	50	100	ns	$23 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
	10		25	45	ns	$14 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
	15		20	35	ns	$12 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
Output transition times HIGH to LOW	5	t_{THL}	60	120	ns	$10 \text{ ns} + (1,0 \text{ ns/pF}) C_L$
	10		30	60	ns	$9 \text{ ns} + (0,42 \text{ ns/pF}) C_L$
	15		20	40	ns	$6 \text{ ns} + (0,28 \text{ ns/pF}) C_L$
LOW to HIGH	5	t_{TLH}	60	120	ns	$10 \text{ ns} + (1,0 \text{ ns/pF}) C_L$
	10		30	60	ns	$9 \text{ ns} + (0,42 \text{ ns/pF}) C_L$
	15		20	40	ns	$6 \text{ ns} + (0,28 \text{ ns/pF}) C_L$

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$1100 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz)
	10	$5000 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_o = output freq. (MHz)
	15	$14200 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	C_L = load capacitance (pF)
			$\Sigma(f_o C_L)$ = sum of outputs
			V_{DD} = supply voltage (V)

QUADRUPLE 2-INPUT NOR GATE



The HEF4001UB is a quadruple 2-input NOR gate. This unbuffered single stage version provides a direct implementation of the NOR function. The output impedance and output transition time depends on the input voltage and input rise and fall times applied.

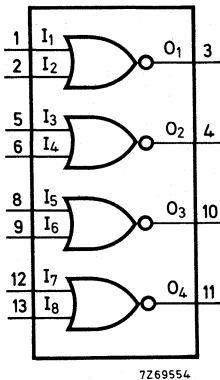


Fig. 1 Functional diagram.

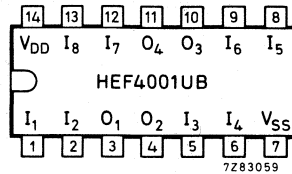


Fig. 2 Pinning diagram.

HEF4001UBP: 14-lead DIL; plastic (SOT-27S,T,V).
HEF4001UBD: 14-lead DIL; ceramic (SOT-73).
HEF4001UBT: 14-lead flat pack; plastic (SO-14; SOT-108A).

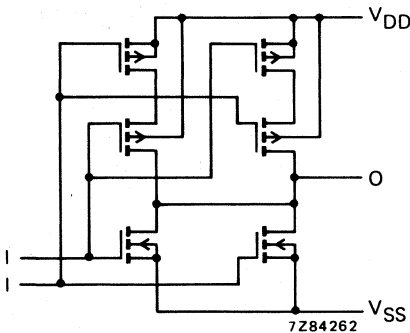


Fig. 3 Schematic diagram (one gate). The splitting-up of the p-transistors provide identical inputs.

FAMILY DATA

I_{DD} LIMITS category GATES

} see Family Specifications

A.C. CHARACTERISTICS

 $V_{SS} = 0 \text{ V}$; $T_{amb} = 25 \text{ }^\circ\text{C}$; $C_L = 50 \text{ pF}$; input transition times $\leq 20 \text{ ns}$

	V_{DD} V	symbol	typ.	max.		typical extrapolation formula
Propagation delays $I_n \rightarrow O_n$ HIGH to LOW	5	t _{PHL}	65	130	ns	$30 \text{ ns} + (0,70 \text{ ns/pF}) C_L$
	10		30	60	ns	$17 \text{ ns} + (0,27 \text{ ns/pF}) C_L$
	15		25	50	ns	$15 \text{ ns} + (0,20 \text{ ns/pF}) C_L$
LOW to HIGH	5	t _{PLH}	40	80	ns	$13 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
	10		20	40	ns	$9 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
	15		15	30	ns	$7 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
Output transition times HIGH to LOW	5	t _{THL}	75	150	ns	$15 \text{ ns} + (1,20 \text{ ns/pF}) C_L$
	10		30	60	ns	$6 \text{ ns} + (0,48 \text{ ns/pF}) C_L$
	15		20	40	ns	$4 \text{ ns} + (0,32 \text{ ns/pF}) C_L$
LOW to HIGH	5	t _{TLH}	60	110	ns	$10 \text{ ns} + (1,00 \text{ ns/pF}) C_L$
	10		30	60	ns	$9 \text{ ns} + (0,42 \text{ ns/pF}) C_L$
	15		20	40	ns	$6 \text{ ns} + (0,28 \text{ ns/pF}) C_L$
Input capacitance		C _{IN}	—	10	pF	

	V_{DD} V	typical formula for P (μW)	where f _i = input freq. (MHz) f _o = output freq. (MHz) C _L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V _{DD} = supply voltage (V)
Dynamic power dissipation per package (P)	5	$500 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	10	$5000 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$30\,000 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

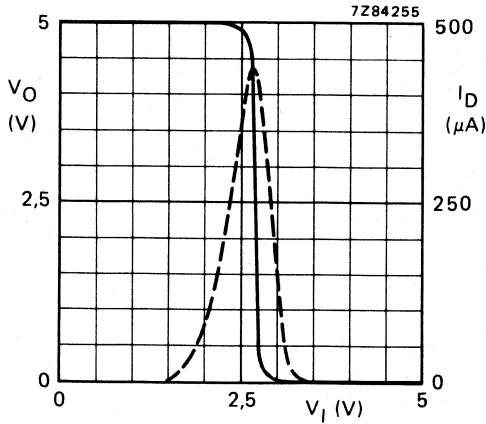


Fig. 4 Typical transfer characteristics; one input, the other input connected to V_{SS} ; — V_O ; - - - I_D (drain current); $I_O = 0$; $V_{DD} = 5$ V.

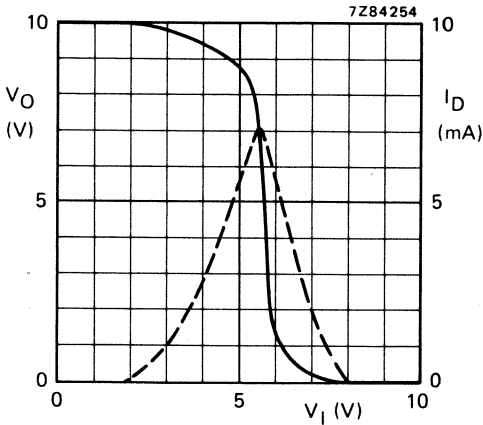


Fig. 5 Typical transfer characteristics; one input, the other input connected to V_{SS} ; — V_O ; - - - I_D (drain current); $I_O = 0$; $V_{DD} = 10$ V.

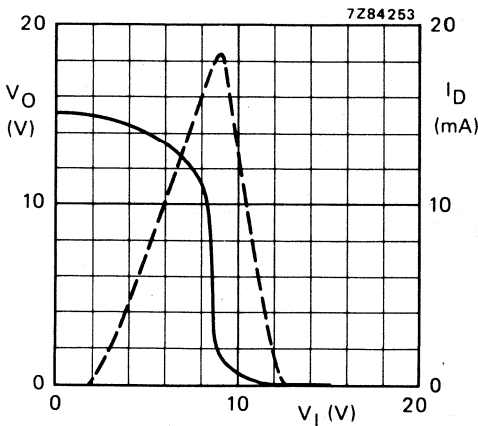


Fig. 6 Typical transfer characteristics; one input, the other input connected to V_{SS} ; — V_O ; - - - I_D (drain current); $I_O = 0$; $V_{DD} = 15$ V.

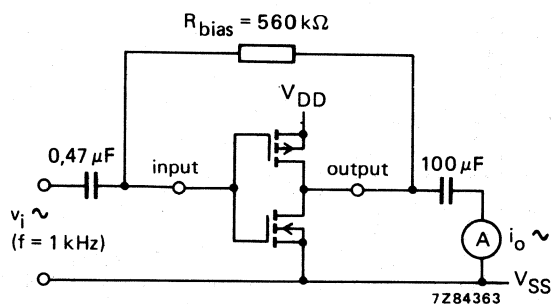


Fig. 7 Test set-up for measuring forward transconductance $g_{fs} = di_o/dv_i$ at v_o is constant (see also graph Fig. 8).

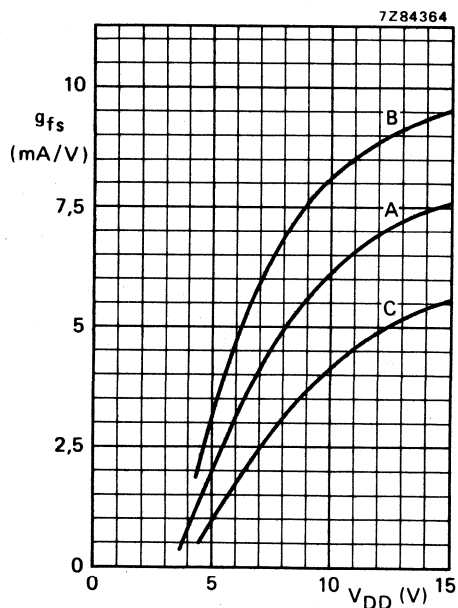


Fig. 8 Typical forward transconductance g_{fs} as a function of the supply voltage at $T_{amb} = 25$ °C.

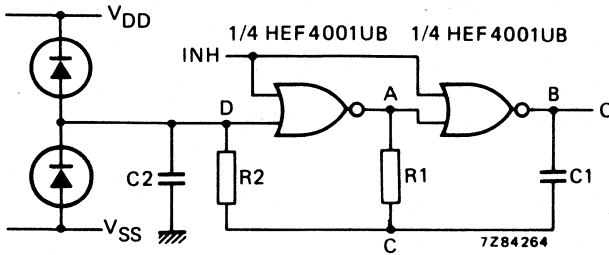
Curves in Fig. 8:

- A : average,
- B : average + 2 s,
- C : average - 2 s, in where:
's' is the observed standard deviation.

APPLICATION INFORMATION

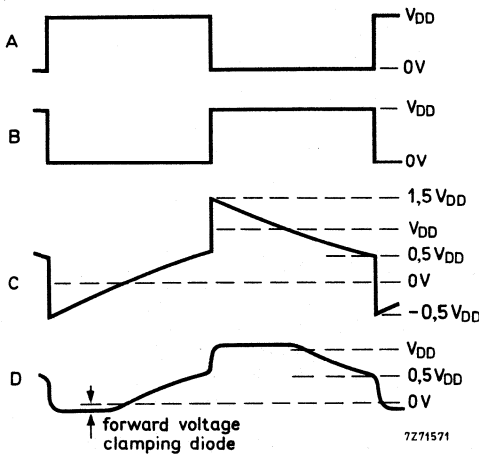
Some examples of applications for the HEF4001UB are shown below.

Because of the fact that this circuit is unbuffered, it is suitable for use in (partly) analogue circuits.



INH	O
H	L
L	OSC

(a)



(b)

Fig. 9(a) Astable relaxation oscillator using two HEF4001UB gates; the diodes may be BAW62; C2 is a parasitic capacitance. (b) Waveforms at the points marked A, B, C and D in the circuit diagram.

In Fig. 9 the oscillation frequency is mainly determined by $R1C1$, provided $R1 \ll R2$ and $R2C2 \ll R1C1$.

The function of $R2$ is to minimize the influence of the forward voltage across the protection diodes on the frequency; $C2$ is a stray (parasitic) capacitance. The period T_p is given by $T_p = T_1 + T_2$, in which

$$T_1 = R1C1 \ln \frac{V_{DD} + V_{ST}}{V_{ST}} \text{ and } T_2 = R1C1 \ln \frac{2V_{DD} - V_{ST}}{V_{DD} - V_{ST}} \text{ where}$$

V_{ST} is the signal threshold level of the gate. The period is fairly independent of V_{DD} , V_{ST} and temperature. The duty factor, however, is influenced by V_{ST} .

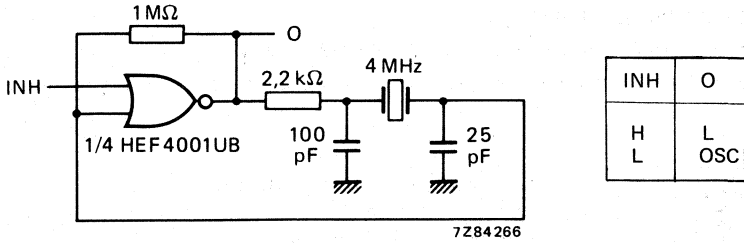


Fig. 10 Example of a crystal oscillator using one HEF4001UB gate.

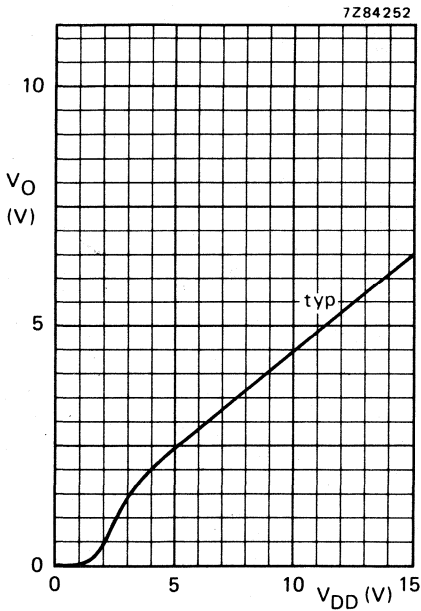


Fig. 11 Output voltages as a function of supply voltage.

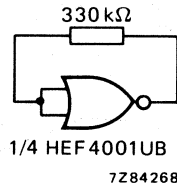


Fig. 12 Test set-up for measuring graph of Fig. 11. Condition: all other inputs connected to ground.

NOTES

If a gate is just used as an amplifying inverter, there are two possibilities:

- a. Connecting the inputs together gives simpler wiring, but makes the device output not completely symmetrical.
- b. Connecting one input to V_{SS} will give the device a symmetrical output.

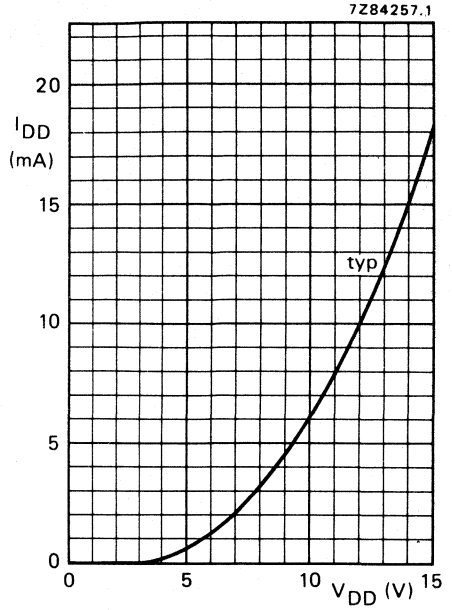
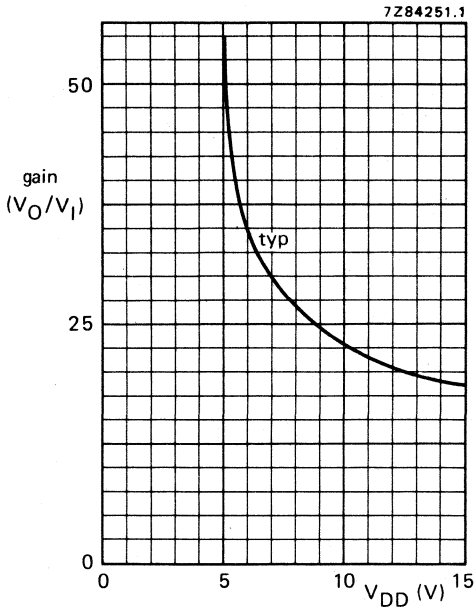


Fig. 13 Voltage gain (V_O/V_I) as a function of supply voltage.

Fig. 14 Supply current as a function of supply voltage.

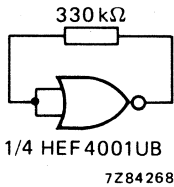


Fig. 15 Test set-up for measuring graphs of Figs 13 and 14. Condition: all other inputs connected to ground.

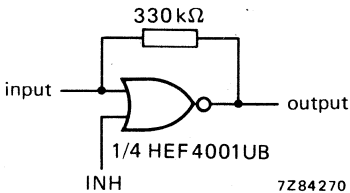


Fig. 16 Example of an analogue amplifier with inhibit using one HEF4001UB gate.

DUAL 4-INPUT NOR GATE



The HEF4002B provides the positive dual 4-input NOR function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

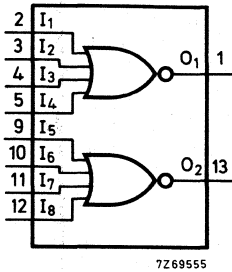


Fig. 1 Functional diagram.

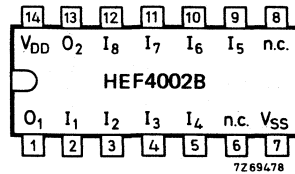


Fig. 2 Pinning diagram.

HEF4002BP : 14-lead DIL; plastic (SOT-27S,T,V).
 HEF4002BD: 14-lead DIL; ceramic (SOT-73).
 HEF4002BT : 14-lead flat pack; plastic (SO-14 ; SOT-108A).

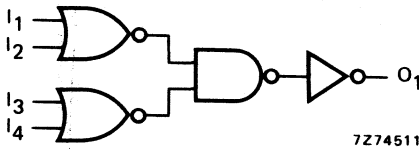


Fig. 3 Logic diagram (one gate).

FAMILY DATA

see Family Specifications

I_{DD} LIMITS category GATES

HEF4002B

gates

A.C. CHARACTERISTICS

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^\circ\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	symbol	typ.	max.		typical extrapolation formula
Propagation delays $I_n \rightarrow O_n$	5	tPHL; tPLH	60	120	ns	$33\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10		25	50	ns	$14\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15		20	40	ns	$12\text{ ns} + (0,16\text{ ns/pF}) C_L$
Output transition times HIGH to LOW	5	tTHL	60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$
	10		30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$
	15		20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$
LOW to HIGH	5	tTLH	60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$
	10		30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$
	15		20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$1050 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz)
	10	$4300 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_o = output freq. (MHz)
	15	$11700 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	C_L = load capacitance (pF)
			$\Sigma(f_o C_L)$ = sum of outputs
			V_{DD} = supply voltage (V)

18-STAGE STATIC SHIFT REGISTER



The HEF4006B is an 18-stage shift register arranged as two 4-stage and two 5-stage shift registers with a common clock input (\overline{CP}). The two 4-stage shift registers each have a data input (D_A , D_B) and a data output (O_{3A} , O_{3B}); the two 5-stage shift registers each have a data input (D_C , D_D) and data outputs from the fourth and fifth stages (O_{3C} , O_{4C} , O_{3D} , O_{4D}).

The registers can be operated in parallel or interconnected to form a single shift register of up to 18 bits. Data are shifted into the first register position of each register from the data inputs (D_A to D_D) and all the data in each register are shifted one position to the right on the HIGH to LOW transition of \overline{CP} .

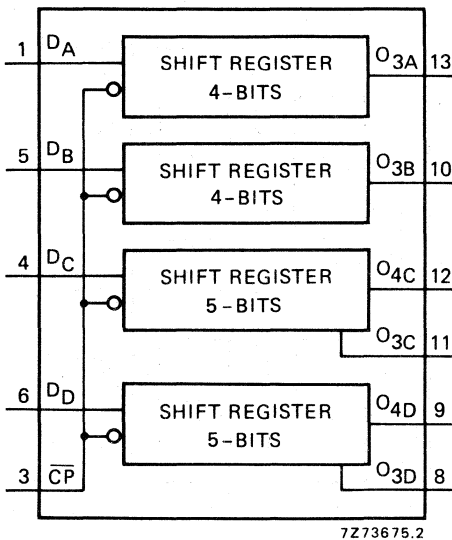


Fig. 1 Functional diagram.

PINNING

D_A to D_D data inputs
 \overline{CP} clock input (HIGH to LOW; edge-triggered)
 O_{3A} to O_{3D} ; O_{4C} ; O_{4D} data outputs

FAMILY DATA

I_{DD} LIMITS category MSI

} see Family Specifications

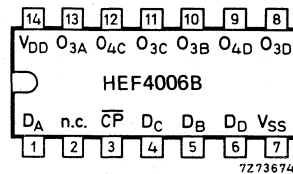


Fig. 2 Pinning diagram.

HEF4006BP: 14-lead DIL; plastic (SOT-27S, T, V).
 HEF4006BD: 14-lead DIL; ceramic (SOT-73).
 HEF4006BT: 14-lead flat pack; plastic (SO-14; SOT-108A).

FUNCTION TABLE

D_n	\overline{CP}	O_n^*
D_1	\nearrow	D_1
X	\searrow	no change

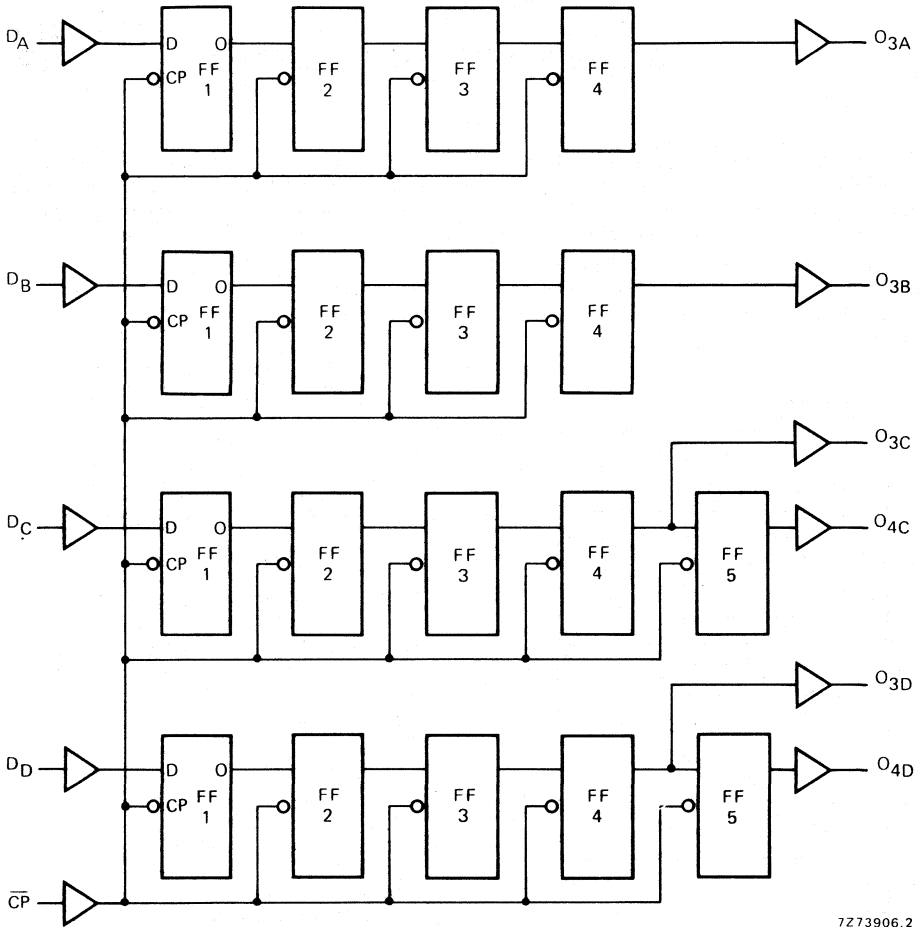
X = state is immaterial

\nearrow = positive-going transition

\searrow = negative-going transition

D_1 = either HIGH or LOW

* The moment D_1 appears at O depends on the register length.



7273906.2

Fig. 3 Logic diagram.

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V _{DD} V	symbol	min	typ	max	typical extrapolation formula	
Propagation delays CP → O _n HIGH to LOW	5	t _{PHL}		90	180	ns	63 ns + (0,55 ns/pF) C _L
	10		40	80	ns	29 ns + (0,23 ns/pF) C _L	
	15		30	60	ns	22 ns + (0,16 ns/pF) C _L	
LOW to HIGH	5	t _{PLH}		90	180	ns	63 ns + (0,55 ns/pF) C _L
	10		40	85	ns	29 ns + (0,23 ns/pF) C _L	
	15		35	70	ns	27 ns + (0,16 ns/pF) C _L	
Output transition times HIGH to LOW	5	t _{THL}		60	120	ns	10 ns + (1,0 ns/pF) C _L
	10		30	60	ns	9 ns + (0,42 ns/pF) C _L	
	15		20	40	ns	6 ns + (0,28 ns/pF) C _L	
LOW to HIGH	5	t _{TLH}		60	120	ns	10 ns + (1,0 ns/pF) C _L
	10		30	60	ns	9 ns + (0,42 ns/pF) C _L	
	15		20	40	ns	6 ns + (0,28 ns/pF) C _L	
Minimum clock pulse width; HIGH	5	t _{WCPH}	60	30		ns	} see also waveforms Fig. 4
	10		40	20		ns	
	15		30	15		ns	
Set-up time D _n → CP	5	t _{su}	20	10		ns	
	10		10	5		ns	
	15		5	0		ns	
Hold time D _n → CP	5	t _{hold}	5	-5		ns	
	10		5	0		ns	
	15		5	0		ns	
Maximum clock pulse frequency	5	f _{max}		9	18	MHz	
	10		15	30	MHz		
	15		18	36	MHz		

	V _{DD} V	typical formula for P (μW)	where f _i = input freq. (MHz) f _o = output freq. (MHz) C _L = load capacitance (pF) Σ(f _o C _L) = sum of outputs V _{DD} = supply voltage (V)
Dynamic power dissipation per package (P)	5	600 f _i + Σ(f _o C _L) × V _{DD} ²	
	10	3200 f _i + Σ(f _o C _L) × V _{DD} ²	
	15	11 600 f _i + Σ(f _o C _L) × V _{DD} ²	

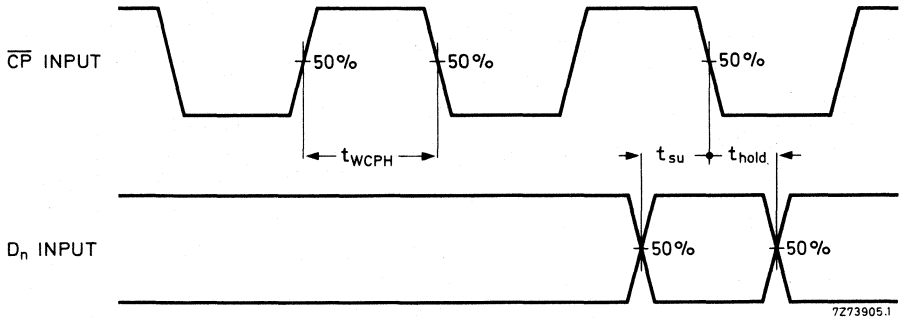


Fig. 4 Waveforms showing minimum clock pulse width, and set-up and hold-times for D_n to \overline{CP} . Set-up and hold times are shown as positive values but may be specified as negative values.

DUAL COMPLEMENTARY PAIR AND INVERTER



The HEF4007UB is a dual complementary pair and an inverter with access to each device. It has three n-channel and three p-channel enhancement mode MOS transistors.

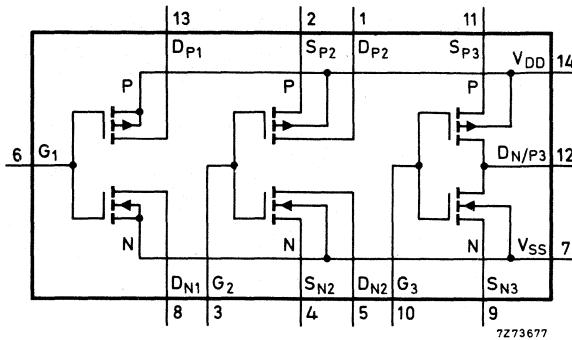


Fig. 1 Schematic diagram.

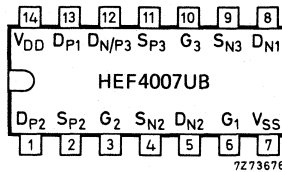


Fig. 2 Pinning diagram.

HEF4007UBP: 14-lead DIL; plastic (SOT-27).
 HEF4007UBD: 14-lead DIL; ceramic (SOT-73).
 HEF4007UBT: 14-lead flat pack; plastic
 (SO-14; SOT-108A).

PINNING

Sp2, Sp3 source connections to 2nd and 3rd p-channel transistors
 Dp1, Dp2 drain connections from the 1st and 2nd p-channel transistors
 Dn1, Dn2 drain connections from the 1st and 2nd n-channel transistors
 Sn2, Sn3 source connections to the 2nd and 3rd n-channel transistors
 Dn/P3 common connection to the 3rd p-channel and n-channel transistor drains
 G1 to G3 gate connections to n-channel and p-channel of the three transistor pairs

FAMILY DATA

IDD LIMITS category GATES

} see Family Specifications

A.C. CHARACTERISTICS

$V_{SS} = 0 \text{ V}$; $T_{amb} = 25 \text{ }^\circ\text{C}$; $C_L = 50 \text{ pF}$; input transition times $\leq 20 \text{ ns}$

	V_{DD} V	symbol	typ.	max.		typical extrapolation formula
Propagation delays $G_n \rightarrow D_n$; D_p HIGH to LOW	5	t_{PHL}	40	80	ns	$13 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
	10		20	40	ns	$9 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
	15		15	30	ns	$7 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
LOW to HIGH	5	t_{PLH}	40	75	ns	$13 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
	10		20	40	ns	$9 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
	15		15	30	ns	$7 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
Output transition times HIGH to LOW	5	t_{THL}	60	120	ns	$10 \text{ ns} + (1,0 \text{ ns/pF}) C_L$
	10		30	60	ns	$9 \text{ ns} + (0,42 \text{ ns/pF}) C_L$
	15		20	40	ns	$6 \text{ ns} + (0,28 \text{ ns/pF}) C_L$
LOW to HIGH	5	t_{TLH}	60	120	ns	$10 \text{ ns} + (1,0 \text{ ns/pF}) C_L$
	10		30	60	ns	$9 \text{ ns} + (0,42 \text{ ns/pF}) C_L$
	15		20	40	ns	$6 \text{ ns} + (0,28 \text{ ns/pF}) C_L$

	V_{DD} V	typical formula for P (μW)	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
Dynamic power dissipation per package (P)	5	$4500 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	10	$20\,000 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$50\,000 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

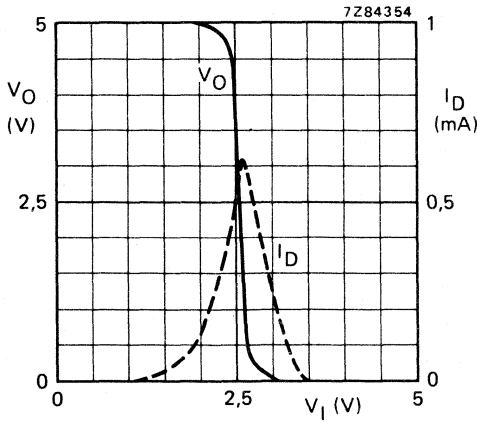


Fig. 3 Typical drain current I_D and output voltage V_O as functions of input voltage; $V_{DD} = 5$ V; $T_{amb} = 25$ °C.

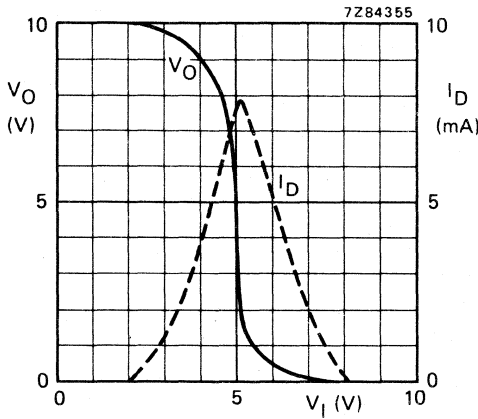


Fig. 4 Typical drain current I_D and output voltage V_O as functions of input voltage; $V_{DD} = 10$ V; $T_{amb} = 25$ °C.

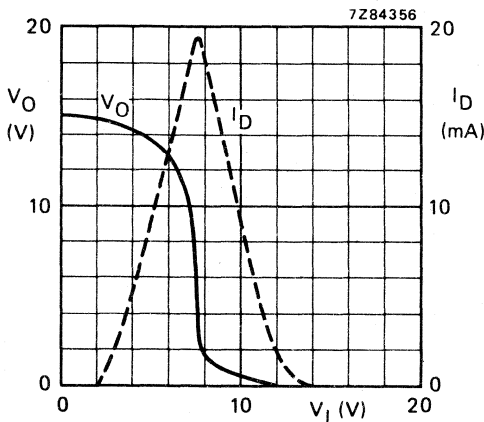


Fig. 5 Typical drain current I_D and output voltage V_O as functions of input voltage; $V_{DD} = 15$ V; $T_{amb} = 25$ °C.

APPLICATION INFORMATION

Some examples of applications for the HEF4007UB are:

- High input impedance amplifiers
- Linear amplifiers
- (Crystal) oscillators
- High-current sink and source drivers
- High impedance buffers.

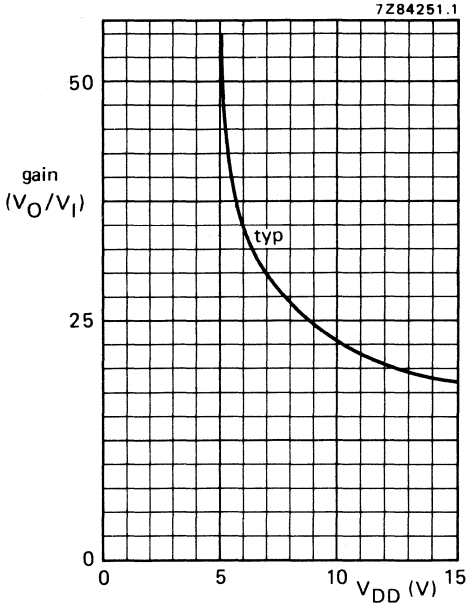


Fig. 6 Voltage gain (V_O/V_I) as a function of supply voltage.

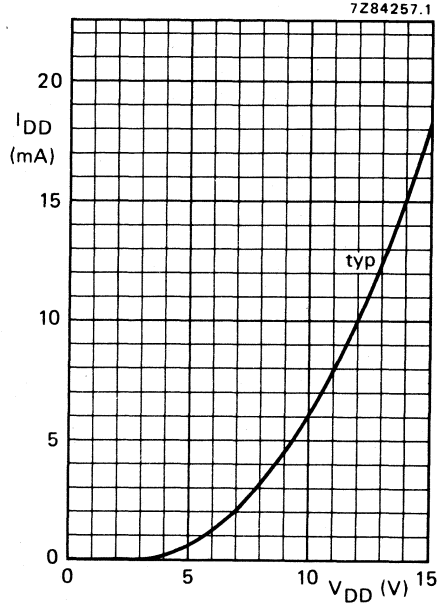


Fig. 7 Supply current as a function of supply voltage.

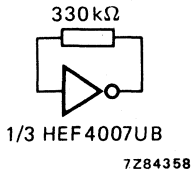


Fig. 8 Test set-up for measuring graphs of Figs 6 and 7. This is also an example of an analogue amplifier using one HEF4007UB gate.

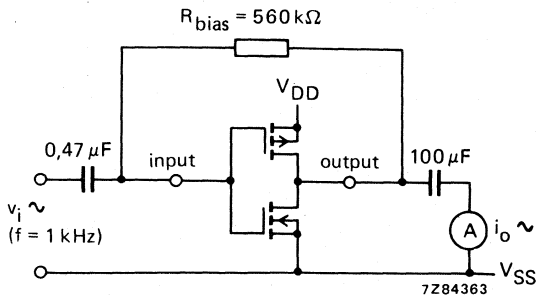
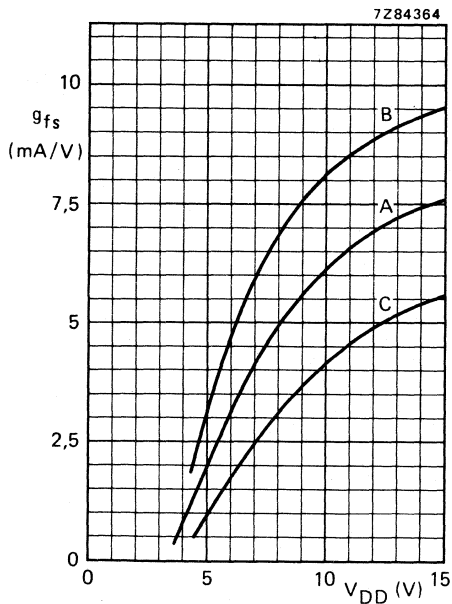


Fig. 9 Test set-up for measuring forward transconductance $g_{fs} = di_o/dv_i$ at v_o is constant (see also graph Fig. 10).



Curves in Fig. 10:

- A: average,
- B: average + 2 s,
- C: average - 2 s, in where 's' is the observed standard deviation.

Fig. 10 Typical forward transconductance g_{fs} as a function of the supply voltage at $T_{amb} = 25\text{ }^{\circ}\text{C}$.

APPLICATION INFORMATION (continued)

Figures 11 to 14 show some applications in which the HEF4007UB is used.

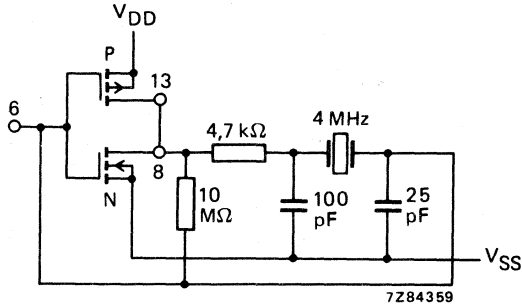


Fig. 11 4 MHz crystal oscillator.

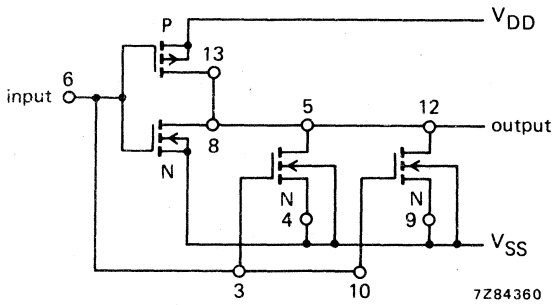


Fig. 12 High current sink driver.

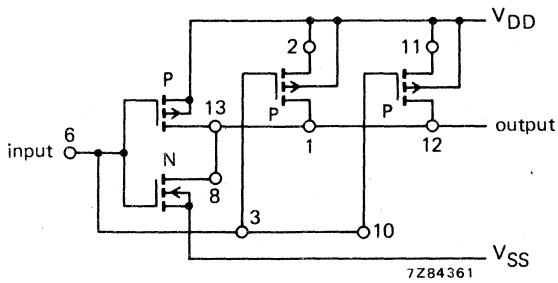


Fig. 13 High current source driver.

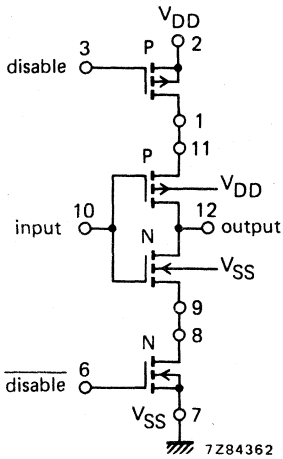


Fig. 14 High impedance buffer.

FUNCTION TABLE for Fig. 14.

input	disable	output
H	L	L
L	L	H
X	H	open

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

X = state is immaterial

NOTE

Rules for maintaining electrical isolation between transistors and monolithic substrate:

Pin number 14 must be maintained at the most positive (or equally positive) potential with respect to any other pin of the HEF4007UB.

Pin number 7 must be maintained at the most negative (or equally negative) potential with respect to any other pin of the HEF4007UB.

Violation of these rules will result in improper transistor operation and/or possible permanent damage to the HEF4007UB.

4-BIT BINARY FULL ADDER



The HEF4008B is a 4-bit binary full adder with two 4-bit data inputs (A_0 to A_3 , B_0 to B_3), a carry input (C_{IN}), four sum outputs (S_0 to S_3), and a carry output (C_{OUT}). The IC uses full look-ahead across 4-bits to generate C_{OUT} . This minimizes the necessity for extensive look-ahead and carry-cascading circuits.

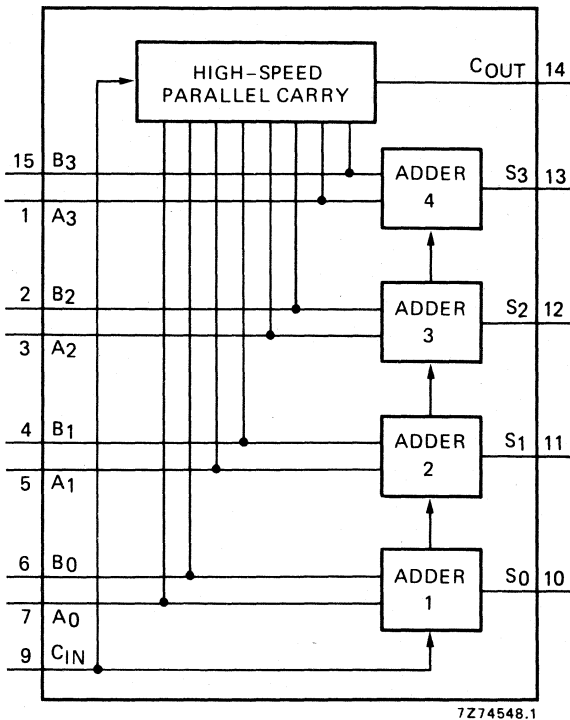


Fig. 1 Functional diagram.

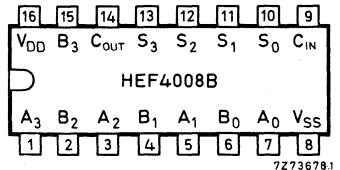


Fig. 2 Pinning diagram.

PINNING

A_0 to A_3 data inputs
 B_0 to B_3 data inputs
 S_0 to S_3 sum outputs
 C_{IN} carry input
 C_{OUT} carry output

TRUTH TABLE (one adder)

C_{IN}	A	B	C_{OUT}	S
L	L	L	L	L
L	L	H	L	H
L	H	L	L	H
L	H	H	H	L
H	L	L	L	H
H	L	H	H	L
H	H	L	H	L
H	H	H	H	H

HEF4008BP: 16-lead DIL; plastic (SOT-38Z).

HEF4008BD: 16-lead DIL; ceramic (SOT-74).

HEF4008BT: 16-lead flat pack; plastic (SO-16; SOT-109A).

FAMILY DATA

I_{DD} LIMITS category MSI

} see Family Specifications

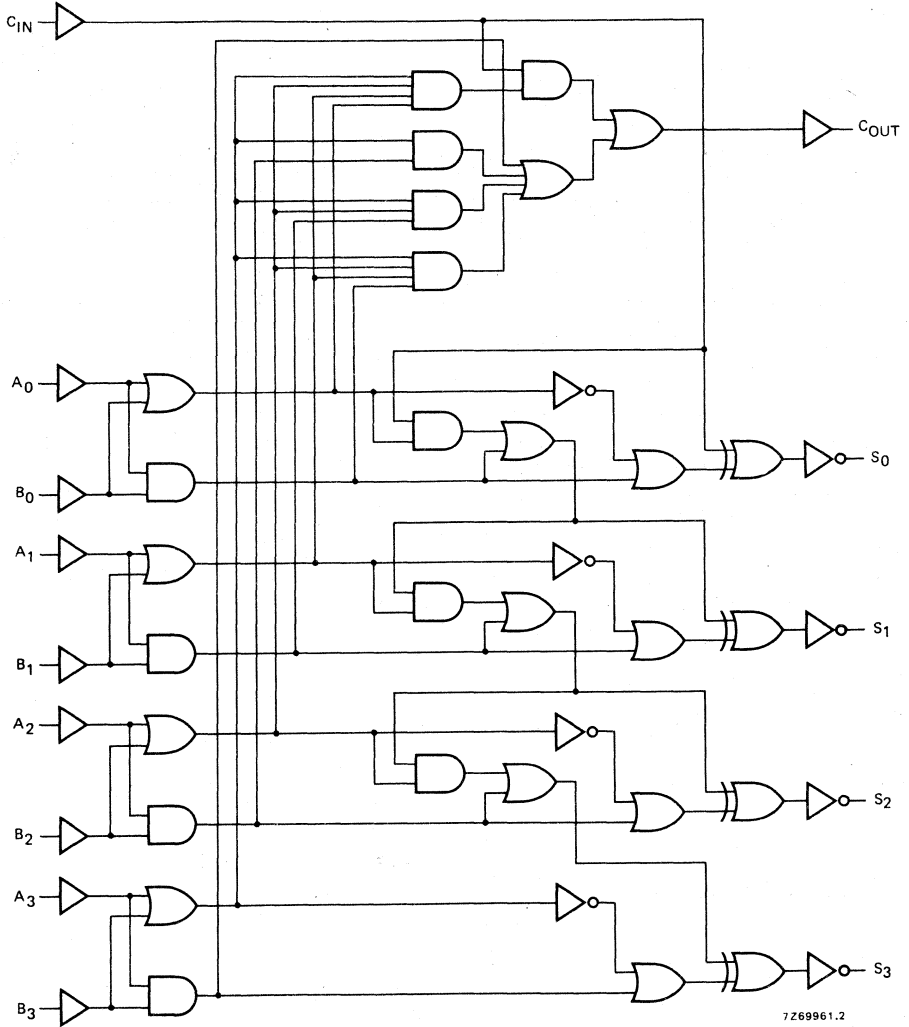


Fig. 3 Logic diagram.

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V _{DD} V	symbol	min.	typ.	max.	typical extrapolation formula
Propagation delays sum in → sum out HIGH to LOW	5	t _{PHL}	150	300	ns	123 ns + (0,55 ns/pF) C _L
	10		55	110	ns	44 ns + (0,23 ns/pF) C _L
	15		40	80	ns	32 ns + (0,16 ns/pF) C _L
LOW to HIGH	5	t _{PLH}	135	270	ns	108 ns + (0,55 ns/pF) C _L
	10		55	110	ns	44 ns + (0,23 ns/pF) C _L
	15		40	80	ns	32 ns + (0,16 ns/pF) C _L
sum in → C _{OUT} HIGH to LOW	5	t _{PHL}	125	250	ns	98 ns + (0,55 ns/pF) C _L
	10		50	100	ns	39 ns + (0,23 ns/pF) C _L
	15		35	70	ns	27 ns + (0,16 ns/pF) C _L
LOW to HIGH	5	t _{PLH}	100	200	ns	73 ns + (0,55 ns/pF) C _L
	10		45	90	ns	34 ns + (0,23 ns/pF) C _L
	15		30	60	ns	22 ns + (0,16 ns/pF) C _L
C _{IN} → sum out HIGH to LOW	5	t _{PHL}	130	260	ns	103 ns + (0,55 ns/pF) C _L
	10		50	100	ns	39 ns + (0,23 ns/pF) C _L
	15		35	70	ns	27 ns + (0,16 ns/pF) C _L
LOW to HIGH	5	t _{PLH}	115	230	ns	88 ns + (0,55 ns/pF) C _L
	10		50	100	ns	39 ns + (0,23 ns/pF) C _L
	15		35	70	ns	27 ns + (0,16 ns/pF) C _L
C _{IN} → C _{OUT} HIGH to LOW	5	t _{PHL}	90	180	ns	63 ns + (0,55 ns/pF) C _L
	10		35	70	ns	24 ns + (0,23 ns/pF) C _L
	15		25	50	ns	17 ns + (0,16 ns/pF) C _L
LOW to HIGH	5	t _{PLH}	75	150	ns	48 ns + (0,55 ns/pF) C _L
	10		35	70	ns	24 ns + (0,23 ns/pF) C _L
	15		25	50	ns	17 ns + (0,16 ns/pF) C _L
Output transition times HIGH to LOW	5	t _{THL}	60	120	ns	10 ns + (1,0 ns/pF) C _L
	10		30	60	ns	9 ns + (0,42 ns/pF) C _L
	15		20	40	ns	6 ns + (0,28 ns/pF) C _L
LOW to HIGH	5	t _{TLH}	60	120	ns	10 ns + (1,0 ns/pF) C _L
	10		30	60	ns	9 ns + (0,42 ns/pF) C _L
	15		20	40	ns	6 ns + (0,28 ns/pF) C _L

	V _{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	1 500 f _i + Σ(f _o C _L) × V _{DD} ²	f _i = input freq. (MHz)
	10	6 000 f _i + Σ(f _o C _L) × V _{DD} ²	f _o = output freq. (MHz)
	15	13 500 f _i + Σ(f _o C _L) × V _{DD} ²	C _L = load capacitance (pF)
			Σ(f _o C _L) = sum of outputs
			V _{DD} = supply voltage (V)

APPLICATION INFORMATION

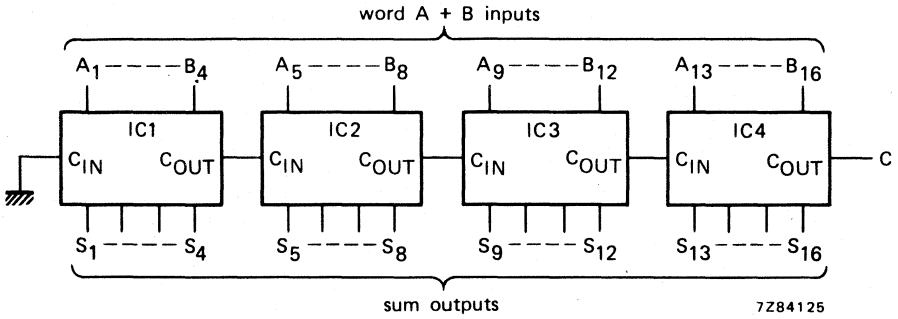


Fig. 4 Example of a 16-bit full adder using 4 HEF4008B ICs.

QUADRUPLE 2-INPUT NAND GATE



The HEF4011B provides the positive quadruple 2-input NAND function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

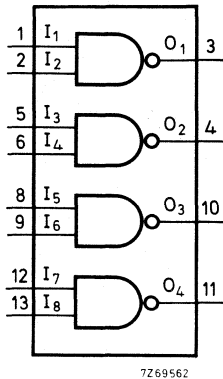


Fig. 1 Functional diagram.

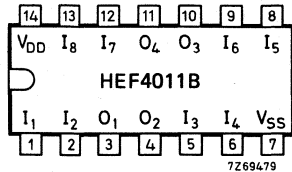


Fig. 2 Pinning diagram.

HEF4011BP: 14-lead DIL; plastic (SOT-27S, T, V).
HEF4011BD: 14-lead DIL; ceramic (SOT-73).
HEF4011BT: 14-lead flat pack; plastic (SO-14; SOT-108A).

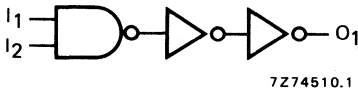


Fig. 3 Logic diagram (one gate).

FAMILY DATA

I_{DD} LIMITS category GATES

} see Family Specifications

A.C. CHARACTERISTICS

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	symbol	typ	max		typical extrapolation formula
Propagation delays $I_n \rightarrow O_n$	5	$t_{PHL}; t_{PLH}$	55	110	ns	$28\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10		25	45	ns	$14\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15		20	35	ns	$12\text{ ns} + (0,16\text{ ns/pF}) C_L$
Output transition times HIGH to LOW	5	t_{THL}	60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$
	10		30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$
	15		20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$
LOW to HIGH	5	t_{TLH}	60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$
	10		30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$
	15		20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$

	V_{DD} V	typical formula for P (μW)	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
Dynamic power dissipation per package (P)	5	$1300 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	10	$6000 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$20100 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

QUADRUPLE 2-INPUT NAND GATE



The HEF4011UB is a quadruple 2-input NAND gate. This unbuffered single stage version provides a direct implementation of the NAND function. The output impedance and output transition time depends on the input voltage and input rise and fall times applied.

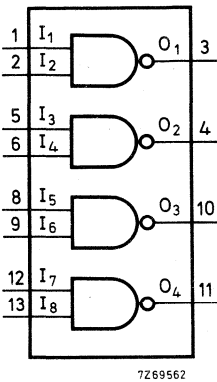


Fig. 1 Functional diagram.

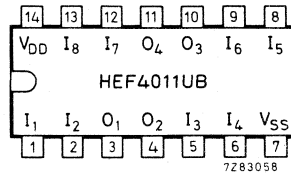


Fig. 2 Pinning diagram.

HEF4011UBP: 14-lead DIL; plastic (SOT-27S,T,V).
HEF4011UBD: 14-lead DIL; ceramic (SOT-73).
HEF4011UBT: 14-lead flat pack; plastic (SO-14; SOT-108A).

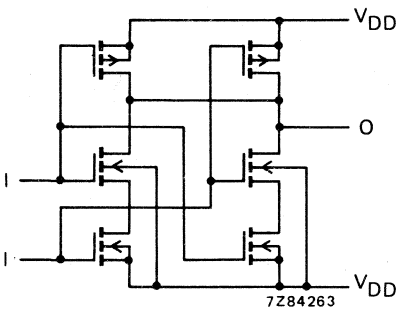


Fig. 3 Schematic diagram (one gate). The splitting-up of the n-transistors provide identical inputs.

FAMILY DATA

I_{DD} LIMITS category GATES

} see Family Specifications

A.C. CHARACTERISTICS

 $V_{SS} = 0 \text{ V}$; $T_{amb} = 25 \text{ }^\circ\text{C}$; $C_L = 50 \text{ pF}$; input transition times $\leq 20 \text{ ns}$

	V_{DD} V	symbol	typ.	max.		typical extrapolation formula
Propagation delays $I_n \rightarrow O_n$ HIGH to LOW	5	t_{PHL}	60	120	ns	$25 \text{ ns} + (0,70 \text{ ns/pF}) C_L$
	10		25	50	ns	$12 \text{ ns} + (0,27 \text{ ns/pF}) C_L$
	15		20	40	ns	$10 \text{ ns} + (0,20 \text{ ns/pF}) C_L$
LOW to HIGH	5	t_{PLH}	35	70	ns	$8 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
	10		20	40	ns	$9 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
	15		17	35	ns	$9 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
Output transition times HIGH to LOW	5	t_{THL}	75	150	ns	$15 \text{ ns} + (1,20 \text{ ns/pF}) C_L$
	10		30	60	ns	$6 \text{ ns} + (0,48 \text{ ns/pF}) C_L$
	15		20	40	ns	$4 \text{ ns} + (0,32 \text{ ns/pF}) C_L$
LOW to HIGH	5	t_{TLH}	60	110	ns	$10 \text{ ns} + (1,00 \text{ ns/pF}) C_L$
	10		30	60	ns	$9 \text{ ns} + (0,42 \text{ ns/pF}) C_L$
	15		20	40	ns	$6 \text{ ns} + (0,28 \text{ ns/pF}) C_L$
Input capacitance		C_{IN}		10	pF	

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$500 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz)
	10		f_o = output freq. (MHz)
	15		C_L = load capacitance (pF)
			$\Sigma(f_o C_L)$ = sum of outputs
			V_{DD} = supply voltage (V)

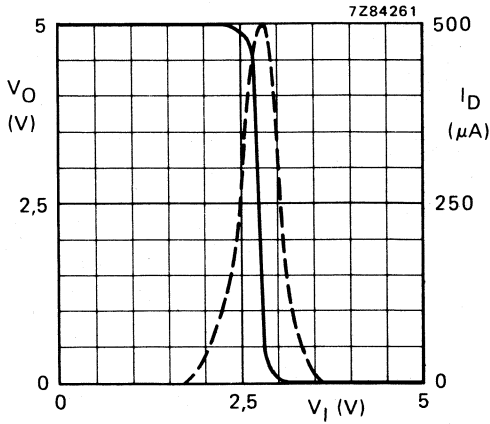


Fig. 4 Typical transfer characteristics; one input, the other input connected to V_{DD} ; — V_O ; - - - I_D (drain current); $I_O = 0$; $V_{DD} = 5$ V.

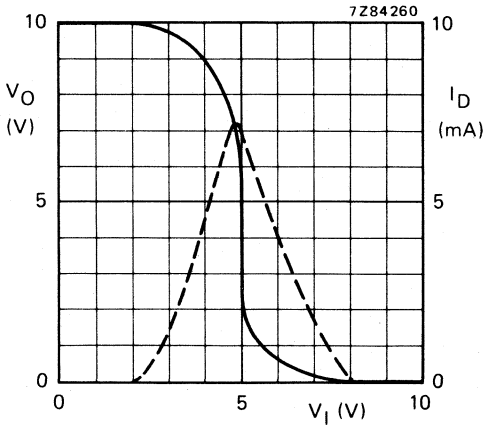


Fig. 5 Typical transfer characteristics; one input, the other input connected to V_{DD} ; — V_O ; - - - I_D (drain current); $I_O = 0$; $V_{DD} = 10$ V.

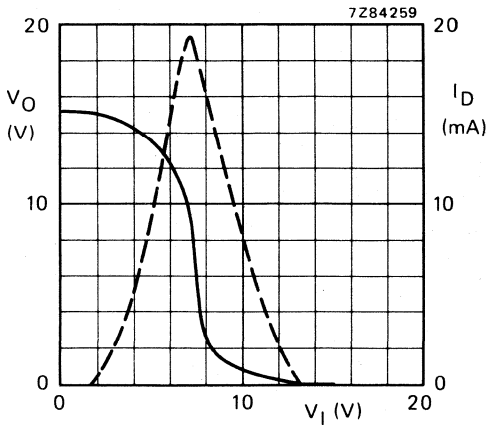


Fig. 6 Typical transfer characteristics; one input, the other input connected to V_{DD} ; — V_O ; - - - I_D (drain current); $I_O = 0$; $V_{DD} = 15$ V.

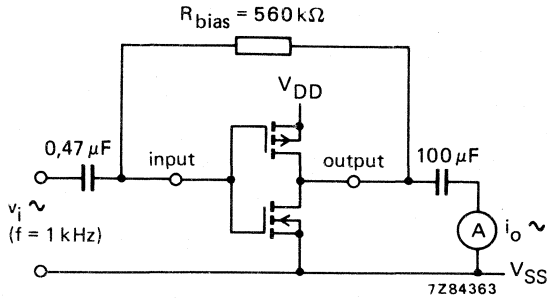


Fig. 7 Test set-up for measuring forward transconductance $g_{fs} = di_o/dv_i$ at v_o is constant (see also graph Fig. 8).

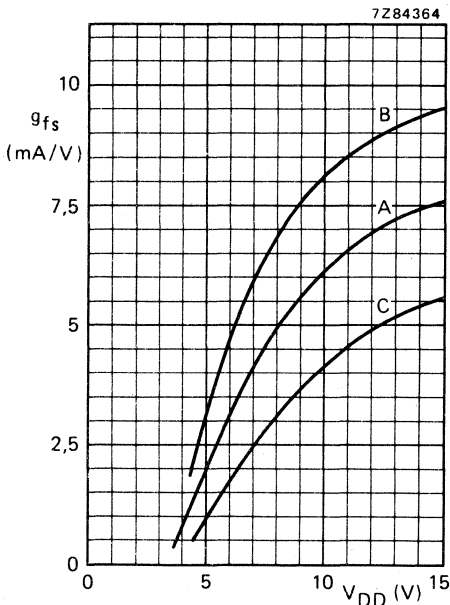


Fig. 8 Typical forward transconductance g_{fs} as a function of the supply voltage at $T_{amb} = 25$ °C.

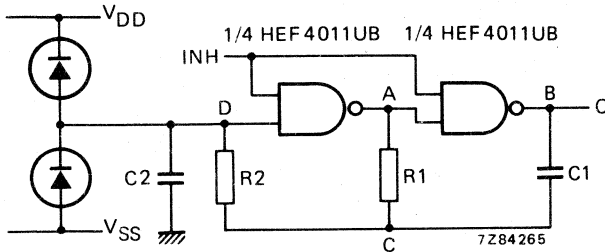
Curves in Fig. 8:

- A : average,
- B : average + 2 s,
- C : average - 2 s, in where:
's' is the observed standard deviation.

APPLICATION INFORMATION

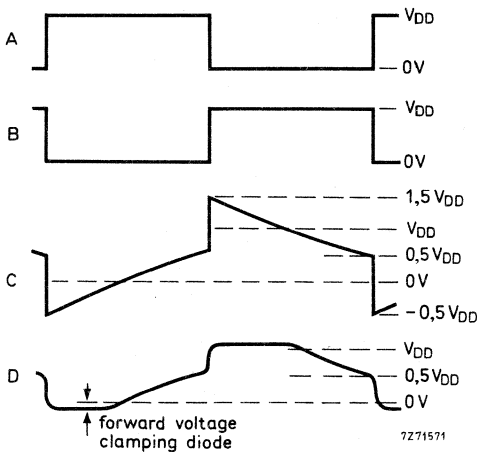
Some examples of applications for the HEF4011UB are shown below.

Because of the fact that this circuit is unbuffered, it is suitable for use in (partly) analogue circuits.



INH	O
L	H
H	OSC

(a)



(b)

Fig. 9(a) Astable relaxation oscillator using two HEF4011UB gates; the diodes may be BAW62; C2 is a parasitic capacitance. (b) Waveforms at the points marked A, B, C and D in the circuit diagram.

In Fig. 9 the oscillation frequency is mainly determined by $R1C1$, provided $R1 \ll R2$ and $R2C2 \ll R1C1$.

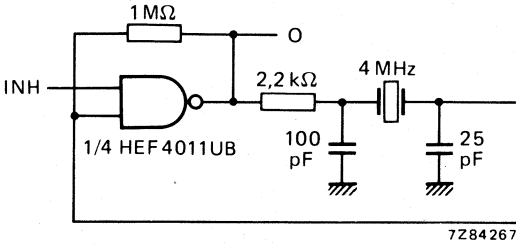
The function of R2 is to minimize the influence of the forward voltage across the protection diodes on the frequency; C2 is a stray (parasitic) capacitance. The period T_p is given by $T_p = T_1 + T_2$, in which

$$T_1 = R1C1 \ln \frac{V_{DD} + V_{ST}}{V_{ST}} \quad \text{and} \quad T_2 = R1C1 \ln \frac{2V_{DD} - V_{ST}}{V_{DD} - V_{ST}} \quad \text{where}$$

V_{ST} is the signal threshold level of the gate. The period is fairly independent of V_{DD} , V_{ST} and temperature. The duty factor, however, is influenced by V_{ST} .

HEF4011UB

gates



INH	O
L	H
H	OSC

Fig. 10 Example of a crystal oscillator using one HEF4011UB gate.

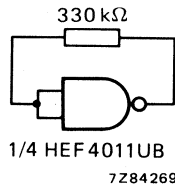
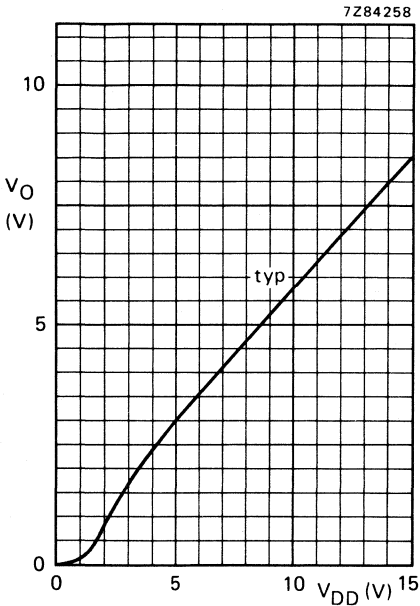


Fig. 12 Test set-up for measuring graph of Fig. 11. Condition: all other inputs connected to ground.

Fig. 11 Output voltage as a function of supply voltage.

NOTES

If a gate is just used as an amplifying inverter, there are two possibilities:

- Connecting the inputs together gives simpler wiring, but makes the device output not completely symmetrical.
- Connecting one input to V_{DD} will give the device a symmetrical output.

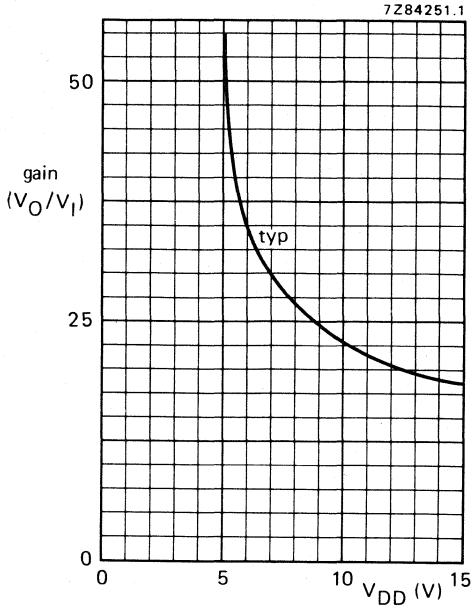


Fig. 13 Voltage gain (V_O/V_I) as a function of supply voltage.

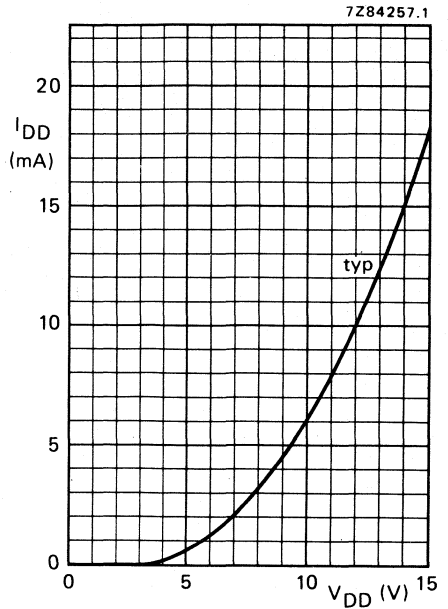


Fig. 14 Supply current as a function of supply voltage.

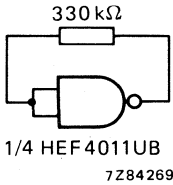


Fig. 15 Test set-up for measuring graphs of Figs 13 and 14. Condition: all other inputs connected to ground.

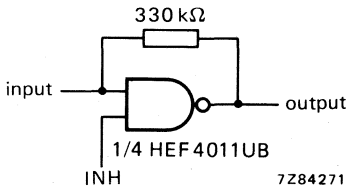


Fig. 16 Example of an analogue amplifier with inhibit using one HEF4011UB gate.

DUAL 4-INPUT NAND GATE



The HEF4012B provides the positive dual 4-input NAND function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

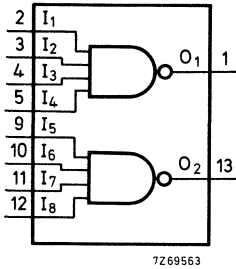


Fig. 1 Functional diagram.

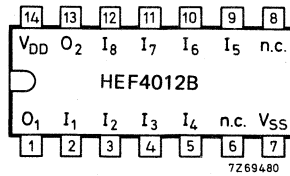


Fig. 2 Pinning diagram.

HEF4012BP: 14-lead DIL; plastic (SOT-27S, T, V).
HEF4012BD: 14-lead DIL; ceramic (SOT-73).
HEF4012BT: 14-lead flat pack; plastic (SO-14; SOT-108A).

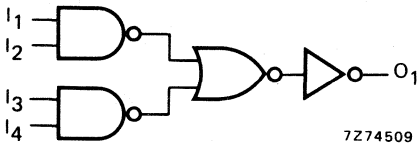


Fig. 3 Logic diagram (one gate).

FAMILY DATA

I_{DD} LIMITS category GATES

see Family Specifications

A.C. CHARACTERISTICS

 $V_{SS} = 0 \text{ V}$; $T_{amb} = 25 \text{ }^\circ\text{C}$; $C_L = 50 \text{ pF}$; input transition times $\leq 20 \text{ ns}$

	V_{DD} V	symbol	typ	max		typical extrapolation formula	
Propagation delays $I_n \rightarrow O_n$ HIGH to LOW	5	t _{PHL}	70	135	ns	$43 \text{ ns} + (0,55 \text{ ns/pF}) C_L$	
	10		25	50	ns	$14 \text{ ns} + (0,23 \text{ ns/pF}) C_L$	
	15		20	35	ns	$12 \text{ ns} + (0,16 \text{ ns/pF}) C_L$	
	LOW to HIGH	5	t _{PLH}	70	140	ns	$43 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
		10		30	60	ns	$19 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
		15		25	50	ns	$17 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
Output transition times HIGH to LOW	5	t _{THL}	60	120	ns	$10 \text{ ns} + (1,0 \text{ ns/pF}) C_L$	
	10		30	60	ns	$9 \text{ ns} + (0,42 \text{ ns/pF}) C_L$	
	15		20	40	ns	$6 \text{ ns} + (0,28 \text{ ns/pF}) C_L$	
	LOW to HIGH	5	t _{TLH}	60	120	ns	$10 \text{ ns} + (1,0 \text{ ns/pF}) C_L$
		10		30	60	ns	$9 \text{ ns} + (0,42 \text{ ns/pF}) C_L$
		15		20	40	ns	$6 \text{ ns} + (0,28 \text{ ns/pF}) C_L$

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$1100 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz)
	10	$4400 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_o = output freq. (MHz)
	15	$12900 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	C_L = load capacitance (pF)
			$\Sigma(f_o C_L)$ = sum of outputs
			V_{DD} = supply voltage (V)

DUAL D-TYPE FLIP-FLOP



The HEF4013B is a dual D-type flip-flop which features independent set direct (S_D), clear direct (C_D), clock inputs (CP) and outputs (O, \bar{O}). Data is accepted when CP is LOW and transferred to the output on the positive-going edge of the clock. The active HIGH asynchronous clear-direct (C_D) and set-direct (S_D) are independent and override the D or CP inputs. The outputs are buffered for best system performance.

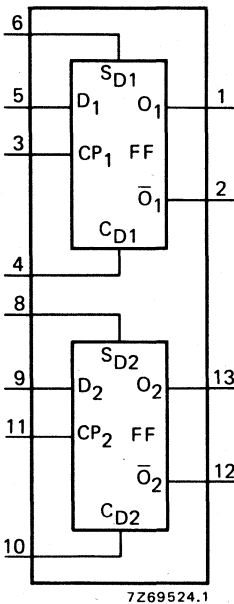


Fig. 1 Functional diagram.

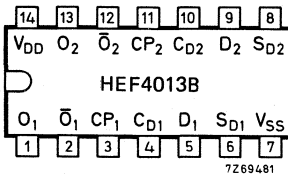


Fig. 2 Pinning diagram.

FUNCTION TABLES

inputs			outputs		
S_D	C_D	CP	D	O	\bar{O}
H	L	X	X	H	L
L	H	X	X	L	H
H	H	X	X	H	H

inputs				outputs	
S_D	C_D	CP	D	O_{n+1}	\bar{O}_{n+1}
L	L	/	L	L	H
L	L	/	H	H	L

- H = HIGH state (the more positive voltage)
- L = LOW state (the less positive voltage)
- X = state is immaterial
- / = positive-going transition
- O_{n+1} = state after clock positive transition

PINNING

- D data inputs
- CP clock input (L to H edge-triggered)
- S_D asynchronous set-direct input (active HIGH)
- C_D asynchronous clear-direct input (active HIGH)
- O true output
- \bar{O} complement output

- HEF4013BP: 14-lead DIL; plastic (SOT-27S, T, V).
- HEF4013BD: 14-lead DIL; ceramic (SOT-73).
- HEF4013BT: 14-lead flat pack; plastic (SO-14; SOT-108A).

FAMILY DATA

I_{DD} LIMITS category FLIP-FLOPS

} see Family Specifications

A.C. CHARACTERISTICS

 $V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	symbol	min.	typ.	max.	typical extrapolation formula	
Propagation delays $CP \rightarrow O, \bar{O}$ HIGH to LOW	5	tPHL		110	220	ns	$83\text{ ns} + (0,55\text{ ns/pF})C_L$
	10		45	90	ns	$34\text{ ns} + (0,23\text{ ns/pF})C_L$	
	15		30	60	ns	$22\text{ ns} + (0,16\text{ ns/pF})C_L$	
	5	tPLH		100	205	ns	$73\text{ ns} + (0,55\text{ ns/pF})C_L$
	10		40	80	ns	$29\text{ ns} + (0,23\text{ ns/pF})C_L$	
	15		30	60	ns	$22\text{ ns} + (0,16\text{ ns/pF})C_L$	
$S_D \rightarrow \bar{O}$ HIGH to LOW	5	tPHL		100	200	ns	$73\text{ ns} + (0,55\text{ ns/pF})C_L$
	10		40	80	ns	$29\text{ ns} + (0,23\text{ ns/pF})C_L$	
	15		30	60	ns	$22\text{ ns} + (0,16\text{ ns/pF})C_L$	
$S_D \rightarrow O$ LOW to HIGH	5	tPLH		135	265	ns	$108\text{ ns} + (0,55\text{ ns/pF})C_L$
	10		50	100	ns	$39\text{ ns} + (0,23\text{ ns/pF})C_L$	
	15		35	70	ns	$27\text{ ns} + (0,16\text{ ns/pF})C_L$	
$C_D \rightarrow O$ HIGH to LOW	5	tPHL		100	200	ns	$73\text{ ns} + (0,55\text{ ns/pF})C_L$
	10		40	80	ns	$29\text{ ns} + (0,23\text{ ns/pF})C_L$	
	15		30	60	ns	$22\text{ ns} + (0,16\text{ ns/pF})C_L$	
$C_D \rightarrow \bar{O}$ LOW to HIGH	5	tPLH		115	225	ns	$88\text{ ns} + (0,55\text{ ns/pF})C_L$
	10		50	95	ns	$39\text{ ns} + (0,23\text{ ns/pF})C_L$	
	15		35	75	ns	$27\text{ ns} + (0,16\text{ ns/pF})C_L$	
Output transition times	5	tTHL		60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF})C_L$
	10		30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF})C_L$	
	15		20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF})C_L$	
	5	tTLH		60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF})C_L$
	10		30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF})C_L$	
	15		20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF})C_L$	

A.C. CHARACTERISTICS

 $V_{SS} = 0 \text{ V}$; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$; $C_L = 50 \text{ pF}$; input transition times $\leq 20 \text{ ns}$

	V_{DD} V	symbol	min.	typ.	max.	
Set-up time D \rightarrow CP	5		60	30	ns	} see also waveforms Figs 4 and 5
	10	t_{su}	30	10	ns	
	15		30	10	ns	
Hold time D \rightarrow CP	5		20	-10	ns	
	10	t_{hold}	20	0	ns	
	15		20	0	ns	
Minimum clock pulse width; LOW	5		85	45	ns	
	10	t_{WCPL}	40	20	ns	
	15		30	15	ns	
Minimum S_D pulse width; HIGH	5		65	35	ns	
	10	t_{WSDH}	35	20	ns	
	15		30	15	ns	
Minimum C_D pulse width; HIGH	5		90	45	ns	
	10	t_{WCDH}	40	20	ns	
	15		35	20	ns	
Recovery time for S_D	5		20	10	ns	
	10	t_{RSD}	15	5	ns	
	15		15	5	ns	
Recovery time for C_D	5		40	25	ns	
	10	t_{RCD}	25	10	ns	
	15		25	10	ns	
Maximum clock pulse frequency	5		6	12	MHz	
	10	f_{max}	12	25	MHz	
	15		18	36	MHz	

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$1\ 050 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz)
	10	$4\ 600 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_o = output freq. (MHz)
	15	$13\ 350 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	C_L = total load cap. (pF)
			$\Sigma(f_o C_L)$ = sum of outputs
			V_{DD} = supply voltage (V)

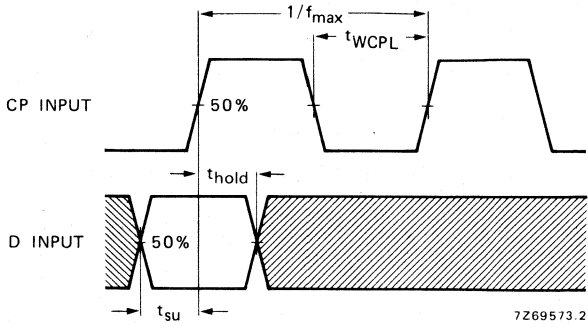


Fig. 4 Waveforms showing set-up times, hold times and minimum clock pulse width. Set-up and hold times are shown as positive values but may be specified as negative values.

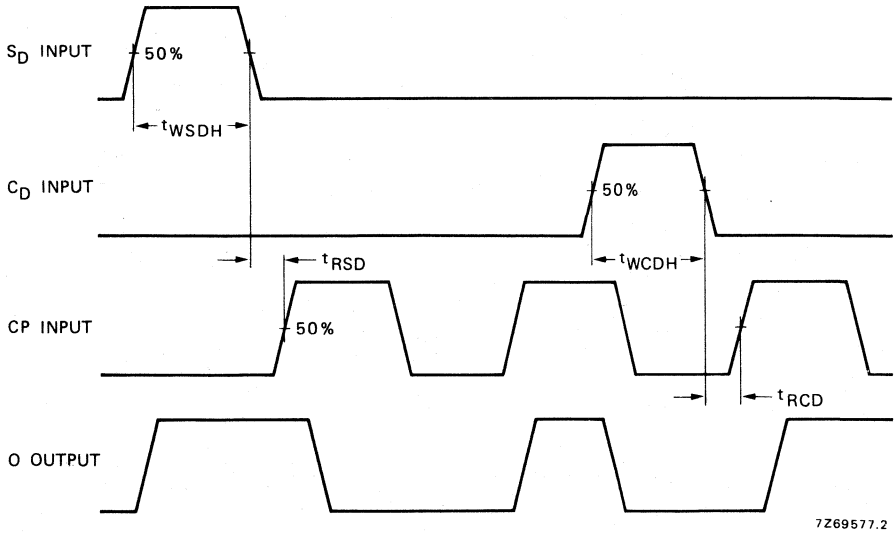


Fig. 5 Waveforms showing recovery times for S_D and C_D; minimum S_D and C_D pulse widths; output \bar{O} connected to D.

APPLICATION INFORMATION

Some examples of applications for the HEF4013B are:

- Counters/dividers
- Registers
- Toggle flip-flops

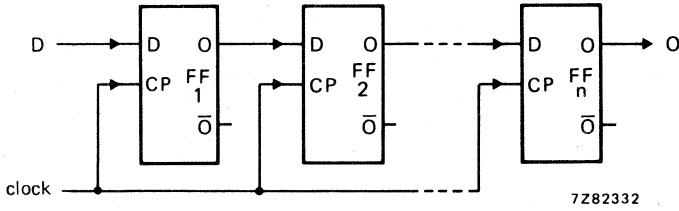


Fig. 6 Typical application of the HEF4013B in an n-stage shift register.

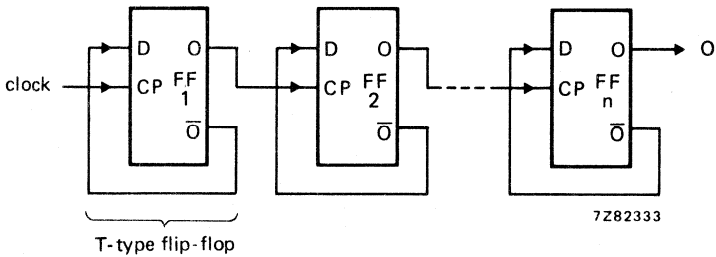


Fig. 7 Typical application of the HEF4013B in a binary ripple up-counter; divide-by- 2^n .

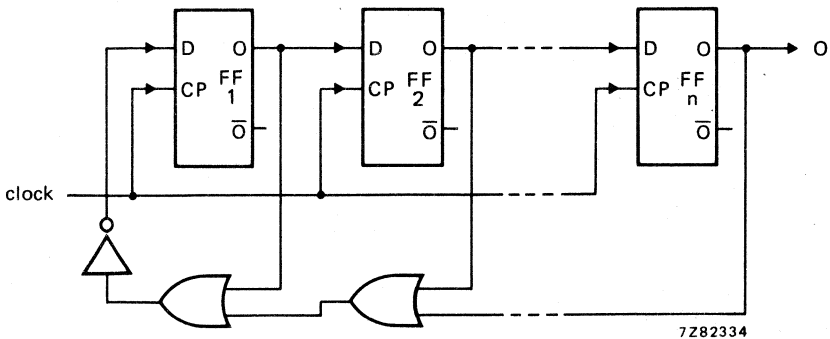


Fig. 8 Typical application of the HEF4013B in a modified ring counter; divide-by-(n + 1).

8-BIT STATIC SHIFT REGISTER



The HEF4014B is a fully synchronous edge-triggered 8-bit static shift register with eight synchronous parallel inputs (P_0 to P_7), a synchronous serial data input (D_S), a synchronous parallel enable input (PE), a LOW to HIGH edge-triggered clock input (CP) and buffered parallel outputs from the last three stages (O_5 to O_7).

Operation is synchronous and the device is edge-triggered on the LOW to HIGH transition of CP. Each register stage is of a D-type master-slave flip-flop. When PE is HIGH, data is loaded into the register from P_0 to P_7 on the LOW to HIGH transition of CP. When PE is LOW, data is shifted to the first position from D_S , and all the data in the register is shifted one position to the right on the LOW to HIGH transition of CP.

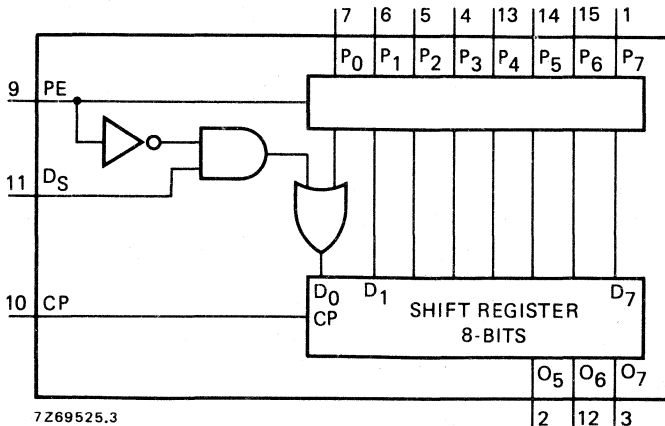


Fig. 1 Functional diagram.

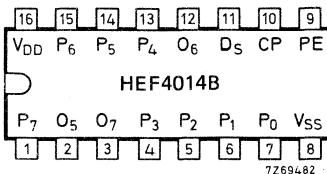


Fig. 2 Pinning diagram.

HEF4014BP: 16-lead DIL; plastic (SOT-38Z).
HEF4014BD: 16-lead DIL; ceramic (SOT-74).
HEF4014BT: 16-lead flat pack; plastic (SO-16; SOT-109A).

FAMILY DATA

I_{DD} LIMITS category MSI

} see Family Specifications

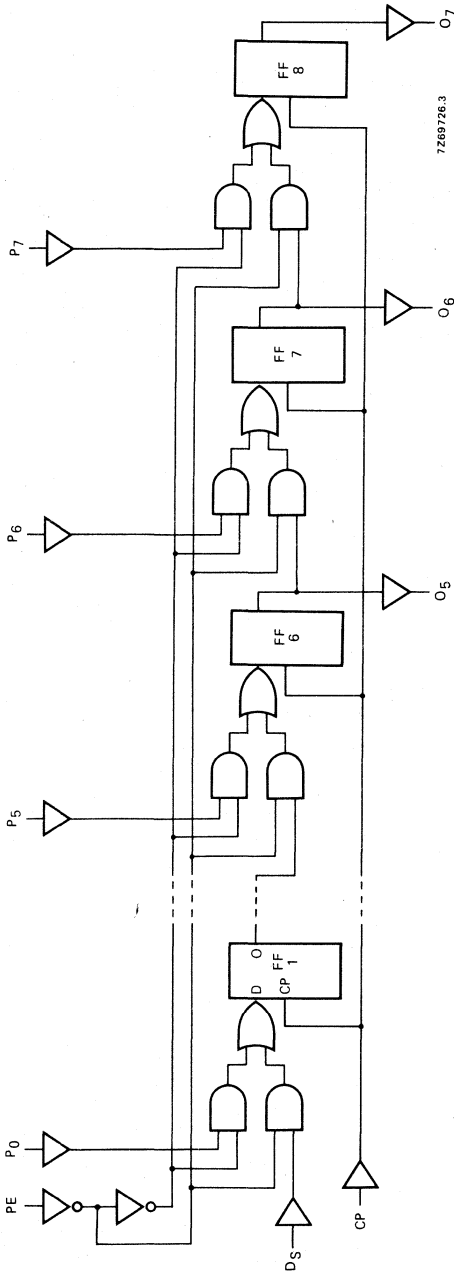


Fig. 3 Logic diagram.

PINNING

- PE parallel enable input
- P₀ to P₇ parallel data inputs
- D_S serial data input
- CP clock input (LOW to HIGH edge-triggered)
- O₅ to O₇ buffered parallel outputs from the last three stages

FUNCTION TABLES

Serial operation

n	inputs			outputs		
	CP	D _S	PE	O ₅	O ₆	O ₇
1	∕	D ₁	L	X	X	X
2	∕	D ₂	L	X	X	X
3	∕	D ₃	L	X	X	X
6	∕	X	L	D ₁	X	X
7	∕	X	L	D ₂	D ₁	X
8	∕	X	L	D ₃	D ₂	D ₁
	∖	X	X	no change		

Parallel operation

n	inputs			outputs		
	CP	D _S	PE	O ₅	O ₆	O ₇
1	∕	X	H	P ₅	P ₆	P ₇
	∖	X	X	no change		

- H = HIGH state (the more positive voltage)
- L = LOW state (the less positive voltage)
- X = state is immaterial
- ∕ = positive-going transition
- ∖ = negative-going transition
- D_n = either HIGH or LOW
- n = number of clock pulse transitions

A.C. CHARACTERISTICS

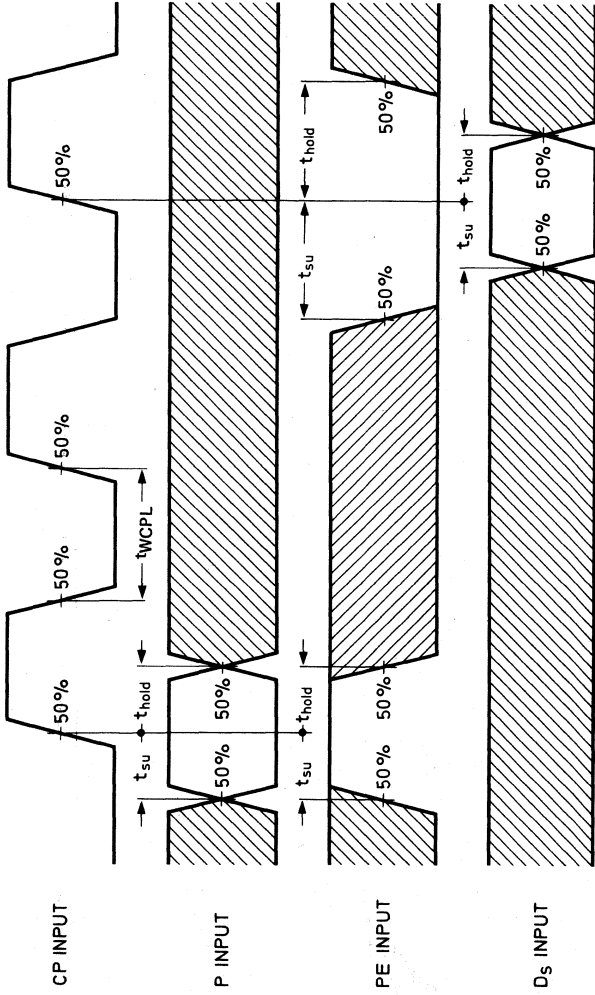
V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V _{DD} V	typical formula for P (μW)	where f _i = input freq. (MHz) f _o = output freq. (MHz) C _L = load cap. (pF) Σ(f _o C _L) = sum of outputs V _{DD} = supply voltage (V)
Dynamic power dissipation per package (P)	5	1 200 f _i + Σ(f _o C _L) × V _{DD} ²	
	10	5 250 f _i + Σ(f _o C _L) × V _{DD} ²	
	15	13 700 f _i + Σ(f _o C _L) × V _{DD} ²	

A.C. CHARACTERISTICS

 $V_{SS} = 0 \text{ V}$; $T_{amb} = 25 \text{ }^\circ\text{C}$; $C_L = 50 \text{ pF}$; input transition times $\leq 20 \text{ ns}$

	V_{DD} V	symbol	min.	typ.	max.	typical extrapolation formula	
Propagation delays							
$C_p \rightarrow O_n$	5			145	290	ns	$118 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
HIGH to LOW	10	t_{PHL}		60	120	ns	$49 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
	15			45	90	ns	$37 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
	5			110	225	ns	$83 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
LOW to HIGH	10	t_{PLH}		50	100	ns	$39 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
	15			40	75	ns	$32 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
Output transition times							
HIGH to LOW	5			60	120	ns	$10 \text{ ns} + (1,0 \text{ ns/pF}) C_L$
	10	t_{THL}		30	60	ns	$9 \text{ ns} + (0,42 \text{ ns/pF}) C_L$
	15			20	40	ns	$6 \text{ ns} + (0,28 \text{ ns/pF}) C_L$
	5			60	120	ns	$10 \text{ ns} + (1,0 \text{ ns/pF}) C_L$
LOW to HIGH	10	t_{TLH}		30	60	ns	$9 \text{ ns} + (0,42 \text{ ns/pF}) C_L$
	15			20	40	ns	$6 \text{ ns} + (0,28 \text{ ns/pF}) C_L$
Set-up times							
$PE \rightarrow CP$	5		180	90		ns	
	10	t_{su}	70	35		ns	
	15		50	25		ns	
	5		110	55		ns	
$D_S \rightarrow CP$	10	t_{su}	40	20		ns	
	15		30	15		ns	
	5		160	80		ns	
$P_n \rightarrow CP$	10	t_{su}	60	30		ns	
	15		40	20		ns	
Hold times							
$PE \rightarrow CP$	5		25	-5		ns	see also waveforms Fig. 4
	10	t_{hold}	20	0		ns	
	15		15	0		ns	
	5		30	15		ns	
$D_S \rightarrow CP$	10	t_{hold}	20	10		ns	
	15		15	7		ns	
	5		30	15		ns	
$P_n \rightarrow CP$	10	t_{hold}	20	10		ns	
	15		15	7		ns	
Minimum clock pulse width; LOW	5		110	55		ns	
	10	t_{WCPL}	45	20		ns	
	15		30	15		ns	
Maximum clock pulse frequency	5		5	9		MHz	
	10	f_{max}	11	22		MHz	
	15		16	32		MHz	



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Fig. 4 Waveforms showing minimum clock pulse width, and set-up and hold times for PE to CP, Ds to CP, and P to CP. Set-up and hold times are shown as positive values but may be specified as negative values.

APPLICATION INFORMATION

Some examples of applications for the HEF4014B are:

- Parallel-to-serial converter
- Serial data queuing
- General purpose register

DUAL 4-BIT STATIC SHIFT REGISTER



The HEF4015B is a dual edge-triggered 4-bit static shift register (serial-to-parallel converter). Each shift register has a serial data input (D), a clock input (CP), four fully buffered parallel outputs (O_0 to O_3) and an overriding asynchronous master reset input (MR). Information present on D is shifted to the first register position, and all the data in the register is shifted one position to the right on the LOW-to-HIGH transition of CP. A HIGH on MR clears the register and forces O_0 to O_3 to LOW, independent of CP and D.

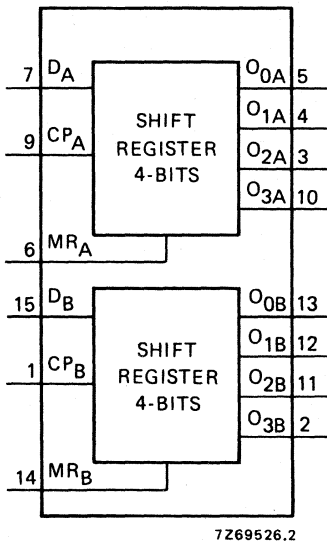


Fig. 1 Functional diagram.



Fig. 2 Pinning diagram.

HEF4015BP: 16-lead DIL; plastic (SOT-38Z).
 HEF4015BD: 16-lead DIL; ceramic (SOT-74).
 HEF4015BT: 16-lead flat pack; plastic (SO-16; SOT-109A).

PINNING

D_A, D_B serial data input
 MR_A, MR_B master reset input (active HIGH)
 CP_A, CP_B clock input (LOW-to-HIGH edge-triggered)
 $O_{0A}, O_{1A}, O_{2A}, O_{3A}$ parallel outputs
 $O_{0B}, O_{1B}, O_{2B}, O_{3B}$ parallel outputs

APPLICATION INFORMATION

Some examples of applications for the HEF4015B are:

- Serial-to-parallel converter
- Buffer stores
- General purpose register

FAMILY DATA

I_{DD} LIMITS category MSI

} see Family Specifications

A.C. CHARACTERISTICS

 $V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	symbol	min.	typ.	max.	typical extrapolation formula	
Propagation delays CP \rightarrow O_n HIGH to LOW	5	t_{PHL}		145	290	ns	$118\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10		60	120	ns	$49\text{ ns} + (0,23\text{ ns/pF}) C_L$	
	15		40	80	ns	$32\text{ ns} + (0,16\text{ ns/pF}) C_L$	
	5		120	240	ns	$93\text{ ns} + (0,55\text{ ns/pF}) C_L$	
	10		55	110	ns	$44\text{ ns} + (0,23\text{ ns/pF}) C_L$	
	15		40	75	ns	$32\text{ ns} + (0,16\text{ ns/pF}) C_L$	
LOW to HIGH	5	t_{PLH}		120	240	ns	$93\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10		55	110	ns	$44\text{ ns} + (0,23\text{ ns/pF}) C_L$	
	15		40	75	ns	$32\text{ ns} + (0,16\text{ ns/pF}) C_L$	
	5		185	370	ns	$158\text{ ns} + (0,55\text{ ns/pF}) C_L$	
	10		70	140	ns	$59\text{ ns} + (0,23\text{ ns/pF}) C_L$	
	15		40	85	ns	$32\text{ ns} + (0,16\text{ ns/pF}) C_L$	
Output transition times HIGH to LOW	5	t_{THL}		60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$
	10		30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$	
	15		20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$	
	5		60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$	
	10		30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$	
	15		20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$	
Set-up time D \rightarrow CP	5	t_{su}	110	55	ns	see waveforms Figs 4 and 5	
	10		30	15	ns		
	15		20	10	ns		
Hold time D \rightarrow CP	5	t_{hold}	40	20	ns	see waveforms Figs 4 and 5	
	10		20	10	ns		
	15		15	8	ns		
Minimum clock pulse width; LOW	5	t_{WCPL}	100	50	ns	see waveforms Figs 4 and 5	
	10		35	20	ns		
	15		30	15	ns		
Minimum MR pulse width; HIGH	5	t_{WMRH}	110	55	ns	see waveforms Figs 4 and 5	
	10		35	20	ns		
	15		30	15	ns		
Recovery time for MR	5	t_{RMR}	110	65	ns	see waveforms Figs 4 and 5	
	10		40	20	ns		
	15		25	15	ns		
Maximum clock pulse frequency	5	f_{max}	4	9	MHz	see waveforms Figs 4 and 5	
	10		12	23	MHz		
	15		17	34	MHz		
	V_{DD} V	typical formula for P (μW)	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)				
Dynamic power dissipation per package (P)	5	$1\,500 f_i + \Sigma(f_o C_L) \times V_{DD}^2$					
	10		$7\,800 f_i + \Sigma(f_o C_L) \times V_{DD}^2$				
	15			$26\,100 f_i + \Sigma(f_o C_L) \times V_{DD}^2$			

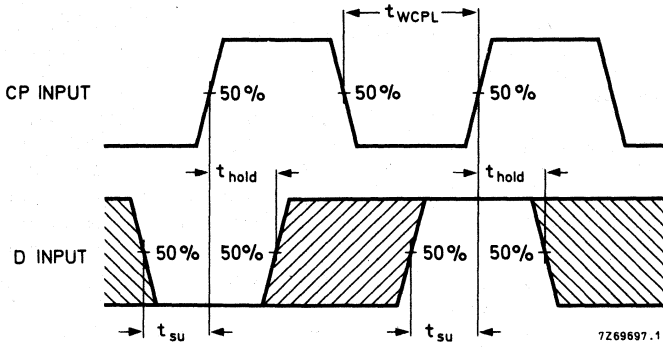


Fig. 4 Waveforms showing set-up times, hold times and minimum clock pulse width. Set-up and hold times are shown as positive values but may be specified as negative values.

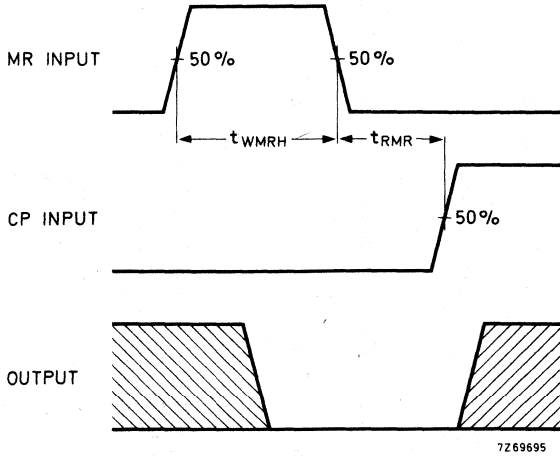
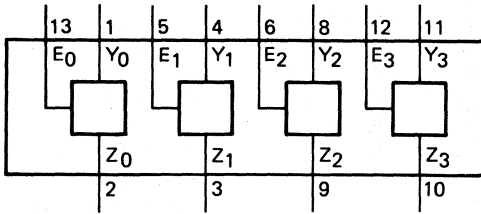


Fig. 5 Waveforms showing recovery time for MR and minimum MR pulse width.

QUADRUPLE BILATERAL SWITCHES

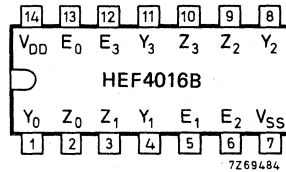


The HEF4016B has four independent analogue switches (transmission gates). Each switch has two input/output terminals (Y/Z) and an active HIGH enable input (E). When E is connected to V_{DD} a low impedance bidirectional path between Y and Z is established (ON condition). When E is connected to V_{SS} the switch is disabled and a high impedance between Y and Z is established (OFF condition). Current through a switch will not cause additional V_{DD} current provided the voltage at the terminals of the switch is maintained within the supply voltage range; $V_{DD} \geq (V_Y, V_Z) \geq V_{SS}$. Inputs Y and Z are electrically equivalent terminals.



7269571.2

Fig. 1 Functional diagram.



7269484

Fig. 2 Pinning diagram.

HEF4016BP: 14-lead DIL: plastic (SOT-27S,T,V).
HEF4016BD: 14-lead DIL: ceramic (SOT-73).
HEF4016BT: 14-lead flat pack; plastic (SO-14; SOT-108A).

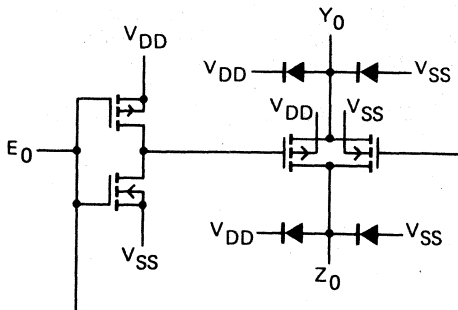
PINNING

E_0 to E_3 enable inputs
 Y_0 to Y_3 input/output terminals
 Z_0 to Z_3 input/output terminals

APPLICATION INFORMATION

Some examples of applications for the HEF4016B are:

- Signal gating
- Modulation
- Demodulation
- Chopper



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Fig. 3 Schematic diagram (one switch).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Power dissipation per switch

P max. 100 mW

For other RATINGS see Family Specifications

D.C. CHARACTERISTICS

T_{amb} = 25 °C

	V _{DD} V	symbol	typ.	max.		conditions
ON resistance	5	R _{ON}	8000	—	Ω	} E _n at V _{DD} V _{is} = V _{SS} to V _{DD} see Fig. 4
	10		230	690	Ω	
	15		115	350	Ω	
ON resistance	5	R _{ON}	140	425	Ω	} E _n at V _{DD} V _{is} = V _{SS} see Fig. 4
	10		65	195	Ω	
	15		50	145	Ω	
ON resistance	5	R _{ON}	170	515	Ω	} E _n at V _{DD} V _{is} = V _{DD} see Fig. 4
	10		95	285	Ω	
	15		75	220	Ω	
'Δ' ON resistance between any two channels	5	ΔR _{ON}	—	—	Ω	} E _n at V _{DD} V _{is} = V _{SS} to V _{DD} see Fig. 4
	10		15	—	Ω	
	15		10	—	Ω	
OFF-state leakage current, any channel OFF	5	I _{OZ}	—	—	nA	} E _n at V _{SS}
	10		—	—	nA	
	15		—	200	nA	
E _n input voltage LOW	5	V _{IL}	1,5	—	V	} I _{is} = 10 μA see Fig. 9
	10		1,5	—	V	
	15		1,5	—	V	

	V _{DD} V	symbol	T _{amb} (°C)			conditions
			—40 max.	+ 25 max.	+ 85 max.	
Quiescent device current	5	I _{DD}	1,0	1,0	7,5 μA	} V _{SS} = 0; all valid input combinations; V _I = V _{SS} or V _{DD}
	10		2,0	2,0	15,0 μA	
	15		4,0	4,0	30,0 μA	
Input leakage current at E _n	15	± I _{IN}	—	300	1000 nA	E _n at V _{SS} or V _{DD}

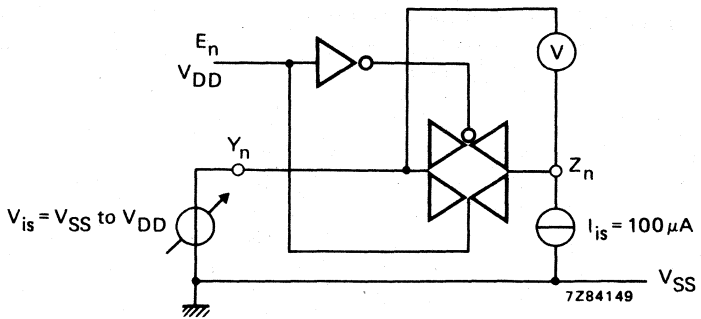


Fig. 4 Test set-up for measuring R_{ON} .

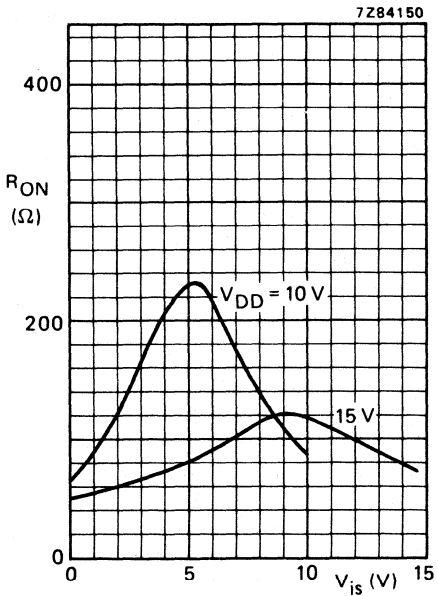


Fig. 5 Typical R_{ON} as a function of input voltage.

E_n at V_{DD}
 $I_{is} = 100 \mu A$
 $V_{SS} = 0 V$

A.C. CHARACTERISTICS

 $V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	symbol	typ.	max.		
Propagation delays $V_{is} \rightarrow V_{os}$ HIGH to LOW	5	tPHL	25	50	ns	} note 1
	10		10	20	ns	
	15		5	10	ns	
LOW to HIGH	5	tPLH	20	40	ns	} note 1
	10		10	20	ns	
	15		5	10	ns	
Output disable times $E_n \rightarrow V_{os}$ HIGH	5	tPHZ	95	190	ns	} note 2
	10		85	170	ns	
	15		85	170	ns	
LOW	5	tPLZ	50	100	ns	} note 2
	10		55	110	ns	
	15		60	120	ns	
Output enable times $E_n \rightarrow V_{os}$ HIGH	5	tpZH	35	70	ns	} note 2
	10		20	40	ns	
	15		15	30	ns	
LOW	5	tpZL	35	70	ns	} note 2
	10		15	30	ns	
	15		10	20	ns	
Distortion, sine-wave response	5		—		%	} note 3
	10		0,08		%	
	15		0,04		%	
Crosstalk between any two channels	5		—		MHz	} note 4
	10		1		MHz	
	15		—		MHz	
Crosstalk; enable input to output	5		—		mV	} note 5
	10		50		mV	
	15		—		mV	
OFF-state feed-through	5		—		MHz	} note 6
	10		1		MHz	
	15		—		MHz	
ON-state frequency response	5		—		MHz	} note 7
	10		90		MHz	
	15		—		MHz	

	V_{DD} V	typical formula for P (μW)	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
Dynamic power dissipation per package (P)	5	$200 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	10	$1100 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$3500 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

NOTES

V_{is} is the input voltage at a Y or Z terminal, whichever is assigned as input.

V_{os} is the output voltage at a Y or Z terminal, whichever is assigned as output.

1. $R_L = 10\text{ k}\Omega$ to V_{SS} ; $C_L = 50\text{ pF}$ to V_{SS} ; $E_n = V_{DD}$; $V_{is} = V_{DD}$ (square-wave); see Figs 6 and 10.

2. $R_L = 10\text{ k}\Omega$; $C_L = 50\text{ pF}$ to V_{SS} ; $E_n = V_{DD}$ (square-wave);

$V_{is} = V_{DD}$ and R_L to V_{SS} for tp_{HZ} and tp_{ZH} ;

$V_{is} = V_{SS}$ and R_L to V_{DD} for tp_{LZ} and tp_{ZL} ; see Figs 6 and 11.

3. $R_L = 10\text{ k}\Omega$; $C_L = 15\text{ pF}$; $E_n = V_{DD}$; $V_{is} = \frac{1}{2}V_{DD(p-p)}$ (sine-wave, symmetrical about $\frac{1}{2}V_{DD}$);

$f_{is} = 1\text{ kHz}$; see Fig. 7.

4. $R_L = 1\text{ k}\Omega$; $V_{is} = \frac{1}{2}V_{DD(p-p)}$ (sine-wave, symmetrical about $\frac{1}{2}V_{DD}$);

$20\log\frac{V_{os}(B)}{V_{is}(A)} = 50\text{ dB}$; $E_n(A) = V_{SS}$; $E_n(B) = V_{DD}$; see Fig. 8.

5. $R_L = 10\text{ k}\Omega$ to V_{SS} ; $C_L = 15\text{ pF}$ to V_{SS} ; $E_n = V_{DD}$ (square-wave); crosstalk is $|V_{os}|$ (peak value); see Fig. 6.

6. $R_L = 1\text{ k}\Omega$; $C_L = 5\text{ pF}$; $E_n = V_{SS}$; $V_{is} = \frac{1}{2}V_{DD(p-p)}$ (sine-wave, symmetrical about $\frac{1}{2}V_{DD}$);

$20\log\frac{V_{os}}{V_{is}} = 50\text{ dB}$; see Fig. 7.

7. $R_L = 1\text{ k}\Omega$; $C_L = 5\text{ pF}$; $E_n = V_{DD}$; $V_{is} = \frac{1}{2}V_{DD(p-p)}$ (sine-wave, symmetrical about $\frac{1}{2}V_{DD}$);

$20\log\frac{V_{os}}{V_{is}} = -3\text{ dB}$; see Fig. 7.



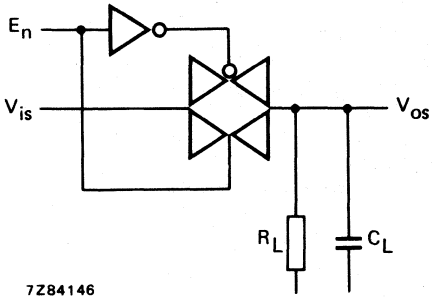


Fig. 6.

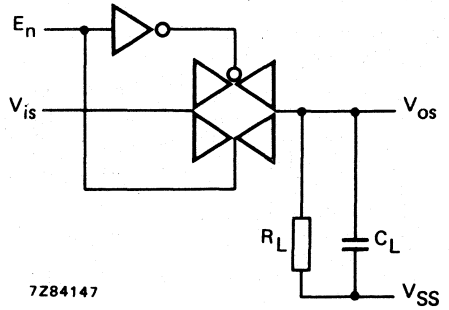


Fig. 7.

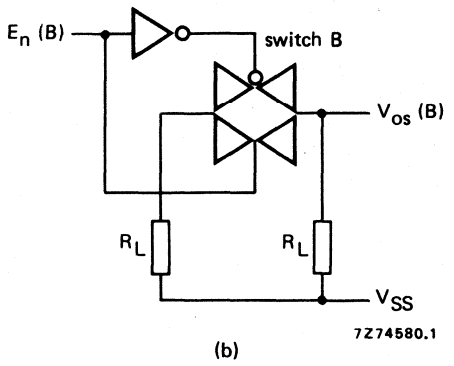
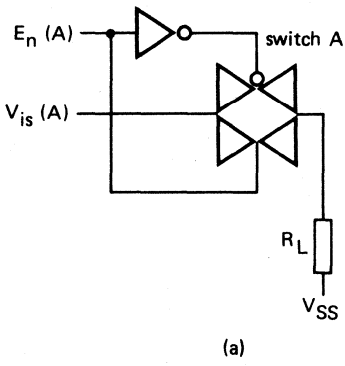


Fig. 8.

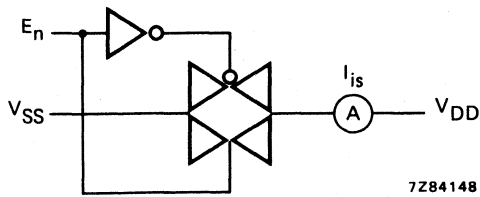


Fig. 9.

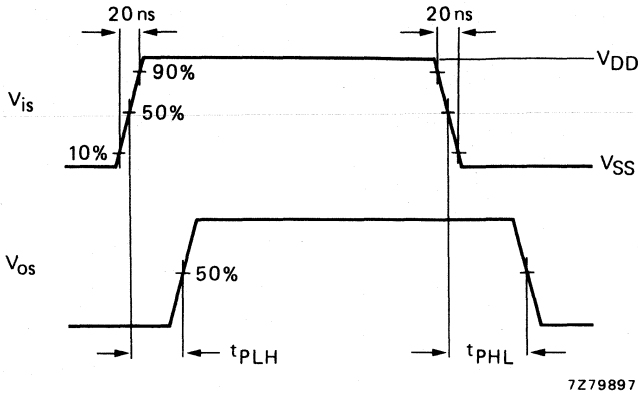
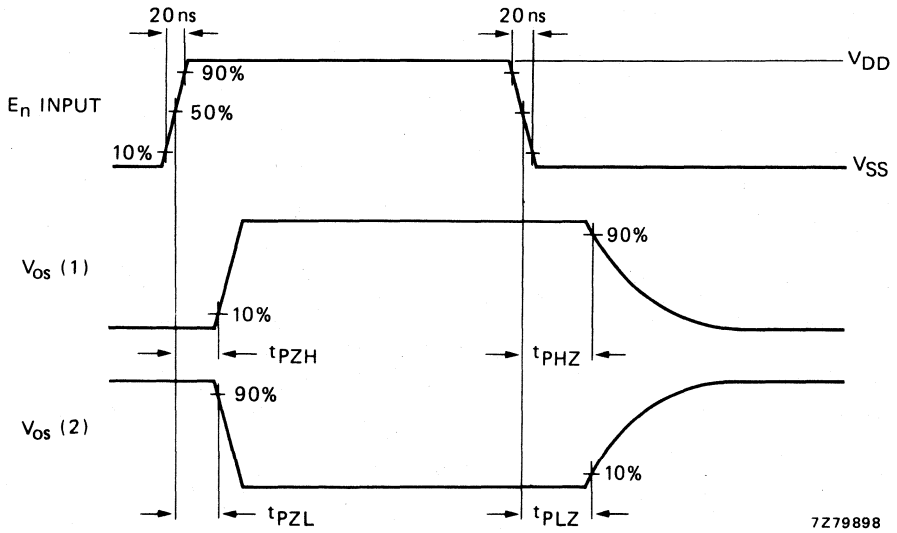


Fig. 10 Waveforms showing propagation delays from V_{is} to V_{os} .



(1) V_{is} at V_{DD} ; (2) V_{is} at V_{SS} .

Fig. 11 Waveforms showing output disable and enable times.

5-STAGE JOHNSON COUNTER



The HEF4017B is a 5-stage Johnson decade counter with ten spike-free decoded active HIGH outputs (O_0 to O_9), an active LOW output from the most significant flip-flop (\bar{O}_{5-9}), active HIGH and active LOW clock inputs (CP_0 , \bar{CP}_1) and an overriding asynchronous master reset input (MR).

The counter is advanced by either a LOW to HIGH transition at CP_0 while \bar{CP}_1 is LOW or a HIGH to LOW transition at \bar{CP}_1 while CP_0 is HIGH (see also function table).

When cascading counters, the \bar{O}_{5-9} output, which is LOW while the counter is in states 5, 6, 7, 8 and 9, can be used to drive the CP_0 input of the next counter.

A HIGH on MR resets the counter to zero ($O_0 = \bar{O}_{5-9} = \text{HIGH}$; O_1 to $O_9 = \text{LOW}$) independent of the clock inputs (CP_0 , \bar{CP}_1).

Automatic code correction of the counter is provided by an internal circuit: following any illegal code the counter returns to a proper counting mode within 11 clock pulses.

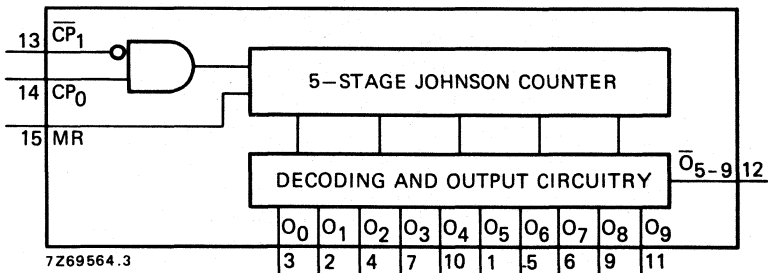


Fig. 1 Functional diagram.

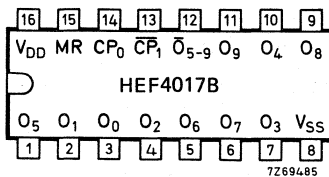


Fig. 2 Pinning diagram.

HEF4017BP: 16-lead DIL; plastic (SOT-38Z).

HEF4017BD: 16-lead DIL; ceramic (SOT-74).

HEF4017BT: 16-lead flat pack; plastic (SO-16; SOT-109A).

PINNING

CP_0	clock input (LOW to HIGH triggered)
\bar{CP}_1	clock input (HIGH to LOW triggered)
MR	master reset input
O_0 to O_9	decoded outputs
\bar{O}_{5-9}	carry output (active LOW)

FAMILY DATA

IDD LIMITS category MSI

} see Family Specifications

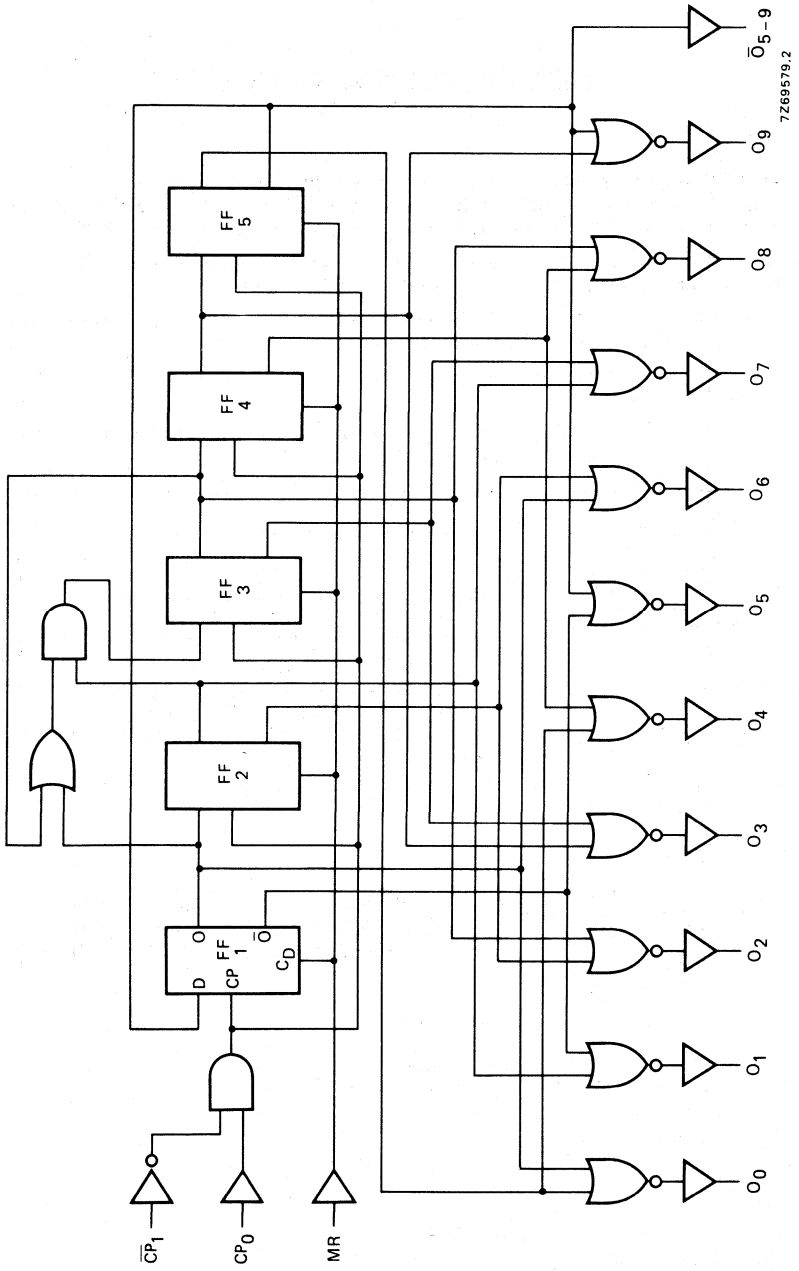


Fig. 3 Logic diagram.

FUNCTION TABLE

MR	CP ₀	\overline{CP}_1	operation
H	X	X	$O_0 = \overline{O}_{5-9} = H$; O_1 to $O_9 = L$
L	H	\searrow	Counter advances
L	\swarrow	L	Counter advances
L	L	X	No change
L	X	H	No change
L	H	\swarrow	No change
L	\searrow	L	No change

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

X = state is immaterial

 \swarrow = positive-going transition \searrow = negative-going transition

A.C. CHARACTERISTICS

 $V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^\circ\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	symbol	min.	typ.	max.	typical extrapolation formula	
Propagation delays $CP_0, \overline{CP}_1 \rightarrow O_0$ to O_9 HIGH to LOW	5			195	390	ns	$168\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10	t_{PHL}		75	145	ns	$64\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			50	100	ns	$42\text{ ns} + (0,16\text{ ns/pF}) C_L$
LOW to HIGH	5			245	485	ns	$218\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10	t_{PLH}		95	195	ns	$84\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			60	125	ns	$52\text{ ns} + (0,16\text{ ns/pF}) C_L$
$CP_0, \overline{CP}_1 \rightarrow \overline{O}_{5-9}$ HIGH to LOW	5			245	485	ns	$218\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10	t_{PHL}		90	185	ns	$79\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			60	120	ns	$52\text{ ns} + (0,16\text{ ns/pF}) C_L$
LOW to HIGH	5			190	380	ns	$163\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10	t_{PLH}		75	145	ns	$64\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			50	105	ns	$42\text{ ns} + (0,16\text{ ns/pF}) C_L$
MR $\rightarrow O_1$ to O_9 HIGH to LOW	5			130	260	ns	$103\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10	t_{PHL}		55	105	ns	$44\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			40	75	ns	$32\text{ ns} + (0,16\text{ ns/pF}) C_L$
MR $\rightarrow \overline{O}_{5-9}$ LOW to HIGH	5			110	220	ns	$83\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10	t_{PLH}		45	90	ns	$34\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			35	70	ns	$27\text{ ns} + (0,16\text{ ns/pF}) C_L$
MR $\rightarrow O_0$ LOW to HIGH	5			130	260	ns	$103\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10	t_{PLH}		55	105	ns	$44\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			40	75	ns	$32\text{ ns} + (0,16\text{ ns/pF}) C_L$
Output transition times HIGH to LOW	5			60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$
	10	t_{THL}		30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$
	15			20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$
LOW to HIGH	5			60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$
	10	t_{TLH}		30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$
	15			20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$

A.C. CHARACTERISTICS

 $V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	symbol	min.	typ.	max.	
Hold times $CP_0 \rightarrow \overline{CP}_1$	5	t_{hold}	140	70	ns	see also waveforms Figs 4 and 5
	10		50	25	ns	
	15		30	15	ns	
$\overline{CP}_1 \rightarrow CP_0$	5	t_{hold}	170	85	ns	
	10		60	30	ns	
	15		40	20	ns	
Minimum clock pulse width	5	t_{WCP}	75	35	ns	
	10		30	15	ns	
	15		20	10	ns	
Minimum MR pulse width; HIGH	5	t_{WMRH}	70	35	ns	
	10		30	15	ns	
	15		20	10	ns	
Recovery time for MR	5	t_{RMR}	50	25	ns	
	10		25	10	ns	
	15		20	10	ns	
Maximum clock pulse frequency	5	f_{max}	3	6	MHz	
	10		8	16	MHz	
	15		12	24	MHz	

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$475 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz)
	10	$2400 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_o = output freq. (MHz)
	15	$6525 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	C_L = load cap. (pF)
			$\Sigma(f_o C_L)$ = sum of outputs
			V_{DD} = supply voltage (V)

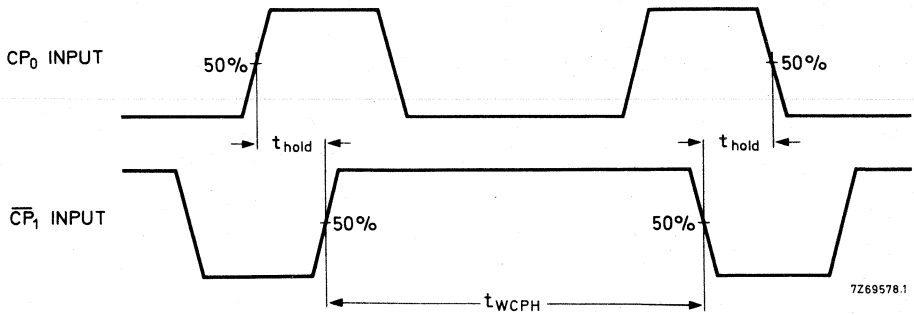


Fig. 4 Waveforms showing hold times for CP₀ to \overline{CP}_1 and \overline{CP}_1 to CP₀. Hold times are shown as positive values, but may be specified as negative values.

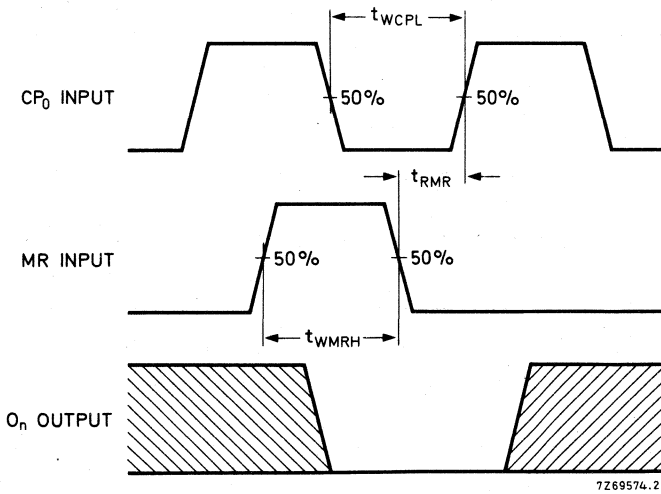


Fig. 5 Waveforms showing recovery time for MR; minimum CP₀ and MR pulse widths. Conditions: $\overline{CP}_1 = \text{LOW}$ while CP₀ is triggered on a LOW to HIGH transition. t_{WCP} and t_{RMR} also apply when CP₀ = HIGH and \overline{CP}_1 is triggered on a HIGH to LOW transition.

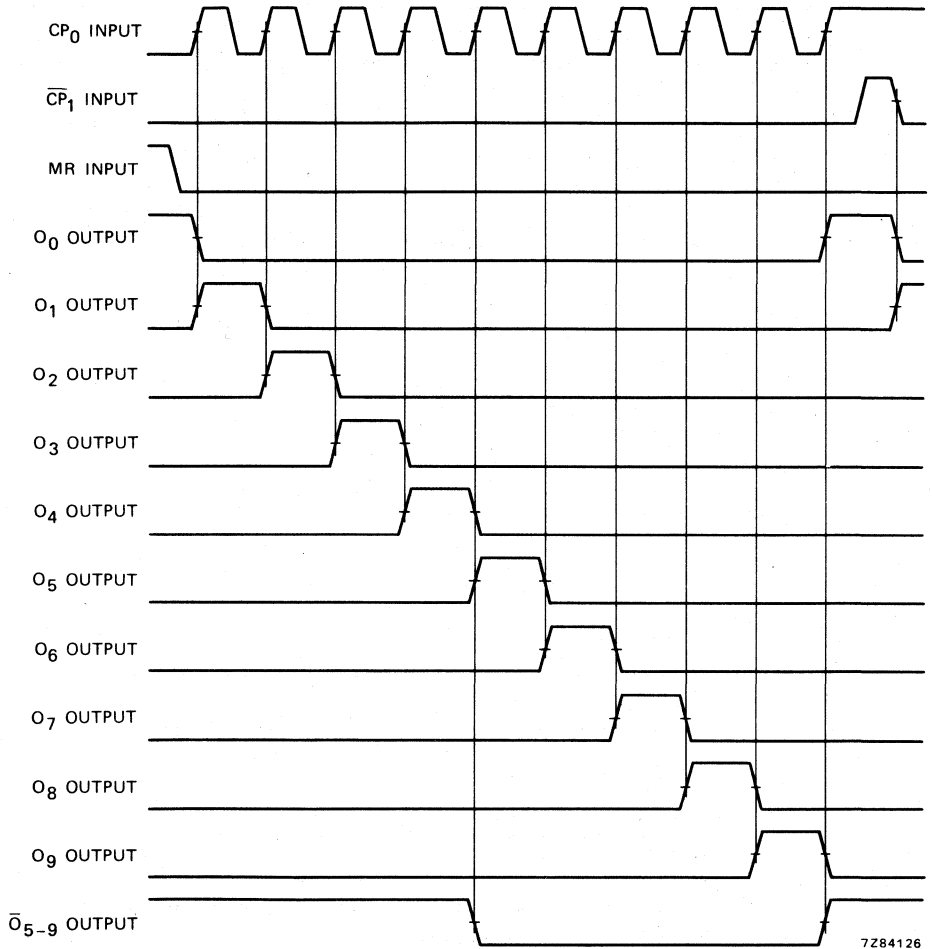


Fig. 6 Timing diagram.

APPLICATION INFORMATION

Some examples of applications for the HEF4017B are:

- Decade counter with decimal decoding
- 1 out of n decoding counter (when cascaded)
- Sequential controller
- Timer.

Figure 7 shows a technique for extending the number of decoded output states for the HEF4017B. Decoded outputs are sequential within each stage and from stage to stage, with no dead time (except propagation delay).

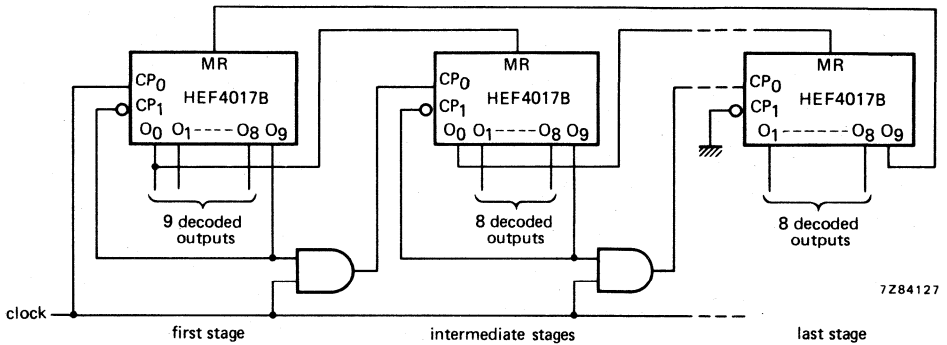


Fig. 7 Counter expansion.

Note

It is essential not to enable the counter on \overline{CP}_1 when CP₀ is HIGH, or on CP₀ when \overline{CP}_1 is LOW, as this would cause an extra count.

PRESETTABLE DIVIDE-BY-N COUNTER



The HEF4018B is a 5-stage Johnson counter with a clock input (CP), a data input (D), an asynchronous parallel load input (PL), five parallel inputs (P_0 to P_4), five active LOW buffered outputs (\bar{O}_0 to \bar{O}_4), and an overriding asynchronous master reset input (MR). Information on P_0 to P_4 is asynchronously loaded into the counter while PL is HIGH, independent of CP and D inputs. When P_L is LOW, the counter advances on the LOW to HIGH transition of CP. By connecting \bar{O}_0 to \bar{O}_4 to D, the counter operates as a divide-by-n counter ($n = 2$ to 10 ; see also function selection below). Each register stage is a D-type master-slave flip-flop with a set-direct/clear-direct input. An internal code correction circuit provides automatic code correction of the counter. From any illegal code the counter is in a proper counting mode within 11 clock pulses. A HIGH on MR resets the counter (\bar{O}_0 to $\bar{O}_4 = \text{HIGH}$) independent of all other inputs.

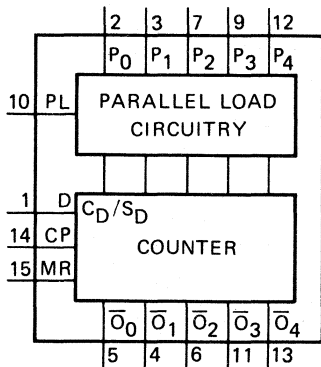


Fig. 1 Functional diagram.

FUNCTION SELECTION

counter mode; divide by	connect D input to	remarks
10 8 6 4 2	\bar{O}_4 \bar{O}_3 \bar{O}_2 \bar{O}_1 O_0	no external components needed
9 7 5 3	$\bar{O}_3 \cdot \bar{O}_4$ $\bar{O}_2 \cdot \bar{O}_3$ $\bar{O}_1 \cdot \bar{O}_2$ $O_0 \cdot O_1$	AND gate needed; counter skips all HIGH states

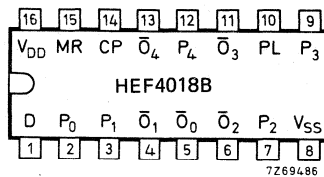


Fig. 2 Pinning diagram.

HEF4018BP: 16-lead DIL; plastic (SOT-38Z).
HEF4018BD: 16-lead DIL; ceramic (SOT-74).
HEF4018BT: 16-lead flat pack; plastic (SO-16; SOT-109A).

PINNING

- PL parallel load input
- P_0 to P_4 parallel inputs
- D data input
- CP clock input (LOW to HIGH edge triggered)
- MR master reset input
- \bar{O}_0 to \bar{O}_4 buffered output (active LOW)

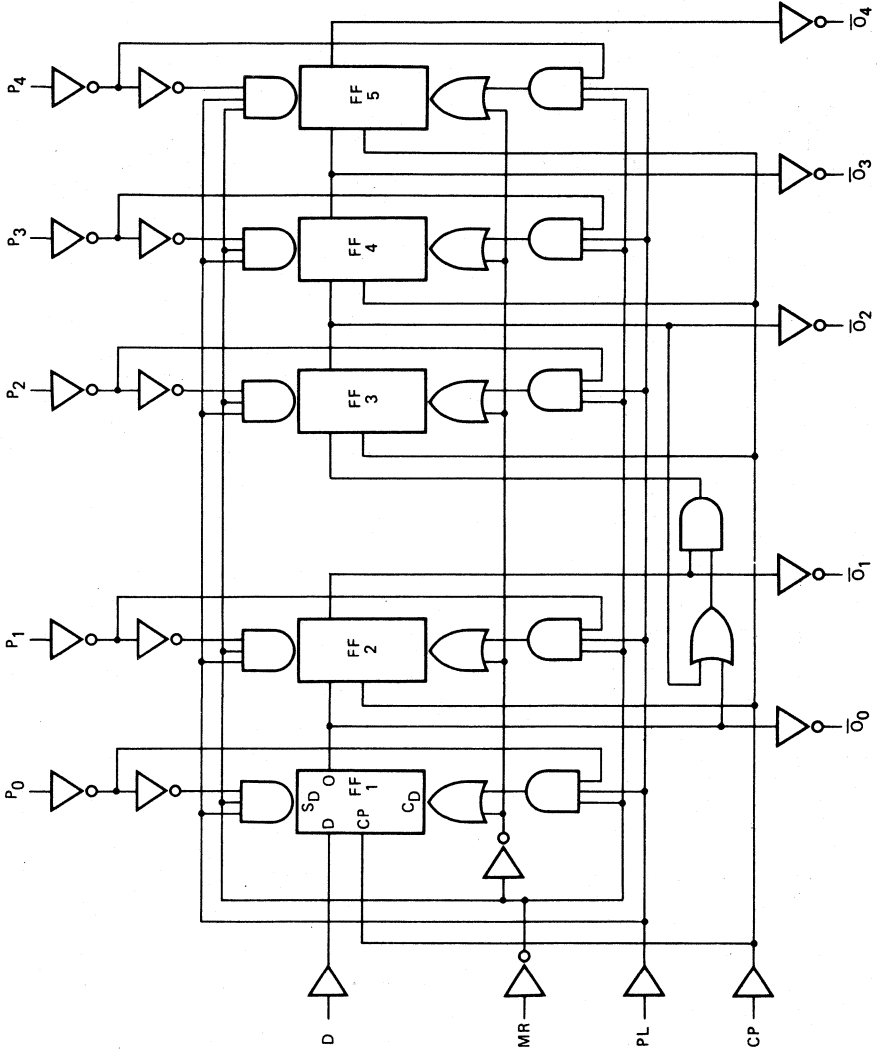
APPLICATION INFORMATION

Some examples of applications for the HEF4018B are:

- Programmable divide-by-n counter
- Programmable frequency division
- Timers

FAMILY DATA

I_{DD} LIMITS category MSI } see Family Specifications



7269821.2

Fig. 3 Logic diagram.

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ≤ 20 ns

	V _{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$700 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f _i = input freq. (MHz)
	10	$3450 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f _o = output freq. (MHz)
	15	$10300 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	C _L = load capacitance (pF)
			Σ(f _o C _L) = sum of outputs
			V _{DD} = supply voltage (V)

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V _{DD} V	symbol	min.	typ.	max.	typical extrapolation formula	
Propagation delays CP → \bar{O} HIGH to LOW	5	t _{PHL}		185	370	ns	158 ns + (0,55 ns/pF) C _L
	10		65	135	ns	54 ns + (0,23 ns/pF) C _L	
	15		50	95	ns	42 ns + (0,16 ns/pF) C _L	
LOW to HIGH	5	t _{PLH}		145	295	ns	118 ns + (0,55 ns/pF) C _L
	10		55	110	ns	44 ns + (0,23 ns/pF) C _L	
	15		40	85	ns	32 ns + (0,16 ns/pF) C _L	
PL → \bar{O} HIGH to LOW	5	t _{PHL}		205	415	ns	178 ns + (0,55 ns/pF) C _L
	10		70	140	ns	59 ns + (0,23 ns/pF) C _L	
	15		50	105	ns	42 ns + (0,16 ns/pF) C _L	
LOW to HIGH	5	t _{PLH}		175	350	ns	148 ns + (0,55 ns/pF) C _L
	10		65	125	ns	54 ns + (0,23 ns/pF) C _L	
	15		50	95	ns	42 ns + (0,16 ns/pF) C _L	
MR → \bar{O} LOW to HIGH	5	t _{PLH}		140	280	ns	113 ns + (0,55 ns/pF) C _L
	10		55	105	ns	44 ns + (0,23 ns/pF) C _L	
	15		40	80	ns	32 ns + (0,16 ns/pF) C _L	
Output transition times HIGH to LOW	5	t _{THL}		60	120	ns	10 ns + (1,0 ns/pF) C _L
	10		30	60	ns	9 ns + (0,42 ns/pF) C _L	
	15		20	40	ns	6 ns + (0,28 ns/pF) C _L	
LOW to HIGH	5	t _{TLH}		60	120	ns	10 ns + (1,0 ns/pF) C _L
	10		30	60	ns	9 ns + (0,42 ns/pF) C _L	
	15		20	40	ns	6 ns + (0,28 ns/pF) C _L	

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V _{DD} V	symbol	min.	typ.	max.	typical extrapolation formula
Set-up time D → CP	5	t _{su}	130	65	ns	see also waveforms Figs 4, 5 and 6
	10		40	20	ns	
	15		30	15	ns	
Hold time D → CP	5	t _{hold}	20	-45	ns	
	10		5	-15	ns	
	15		5	-10	ns	
Minimum clock pulse width; LOW	5	t _{WCPL}	140	70	ns	
	10		50	25	ns	
	15		40	20	ns	
Minimum MR pulse width; HIGH	5	t _{WMRH}	100	50	ns	
	10		35	20	ns	
	15		25	15	ns	
Minimum PL pulse width; HIGH	5	t _{WPLH}	145	75	ns	
	10		50	25	ns	
	15		35	20	ns	
Recovery time for MR	5	t _{RMR}	135	70	ns	
	10		40	20	ns	
	15		25	15	ns	
Recovery time for PL	5	t _{RPL}	170	85	ns	
	10		55	30	ns	
	15		40	20	ns	
Maximum clock pulse frequency	5	f _{max}	2	4	MHz	
	10		6	11	MHz	
	15		8	16	MHz	

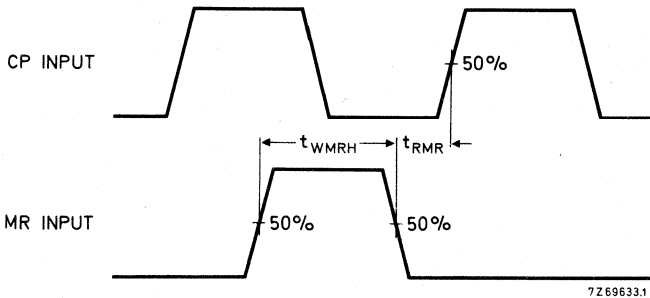


Fig. 4 Waveforms showing minimum MR pulse width and MR recovery time.

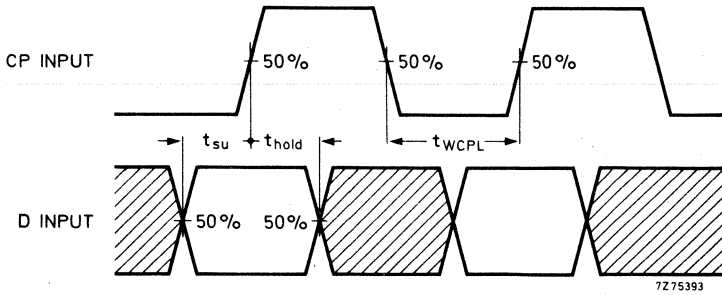


Fig. 5 Waveforms showing minimum clock pulse width, set-up time and hold time for CP and D.

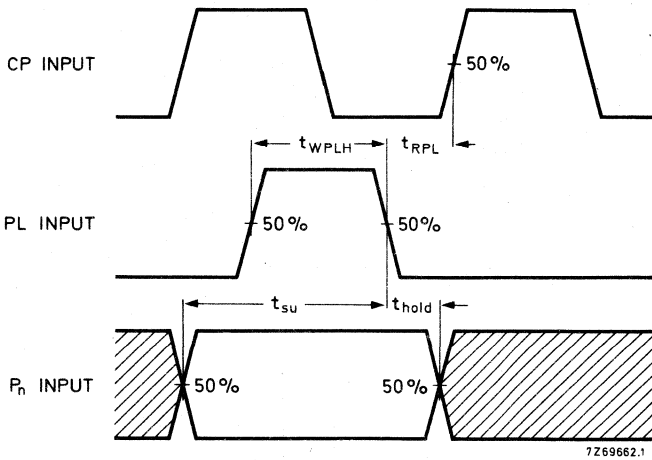


Fig. 6 Waveforms showing minimum PL pulse width, recovery time for PL, and set-up and hold times for P_n to PL. Set-up and hold times are shown as positive values but may be specified as negative values.

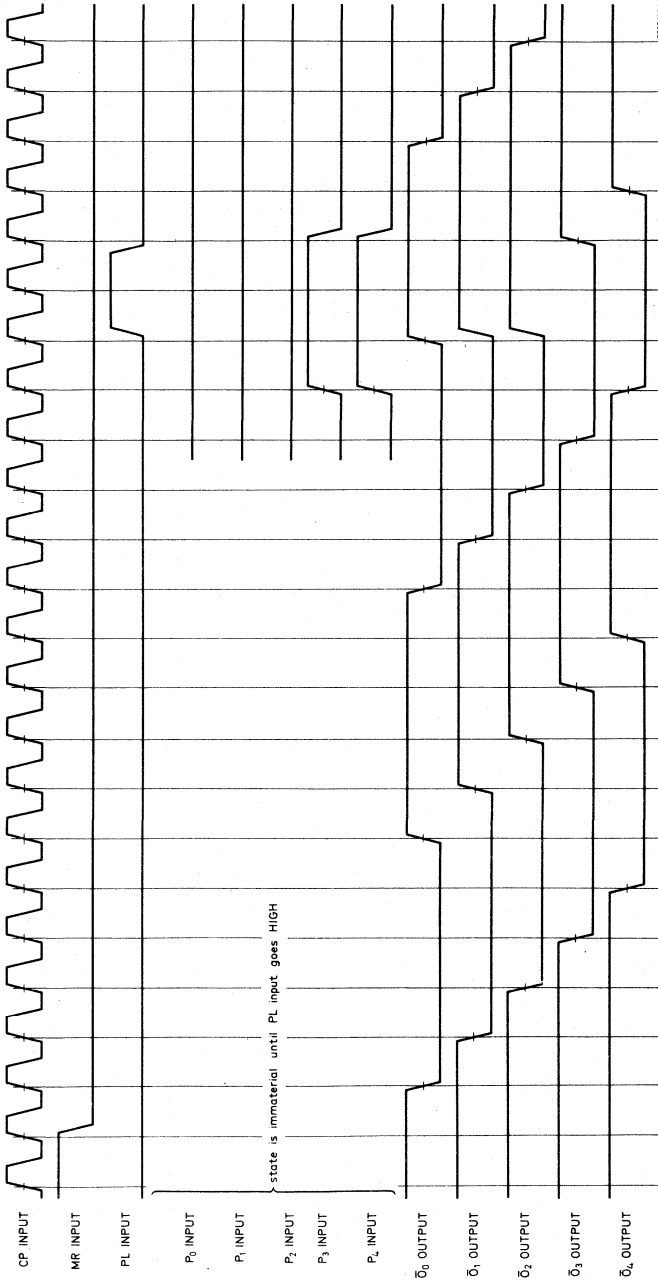


Fig. 7 Timing diagram.

Note

D input connected to \bar{Q}_4 for decade counter configuration.

QUADRUPLE 2-INPUT MULTIPLEXER



The HEF4019B provides four multiplexing circuits with common select inputs (S_A , S_B); each circuit contains two inputs (A_n , B_n) and one output (O_n). It may be used to select four bits of information from one of two sources.

The A inputs are selected when S_A is HIGH, the B inputs when S_B is HIGH. When S_A and S_B are HIGH, output (O_n) is the logical OR of the A_n and B_n inputs ($O_n = A_n + B_n$). When S_A and S_B are LOW, output (O_n) is LOW independent of the multiplexer inputs.

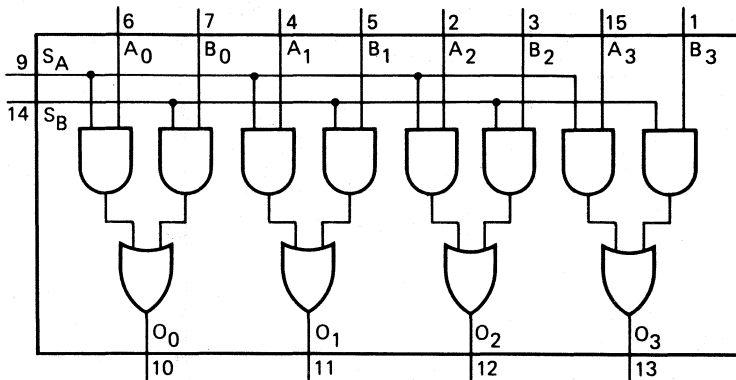
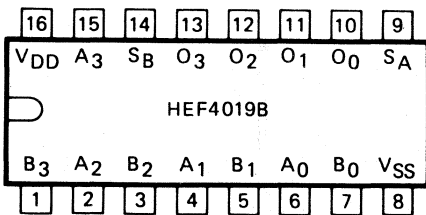


Fig. 1 Functional diagram.

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7Z69487.1

HEF4019BP: 16-lead DIL; plastic (SOT-38Z).
HEF4019BD: 16-lead DIL; ceramic (SOT-74).
HEF4019BT: 16-lead flat pack, plastic (SO-16; SOT-109A).

Fig. 2 Pinning diagram.

PINNING

S_A , S_B	select inputs (active HIGH)	B_0 to B_3	multiplexer inputs
A_0 to A_3	multiplexer inputs	O_0 to O_3	multiplexer outputs

FAMILY DATA

I_{DD} LIMITS category MSI

} see Family Specifications

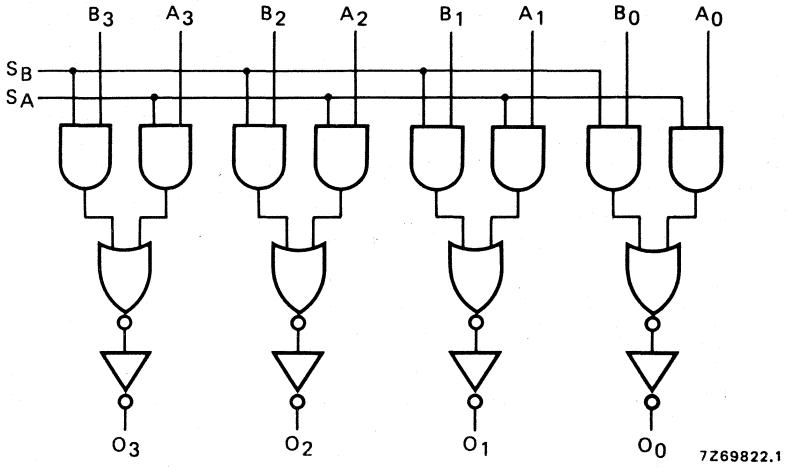


Fig. 3 Logic diagram.

TRUTH TABLE

select		inputs		output
S _A	S _B	A _n	B _n	O _n
L	L	X	X	L
H	L	L	X	L
H	L	H	X	H
L	H	X	L	L
L	H	X	H	H
H	H	H	X	H
H	H	X	H	H
H	H	L	L	L

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

A.C. CHARACTERISTICS

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	symbol	typ.	max.		typical extrapolation formula
Propagation delays $A_n, B_n, S_A, S_B \rightarrow O_n$ HIGH to LOW	5	t _{PHL}	70	145	ns	$43\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10		30	60	ns	$19\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15		25	50	ns	$17\text{ ns} + (0,16\text{ ns/pF}) C_L$
LOW to HIGH	5	t _{PLH}	60	130	ns	$38\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10		25	50	ns	$14\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15		15	35	ns	$7\text{ ns} + (0,16\text{ ns/pF}) C_L$
Output transition times HIGH to LOW	5	t _{THL}	60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$
	10		30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$
	15		20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$
LOW to HIGH	5	t _{TLH}	60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$
	10		30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$
	15		20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$

	V_{DD} V	typical formula for P (μW)	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
Dynamic power dissipation per package (P)	5	$1200 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	10	$5100 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$18700 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

APPLICATION INFORMATION

An example of an application for the HEF4019B is:

- True/complement selection.



14-STAGE BINARY COUNTER



The HEF4020B is a 14-stage binary ripple counter with a clock input (\overline{CP}), an overriding asynchronous master reset input (MR) and twelve fully buffered outputs (O_0, O_3 to O_{13}). The counter advances on the HIGH to LOW transition of \overline{CP} . A HIGH on MR clears all counter stages and forces all outputs LOW, independent of the state of \overline{CP} . Each counter stage is a static toggle flip-flop. A feature of the HEF4020B is: high speed (typ. 35 MHz at $V_{DD} = 15$ V).

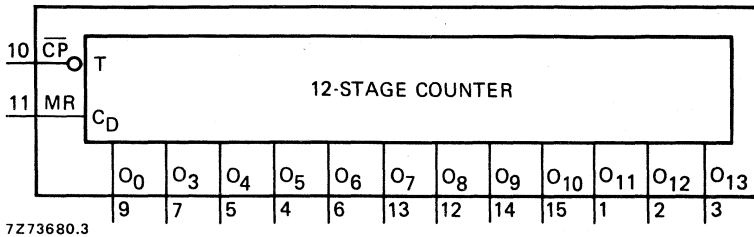


Fig. 1 Functional diagram.

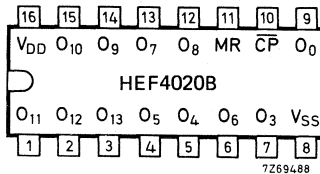


Fig. 2 Pinning diagram.

- HEF4020BP: 16-lead DIL; plastic (SOT-38Z).
- HEF4020BD: 16-lead DIL; ceramic (SOT-74).
- HEF4020BT: 16-lead flat pack; plastic (SO-16; SOT-109A).

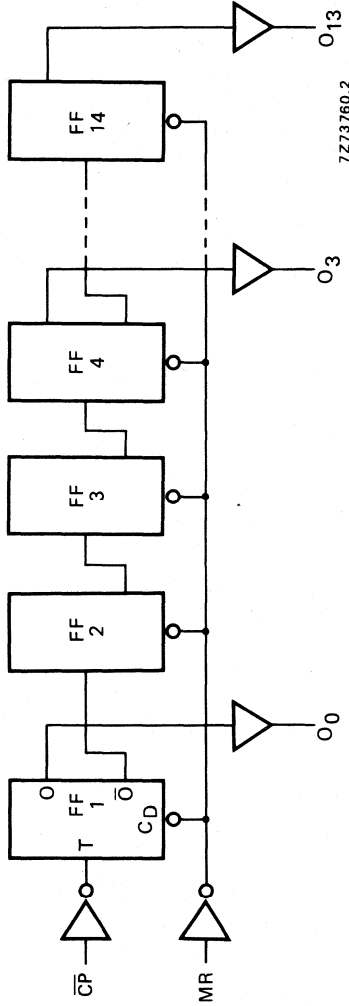
PINNING

- \overline{CP} clock input (HIGH to LOW edge triggered)
- MR master reset input (active HIGH)
- O_0, O_3 to O_{13} parallel outputs

FAMILY DATA

see Family Specifications

I_{DD} LIMITS category MSI



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Fig. 3 Logic diagram.

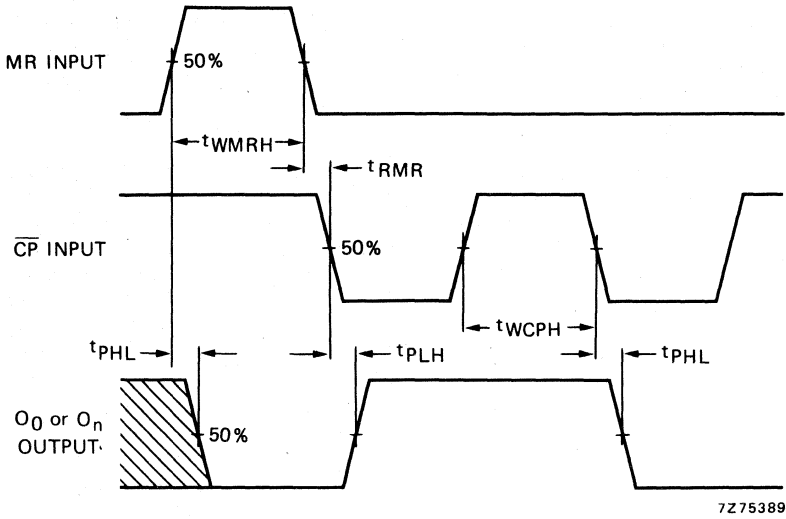


A.C. CHARACTERISTICS

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$; see also waveforms Fig. 4

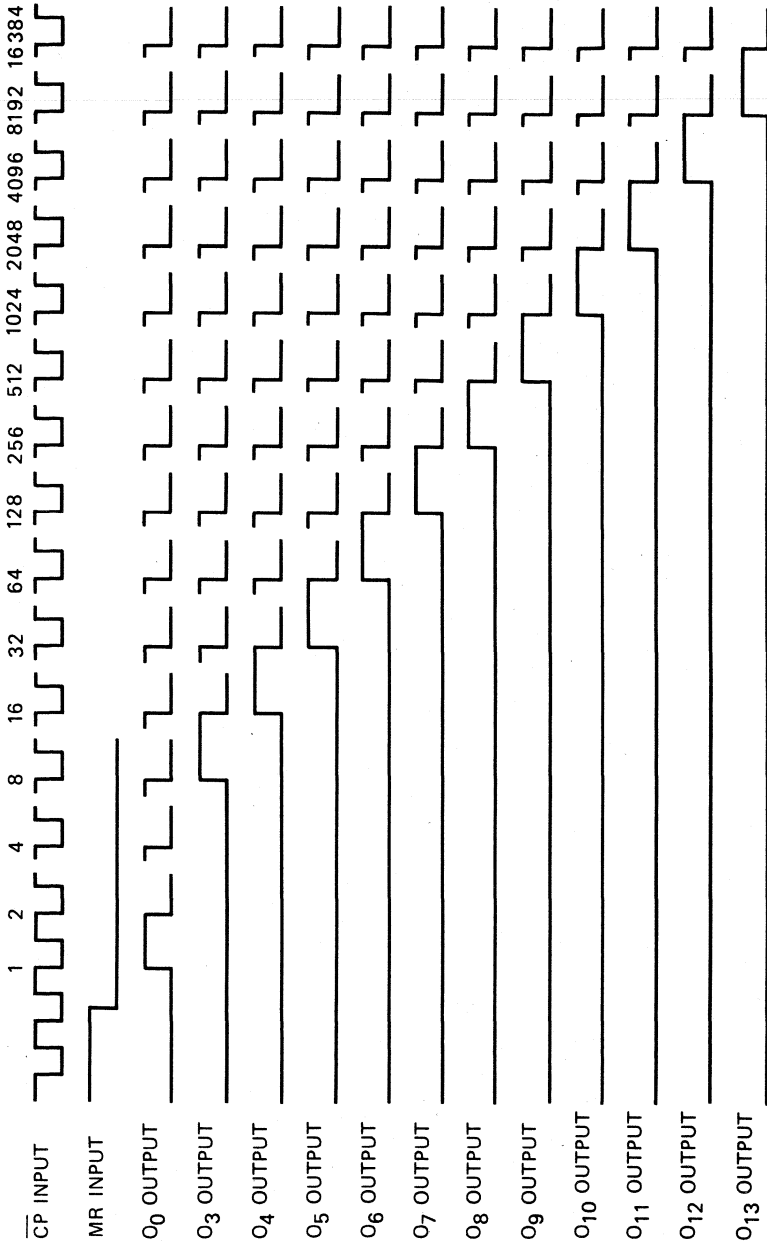
	V_{DD} V	symbol	min.	typ.	max.	typical extrapolation formula	
Propagation delays $\overline{CP} \rightarrow O_0$ HIGH to LOW	5	tPHL		105	210	ns	78 ns + (0,55 ns/pF) C_L
	10		45	90	ns	34 ns + (0,23 ns/pF) C_L	
	15		30	65	ns	22 ns + (0,16 ns/pF) C_L	
LOW to HIGH	5	tPLH		105	210	ns	78 ns + (0,55 ns/pF) C_L
	10		50	95	ns	39 ns + (0,23 ns/pF) C_L	
	15		35	70	ns	27 ns + (0,16 ns/pF) C_L	
$O_n \rightarrow O_{n+1}$ HIGH to LOW	5	tPHL		80	160	ns	53 ns + (0,55 ns/pF) C_L
	10		30	60	ns	19 ns + (0,23 ns/pF) C_L	
	15		20	40	ns	12 ns + (0,16 ns/pF) C_L	
LOW to HIGH	5	tPLH		70	140	ns	43 ns + (0,55 ns/pF) C_L
	10		25	50	ns	14 ns + (0,23 ns/pF) C_L	
	15		20	40	ns	12 ns + (0,16 ns/pF) C_L	
MR $\rightarrow O_n$ HIGH to LOW	5	tPHL		180	360	ns	153 ns + (0,55 ns/pF) C_L
	10		90	180	ns	79 ns + (0,23 ns/pF) C_L	
	15		70	140	ns	62 ns + (0,16 ns/pF) C_L	
Output transition times HIGH to LOW	5	tTHL		60	120	ns	10 ns + (1,0 ns/pF) C_L
	10		30	60	ns	9 ns + (0,42 ns/pF) C_L	
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L	
LOW to HIGH	5	tTLH		60	120	ns	10 ns + (1,0 ns/pF) C_L
	10		30	60	ns	9 ns + (0,42 ns/pF) C_L	
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L	
Minimum clock pulse width; HIGH	5	tWCPH	50	25		ns	
	10		25	15		ns	
	15		20	10		ns	
Minimum MR pulse width; HIGH	5	tWMRH	130	65		ns	
	10		95	50		ns	
	15		90	45		ns	
Recovery time for MR	5	tRMR	115	60		ns	
	10		65	35		ns	
	15		55	25		ns	
Maximum clock pulse frequency	5	f _{max}	5	10		MHz	
	10		13	25		MHz	
	15		18	35		MHz	

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$600 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz)
	10		f_o = output freq. (MHz)
	15		C_L = load cap. (pF)
			$\Sigma(f_o C_L)$ = sum of outputs
			V_{DD} = supply voltage (V)



7Z75389

Fig. 4 Waveforms showing propagation delays for MR to O_n and \overline{CP} to O_0 , minimum MR and \overline{CP} pulse widths.



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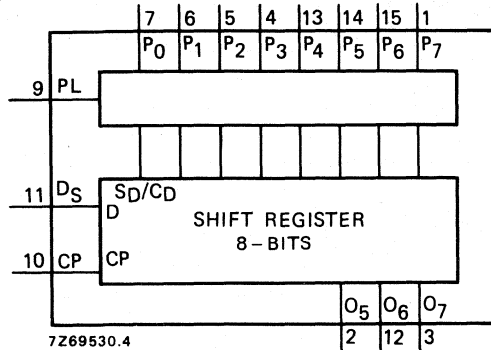
Fig. 5 Timing diagram.

8-BIT STATIC SHIFT REGISTER



The HEF4021B is an 8-bit static shift register (parallel-to-serial converter) with a synchronous serial data input (D_S), a clock input (CP), an asynchronous active HIGH parallel load input (PL), eight asynchronous parallel data inputs (P_0 to P_7) and buffered parallel outputs from the last three stages (O_5 to O_7).

Each register stage is a D-type master-slave flip-flop with a set direct/clear direct input. Information on P_0 to P_7 is asynchronously loaded into the register while PL is HIGH, independent of CP and D_S . When PL is LOW, data on D_S is shifted into the first register position and all the data in the register is shifted one position to the right on the LOW to HIGH transition of CP.



7Z69530.4

Fig. 1 Functional diagram.

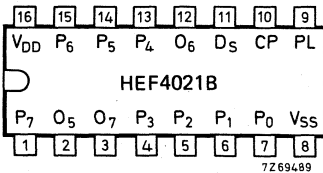


Fig. 2 Pinning diagram.

- HEF4021BP: 16-lead DIL; plastic (SOT-38Z).
- HEF4021BD: 16-lead DIL; ceramic (SOT-74).
- HEF4021BT: 16-lead flat pack; plastic (SO-16; SOT-109A).

PINNING

- PL parallel load input
- P_0 to P_7 parallel data inputs
- D_S serial data input
- CP clock input (LOW to HIGH edge-triggered)
- O_5 to O_7 buffered parallel outputs from the last three stages

FAMILY DATA

I_{DD} LIMITS category MSI } see Family Specifications

FUNCTION TABLES

Serial operation

n	inputs			outputs		
	CP	D _S	PL	O ₅	O ₆	O ₇
1	↘	D ₁	L	X	X	X
2	↘	D ₂	L	X	X	X
3	↘	D ₃	L	X	X	X
6	↘	X	L	D ₁	X	X
7	↘	X	L	D ₂	D ₁	X
8	↘	X	L	D ₃	D ₂	D ₁
	↘	X	L	no change		

Parallel operation

n	inputs			outputs		
	CP	D _S	PL	O ₅	O ₆	O ₇
	X	X	H	P ₅	P ₆	P ₇

- H = HIGH state (the more positive voltage)
- L = LOW state (the less positive voltage)
- X = state is immaterial
- ↘ = positive-going transition
- ↙ = negative-going transition
- D_n = either HIGH or LOW
- n = number of clock pulse transitions

A.C. CHARACTERISTICS

V_{SS} = 0 V; †_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V _{DD} V	symbol	min.	typ.	max.	typical extrapolation formula	
Propagation delays CP → O _n HIGH to LOW	5	t _{PHL}		170	340	ns	143 ns + (0,55 ns/pF)C _L
	10		65	130	ns	54 ns + (0,23 ns/pF)C _L	
	15		45	90	ns	37 ns + (0,16 ns/pF)C _L	
			130	260	ns	103 ns + (0,55 ns/pF)C _L	
	10		55	110	ns	44 ns + (0,23 ns/pF)C _L	
	15		40	80	ns	32 ns + (0,16 ns/pF)C _L	
LOW to HIGH	5	t _{PLH}		240	480	ns	213 ns + (0,55 ns/pF)C _L
	10		90	180	ns	79 ns + (0,23 ns/pF)C _L	
	15		60	125	ns	52 ns + (0,16 ns/pF)C _L	
			175	355	ns	148 ns + (0,55 ns/pF)C _L	
	10		70	140	ns	59 ns + (0,23 ns/pF)C _L	
	15		50	100	ns	42 ns + (0,16 ns/pF)C _L	
Output transition times HIGH to LOW	5	t _{THL}		60	120	ns	10 ns + (1,0 ns/pF) C _L
	10		30	60	ns	9 ns + (0,42 ns/pF) C _L	
	15		20	40	ns	6 ns + (0,28 ns/pF) C _L	
			60	120	ns	10 ns + (1,0 ns/pF) C _L	
	10		30	60	ns	9 ns + (0,42 ns/pF) C _L	
	15		20	40	ns	6 ns + (0,28 ns/pF) C _L	
LOW to HIGH	5	t _{TLH}		60	120	ns	10 ns + (1,0 ns/pF) C _L
	10		30	60	ns	9 ns + (0,42 ns/pF) C _L	
	15		20	40	ns	6 ns + (0,28 ns/pF) C _L	

A.C. CHARACTERISTICS

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^\circ\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	symbol	min.	typ.	max.	
Set-up times $D_S \rightarrow CP$	5		90	45	ns	see also waveforms Figs 4 and 5
	10	t_{su}	35	15	ns	
	15		25	10	ns	
$P_n \rightarrow PL$	5		145	70	ns	
	10	t_{su}	55	25	ns	
	15		40	20	ns	
Hold times $D_S \rightarrow CP$	5		40	20	ns	
	10	t_{hold}	20	10	ns	
	15		15	8	ns	
$P_n \rightarrow PL$	5		15	-10	ns	
	10	t_{hold}	15	0	ns	
	15		15	0	ns	
Minimum clock pulse width; LOW	5		110	55	ns	
	10	t_{WCPL}	40	20	ns	
	15		30	15	ns	
Minimum PL pulse width; HIGH	5		150	75	ns	
	10	t_{WPLH}	55	25	ns	
	15		40	20	ns	
Recovery time for PL	5		120	60	ns	
	10	t_{RPL}	40	20	ns	
	15		30	15	ns	
Maximum clock pulse frequency	5		4	9	MHz	
	10	f_{max}	12	25	MHz	
	15		18	37	MHz	

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5		f_i = input freq. (MHz)
	10	$1200 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_o = output freq. (MHz)
	15	$5250 f_i + \Sigma(f_o C_L) \times V_{DD}^2$ $13\ 250 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)

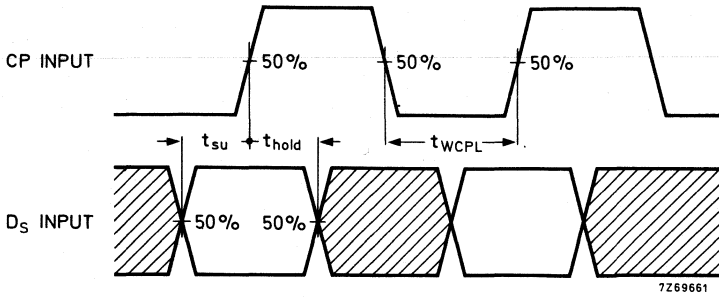


Fig. 4 Waveforms showing minimum clock pulse width, set-up time and hold time for CP and D_S.

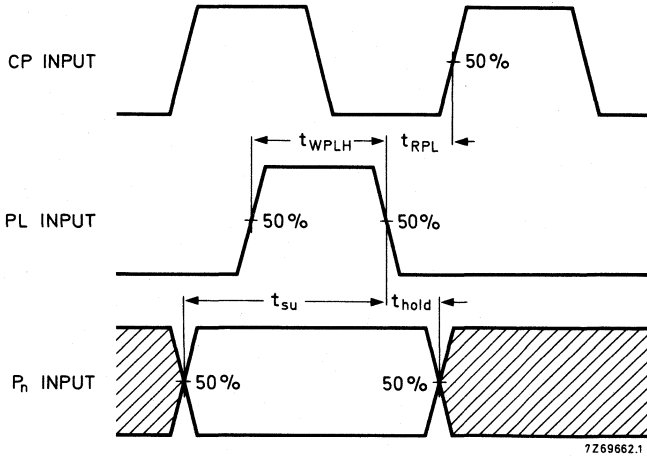


Fig. 5 Waveforms showing minimum PL pulse width, recovery time for PL, and set-up and hold times for P_n to PL. Set-up and hold times are shown as positive values but may be specified as negative values.

4-STAGE DIVIDE-BY-8 JOHNSON COUNTER



The HEF4022B is a 4-stage divide-by-8 Johnson counter with eight spike-free decoded active HIGH outputs (O_0 to O_7), an active LOW output from the most significant flip-flop (\overline{O}_{4-7}), active HIGH and active LOW clock inputs (CP_0 , \overline{CP}_1) and an overriding asynchronous master reset input (MR).

The counter is advanced by either a LOW to HIGH transition at CP_0 while \overline{CP}_1 is LOW or a HIGH to LOW transition at \overline{CP}_1 while CP_0 is HIGH (see also function table). Either CP_0 or \overline{CP}_1 may be used as clock input to the counter and the other clock input may be used as a clock enable input. When cascading counters, the \overline{O}_{4-7} output, which is LOW while the counter is in states, 4, 5, 6 and 7, can be used to drive the CP_0 input of the next counter.

A HIGH on MR resets the counter to zero ($O_0 = \overline{O}_{4-7} = \text{HIGH}$; O_1 to $O_7 = \text{LOW}$) independent of the clock inputs (CP_0 , \overline{CP}_1).

Automatic code correction of the counter is provided by an internal circuit, following any illegal code the counter returns to a proper counting mode within 11 clock pulses.

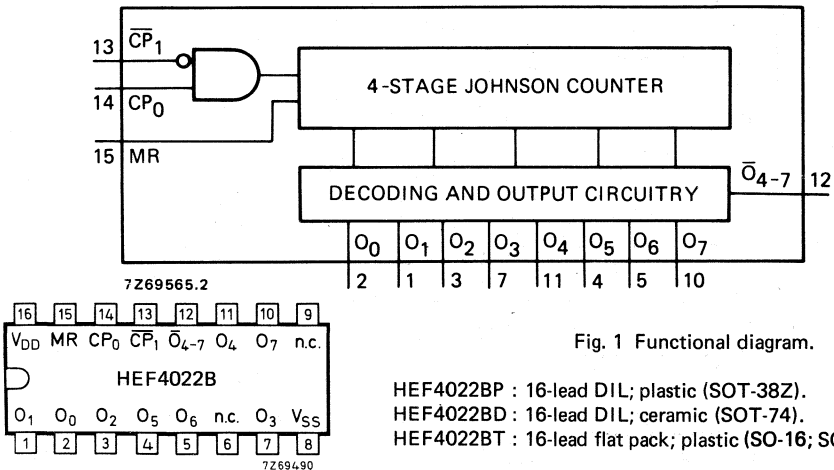


Fig. 1 Functional diagram.

HEF4022BP : 16-lead DIL; plastic (SOT-38Z).

HEF4022BD : 16-lead DIL; ceramic (SOT-74).

HEF4022BT : 16-lead flat pack; plastic (SO-16; SOT-109A).

Fig. 2 Pinning diagram.

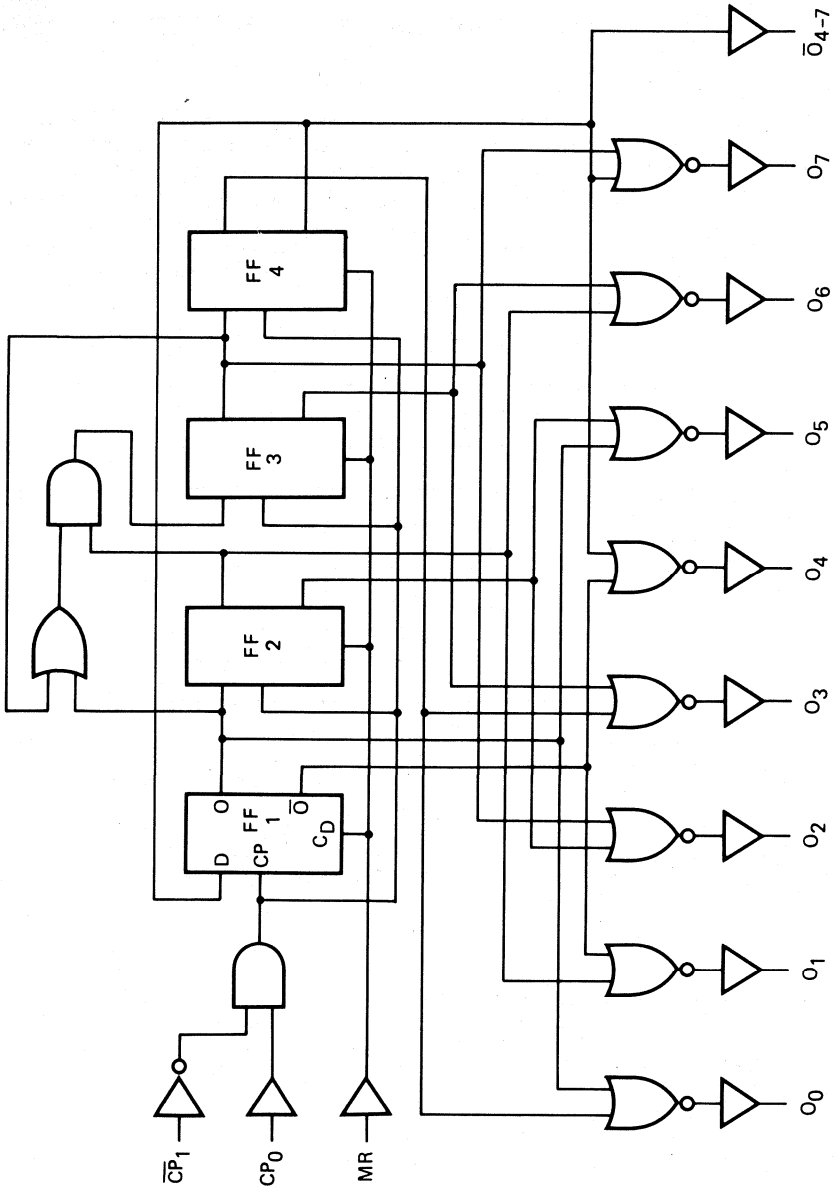
PINNING

- CP_0 clock input (LOW to HIGH; edge-triggered)
 \overline{CP}_1 clock input (HIGH to LOW; edge-triggered)
 MR master reset input
 O_0 to O_7 decoded outputs
 \overline{O}_{4-7} carry output (active LOW)

FAMILY DATA

IDD LIMITS category MSI

} see Family Specifications



7269804.2

Fig. 3 Logic diagram.

FUNCTION TABLE

MR	CP ₀	\overline{CP}_1	operation
H	X	X	O ₀ = \overline{O}_{4-7} = H; O ₁ to O ₇ = L
L	H	\searrow	Counter advances
L	\swarrow	L	Counter advances
L	L	X	No change
L	X	H	No change
L	H	\swarrow	No change
L	\searrow	L	No change

H = HIGH state (the more positive voltage)
 L = LOW state (the less positive voltage)
 X = state is immaterial
 \swarrow = positive-going transition
 \searrow = negative-going transition

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V _{DD} V	symbol	min.	typ.	max.	typical extrapolation formula
Propagation delays						
CP ₀ , \overline{CP}_1 → O _n HIGH to LOW	5			195	390 ns	168 ns + (0,55 ns/pF) C _L
	10	t _{PHL}		75	145 ns	64 ns + (0,23 ns/pF) C _L
	15			50	100 ns	42 ns + (0,16 ns/pF) C _L
LOW to HIGH	5			245	485 ns	218 ns + (0,55 ns/pF) C _L
	10	t _{PLH}		95	195 ns	84 ns + (0,23 ns/pF) C _L
	15			60	125 ns	52 ns + (0,16 ns/pF) C _L
CP ₀ , \overline{CP}_1 → \overline{O}_{4-7} HIGH to LOW	5			245	485 ns	218 ns + (0,55 ns/pF) C _L
	10	t _{PHL}		90	185 ns	79 ns + (0,23 ns/pF) C _L
	15			60	120 ns	52 ns + (0,16 ns/pF) C _L
LOW to HIGH	5			190	380 ns	163 ns + (0,55 ns/pF) C _L
	10	t _{PLH}		75	145 ns	64 ns + (0,23 ns/pF) C _L
	15			50	105 ns	42 ns + (0,16 ns/pF) C _L
MR → O ₁ to O ₇ HIGH to LOW	5			130	260 ns	103 ns + (0,55 ns/pF) C _L
	10	t _{PHL}		55	105 ns	44 ns + (0,23 ns/pF) C _L
	15			40	75 ns	32 ns + (0,16 ns/pF) C _L
MR → O ₀ LOW to HIGH	5			130	260 ns	103 ns + (0,55 ns/pF) C _L
	10	t _{PLH}		55	105 ns	44 ns + (0,23 ns/pF) C _L
	15			40	75 ns	32 ns + (0,16 ns/pF) C _L
MR → \overline{O}_{4-7} LOW to HIGH	5			110	220 ns	83 ns + (0,55 ns/pF) C _L
	10	t _{PLH}		45	90 ns	34 ns + (0,23 ns/pF) C _L
	15			35	70 ns	27 ns + (0,16 ns/pF) C _L
Output transition times						
HIGH to LOW	5			60	120 ns	10 ns + (1,0 ns/pF) C _L
	10	t _{THL}		30	60 ns	9 ns + (0,42 ns/pF) C _L
	15			20	40 ns	6 ns + (0,28 ns/pF) C _L
LOW to HIGH	5			60	120 ns	10 ns + (1,0 ns/pF) C _L
	10	t _{TLH}		30	60 ns	9 ns + (0,42 ns/pF) C _L
	15			20	40 ns	6 ns + (0,28 ns/pF) C _L

A.C. CHARACTERISTICS

 $V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	symbol	min.	typ.	max.	
Hold times $CP_0 \rightarrow \overline{CP}_1$	5	t_{hold}	140	70	ns	} see also waveforms Figs 4 and 5
	10		50	25	ns	
	15		30	15	ns	
$\overline{CP}_1 \rightarrow CP_0$	5	t_{hold}	170	85	ns	
	10		60	30	ns	
	15		40	20	ns	
Minimum clock pulse width	5	t_{WCP}	75	35	ns	
	10		30	15	ns	
	15		20	10	ns	
Minimum MR pulse width; HIGH	5	t_{WMRH}	70	35	ns	
	10		30	15	ns	
	15		20	10	ns	
Recovery time for MR	5	t_{RMR}	30	10	ns	
	10		15	5	ns	
	15		10	5	ns	
Maximum clock pulse frequency	5	f_{max}	3	6	MHz	
	10		8	16	MHz	
	15		12	24	MHz	

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$475 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz)
	10	$2400 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_o = output freq. (MHz)
	15	$6700 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	C_L = load capacitance (pF)
			$\Sigma(f_o C_L)$ = sum of outputs
			V_{DD} = supply voltage (V)

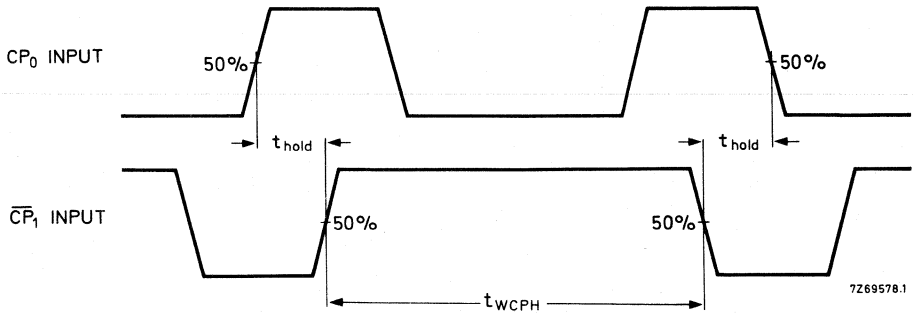


Fig. 4 Waveforms showing hold times for CP_0 to \overline{CP}_1 and \overline{CP}_1 to CP_0 . Hold times are shown as positive values, but may be specified as negative values.

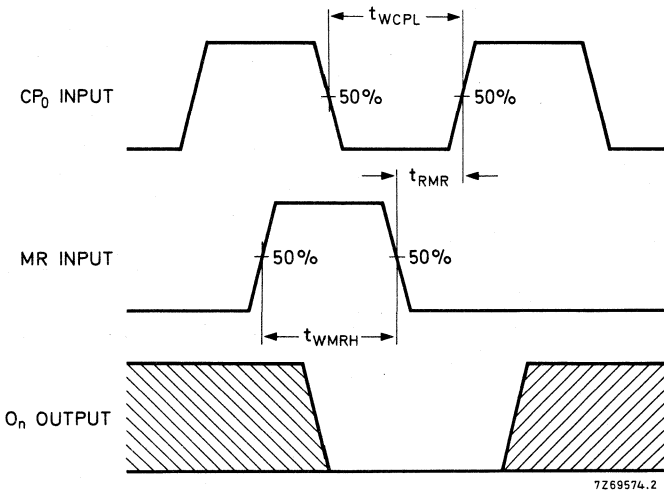


Fig. 5 Waveforms showing recovery time for MR; minimum CP_0 and MR pulse widths.

Conditions: $\overline{CP}_1 = \text{LOW}$ while CP_0 is triggered on a LOW to HIGH transition.
 t_{WCP} and t_{RMR} also apply when $CP_0 = \text{HIGH}$ and \overline{CP}_1 is triggered on a HIGH to LOW transition.

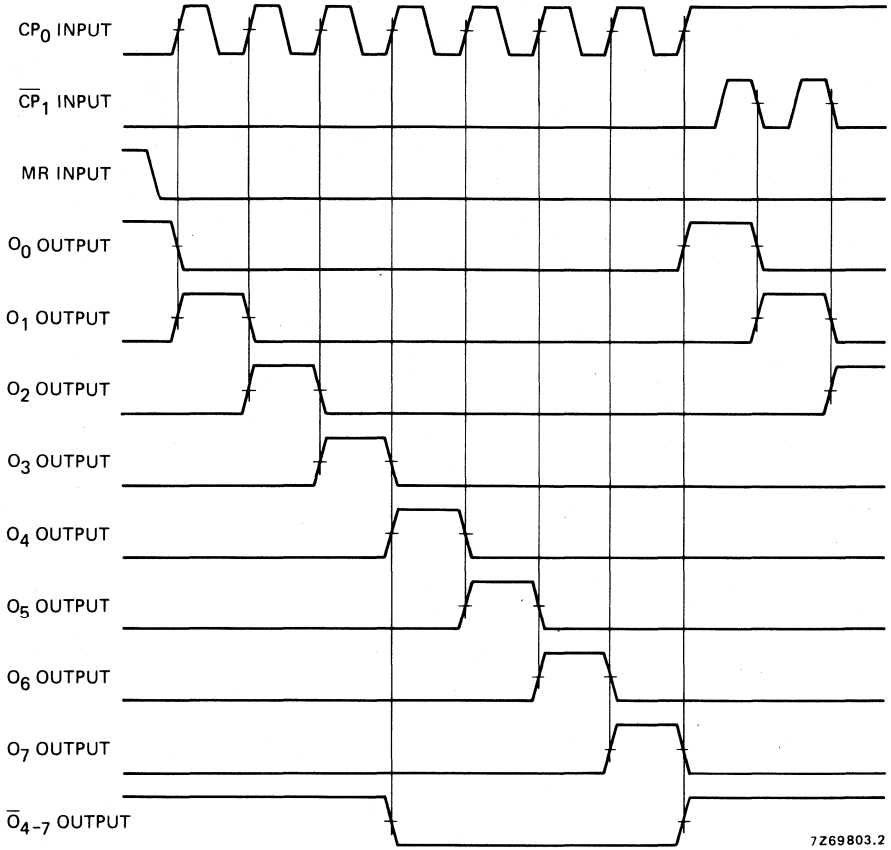


Fig. 6 Timing diagram.

APPLICATION INFORMATION

Some of the features of the HEF4022B are:

- High speed
- Spike-free decoded outputs
- Carry output for cascading

Figure 7 shows a technique for extending the number of decoded output states for the HEF4022B. Decoded outputs are sequential within each stage and from stage to stage, with no dead time (except propagation delay).

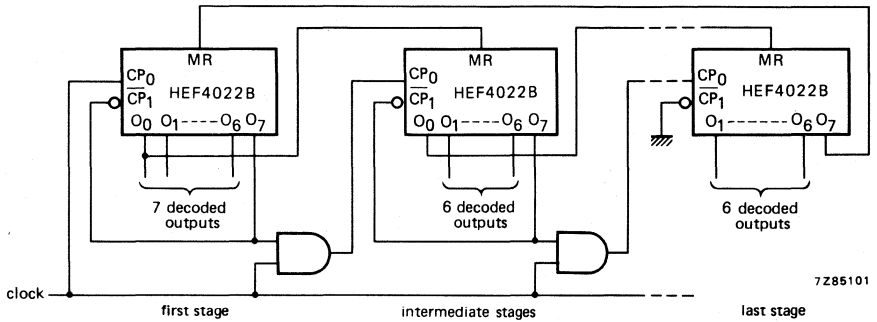
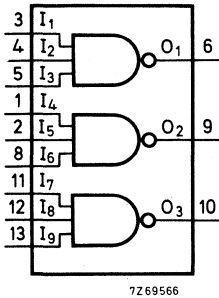


Fig. 7 Counter expansion.



TRIPLE 3-INPUT NAND GATE

The HEF4023B provides the positive triple 3-input NAND function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.



7269566

Fig. 1 Functional diagram.

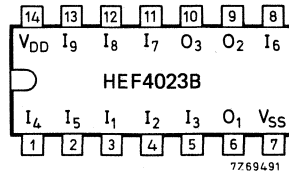
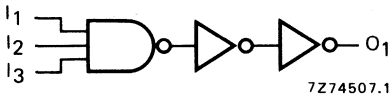


Fig. 2 Pinning diagram.

HEF4023BP: 14-lead DIL; plastic (SOT-27S,T,V).

HEF4023BD: 14-lead DIL; ceramic (SOT-73).

HEF4023BT: 14-lead flat pack; plastic (SO-14; SOT-108A).



7274507.1

Fig. 3 Logic diagram (one gate).

FAMILY DATA

IDD LIMITS category GATES

} see Family Specifications

A.C. CHARACTERISTICS

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^\circ\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	symbol	typ.	max.		typical extrapolation formula	
Propagation delays $I_n \rightarrow O_n$ HIGH to LOW	5	tPHL	65	135	ns	$38\text{ ns} + (0,55\text{ ns/pF}) C_L$	
	10		25	50	ns	$14\text{ ns} + (0,23\text{ ns/pF}) C_L$	
	15		15	30	ns	$7\text{ ns} + (0,16\text{ ns/pF}) C_L$	
	LOW to HIGH	5	tPLH	65	130	ns	$38\text{ ns} + (0,55\text{ ns/pF}) C_L$
		10		30	60	ns	$19\text{ ns} + (0,23\text{ ns/pF}) C_L$
		15		25	45	ns	$17\text{ ns} + (0,16\text{ ns/pF}) C_L$
Output transition times	5	tTHL	60	120	ns	$10\text{ ns} + 1,0\text{ ns/pF}) C_L$	
	10		30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$	
	15		20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$	
	LOW to HIGH	5	tTLH	60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$
		10		30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$
		15		20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$1200 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz)
	10	$5500 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_o = output freq. (MHz)
	15	$16\,400 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	C_L = load capacitance (pF)
			$\Sigma(f_o C_L)$ = sum of outputs
			V_{DD} = supply voltage (V)

7-STAGE BINARY COUNTER



The HEF4024B is a 7-stage binary ripple counter with a clock input (\overline{CP}), and overriding asynchronous master reset input (MR) and seven fully buffered parallel outputs (O_0 to O_6). The counter advances on the HIGH to LOW transition of \overline{CP} . A HIGH on MR clears all counter stages and forces all outputs LOW, independent of \overline{CP} . Each counter stage is a static toggle flip-flop.

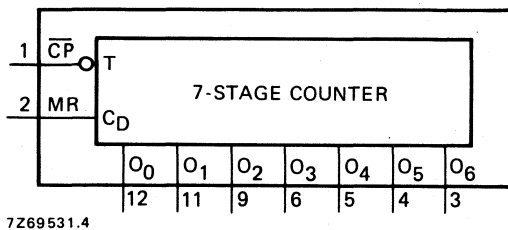


Fig. 1 Functional diagram.

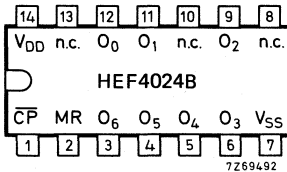


Fig. 2 Pinning diagram.

HEF4024BP: 14-lead DIL; plastic (SOT-27S, T, V).
 HEF4024BD: 14-lead DIL; ceramic (SOT-73).
 HEF4024BT: 14-lead flat pack; plastic (SO-14; SOT-108A).

PINNING

\overline{CP} clock input (HIGH to LOW triggered)
 MR master reset input
 O_0 to O_6 buffered parallel outputs

APPLICATION INFORMATION

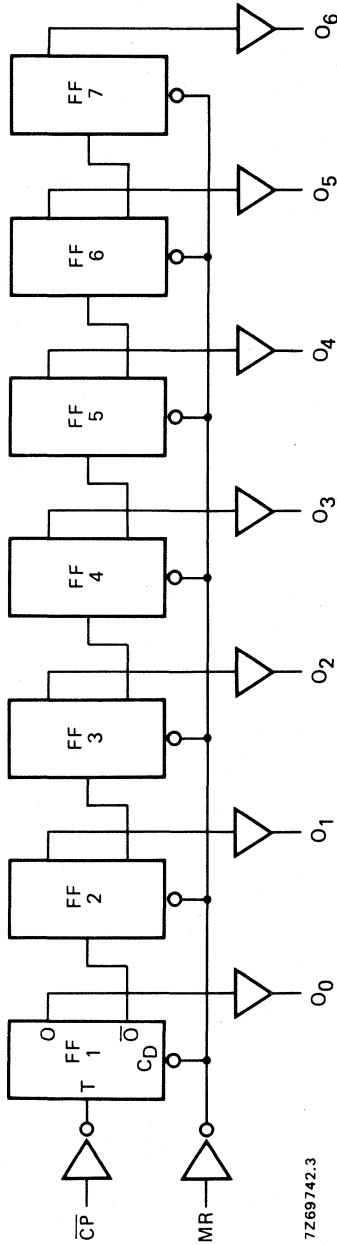
Some examples of applications for the HEF4024B are:

- Frequency dividers
- Time delay circuits

FAMILY DATA

I_{DD} LIMITS category MSI

} see Family Specifications



7Z69742.3

Fig. 3 Logic diagram.

A.C. CHARACTERISTICS

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^\circ\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$; see also waveforms Fig. 4

	V_{DD} V	symbol	min.	typ.	max.	typical extrapolation formula	
Propagation delays $\overline{CP} \rightarrow O_0$ HIGH to LOW	5			100	200	ns	$73\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10	t_{PHL}		40	75	ns	$29\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			25	50	ns	$17\text{ ns} + (0,16\text{ ns/pF}) C_L$
LOW to HIGH	5			105	210	ns	$78\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10	t_{PLH}		45	85	ns	$34\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			30	60	ns	$22\text{ ns} + (0,16\text{ ns/pF}) C_L$
$O_n \rightarrow O_{n+1}$ HIGH to LOW	5			60	120	ns	$33\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10	t_{PHL}		25	50	ns	$14\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			20	40	ns	$12\text{ ns} + (0,16\text{ ns/pF}) C_L$
LOW to HIGH	5			50	100	ns	$23\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10	t_{PLH}		20	40	ns	$9\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			15	30	ns	$7\text{ ns} + (0,16\text{ ns/pF}) C_L$
MR $\rightarrow O_n$ HIGH to LOW	5			120	240	ns	$93\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10	t_{PHL}		45	90	ns	$34\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			30	60	ns	$22\text{ ns} + (0,16\text{ ns/pF}) C_L$
Output transition times HIGH to LOW	5			60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$
	10	t_{THL}		30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$
	15			20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$
LOW to HIGH	5			60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$
	10	t_{TLH}		30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$
	15			20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$
Minimum clock pulse width; HIGH	5		60	30		ns	
	10	t_{WCPH}	30	15		ns	
	15		20	10		ns	
Minimum MR pulse width; HIGH	5		80	40		ns	
	10	t_{WMRH}	35	20		ns	
	15		25	15		ns	
Recovery time for MR	5		20	10		ns	
	10	t_{RMR}	15	5		ns	
	15		15	5		ns	
Maximum clock pulse frequency	5		5	10		MHz	
	10	f_{max}	13	25		MHz	
	15		18	35		MHz	

	V_{DD} V	typical formula for P (μW)	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load cap. (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
Dynamic power dissipation per package (P)	5	$500 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	10	$2100 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$5200 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

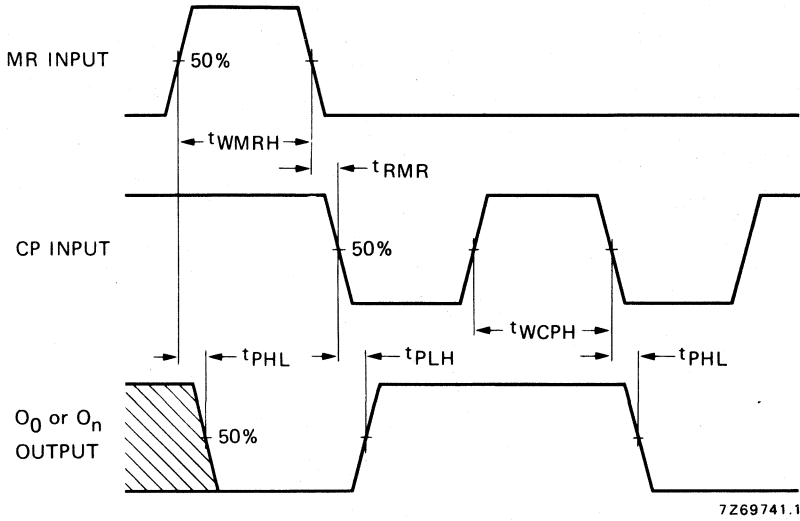


Fig. 4 Waveforms showing propagation delays for MR to O_n and \overline{CP} to O₀, minimum MR and \overline{CP} pulse widths and recovery time for MR.

TRIPLE 3-INPUT NOR GATE



The HEF4025B provides the positive triple 3-input NOR function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

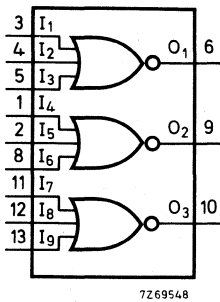


Fig. 1 Functional diagram.

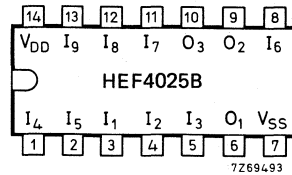


Fig. 2 Pinning diagram.

HEF4025BP : 14-lead DIL; plastic (SOT-27S, T, V).

HEF4025BD : 14-lead DIL; ceramic (SOT-73).

HEF4025BT : 14-lead flat pack; plastic (SO-14; SOT-108A).

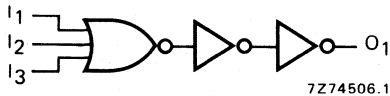


Fig. 3 Logic diagram (one gate).

FAMILY DATA

I_{DD} LIMITS category GATES

} see Family Specifications

A.C. CHARACTERISTICS

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^\circ\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

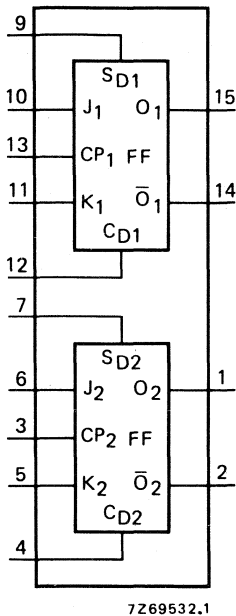
	V_{DD} V	symbol	typ.	max.		typical extrapolation formula
Propagation delays $I_n \rightarrow O_n$ HIGH to LOW	5	tPHL	70	135	ns	$43\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10		25	55	ns	$14\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15		20	40	ns	$12\text{ ns} + (0,16\text{ ns/pF}) C_L$
LOW to HIGH	5	tPLH	60	120	ns	$33\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10		25	50	ns	$14\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15		15	35	ns	$7\text{ ns} + (0,16\text{ ns/pF}) C_L$
Output transition times HIGH to LOW	5	tTHL	60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$
	10		30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$
	15		20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$
LOW to HIGH	5	tTLH	60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$
	10		30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$
	15		20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$900 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz)
	10		f_o = output freq. (MHz)
	15		C_L = load capacitance (pF)
			$\Sigma(f_o C_L)$ = sum of outputs
			V_{DD} = supply voltage (V)

DUAL JK FLIP-FLOP



The HEF4027B is a dual JK flip-flop which is edge-triggered and features independent set direct (S_D), clear direct (C_D), clock (CP) inputs and outputs (O, \bar{O}). Data is accepted when CP is LOW, and transferred to the output on the positive-going edge of the clock. The active HIGH asynchronous clear-direct (C_D) and set-direct (S_D) are independent and override the J, K, and CP inputs. The outputs are buffered for best system performance.



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Fig. 1 Functional diagram.

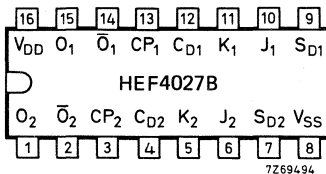


Fig. 2 Pinning diagram.

FUNCTION TABLES

inputs					outputs	
S_D	C_D	CP	J	K	O	\bar{O}
H	L	X	X	X	H	L
L	H	X	X	X	L	H
H	H	X	X	X	H	H

inputs					outputs	
S_D	C_D	CP	J	K	O_{n+1}	\bar{O}_{n+1}
L	L	/	L	L	no change	
L	L	/	H	L	H	L
L	L	/	L	H	L	H
L	L	/	H	H	\bar{O}_n	O_n

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

X = state is immaterial

/ = positive-going transition

 O_{n+1} = state after clock positive transition

PINNING

J,K synchronous inputs

CP clock input (L to H edge-triggered)

 S_D asynchronous set-direct input (active HIGH) C_D asynchronous clear-direct input (active HIGH)

O true output

 \bar{O} complement output

HEF4027BP: 16-lead DIL; plastic (SOT-38Z).

HEF4027BD: 16-lead DIL; ceramic (SOT-74).

HEF4027BT: 16-lead flat pack; plastic (SO-16; SOT-109A).

FAMILY DATA

 I_{DD} LIMITS category FLIP-FLOPS

see Family Specifications

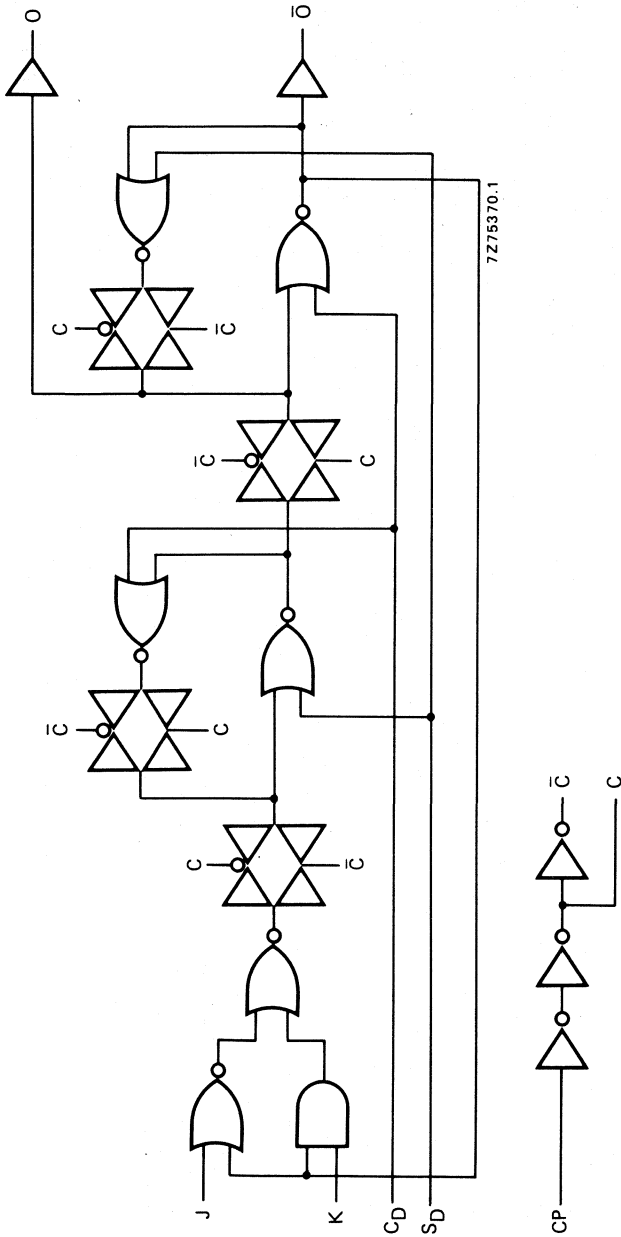


Fig. 3 Logic diagram (one flip-flop).

|||||

A.C. CHARACTERISTICS

 $V_{SS} = 0$ V; $T_{amb} = 25$ °C; $C_L = 50$ pF; input transition times ≤ 20 ns

	V_{DD} V	symbol	min.	typ.	max.	typical extrapolation formula	
Propagation delays CP \rightarrow O, \bar{O} HIGH to LOW	5	t _{PHL}		115	230	ns	88 ns + (0,55 ns/pF) C _L
	10		50	100	ns	39 ns + (0,23 ns/pF) C _L	
	15		35	75	ns	27 ns + (0,16 ns/pF) C _L	
LOW to HIGH	5	t _{PLH}		115	230	ns	88 ns + (0,55 ns/pF) C _L
	10		50	100	ns	39 ns + (0,23 ns/pF) C _L	
	15		35	75	ns	27 ns + (0,16 ns/pF) C _L	
S _D \rightarrow O LOW to HIGH	5	t _{PLH}		75	155	ns	48 ns + (0,55 ns/pF) C _L
	10		35	70	ns	24 ns + (0,23 ns/pF) C _L	
	15		25	45	ns	17 ns + (0,16 ns/pF) C _L	
C _D \rightarrow O HIGH to LOW	5	t _{PHL}		130	260	ns	102 ns + (0,55 ns/pF) C _L
	10		50	105	ns	39 ns + (0,23 ns/pF) C _L	
	15		35	75	ns	27 ns + (0,16 ns/pF) C _L	
Output transition times HIGH to LOW	5	t _{THL}		60	120	ns	10 ns + (1,0 ns/pF) C _L
	10		30	60	ns	9 ns + (0,42 ns/pF) C _L	
	15		20	40	ns	6 ns + (0,28 ns/pF) C _L	
LOW to HIGH	5	t _{TLH}		60	120	ns	10 ns + (1,0 ns/pF) C _L
	10		30	60	ns	9 ns + (0,42 ns/pF) C _L	
	15		20	40	ns	6 ns + (0,28 ns/pF) C _L	
Set-up time J, K \rightarrow CP	5	t _{su}	95	50		ns	see also waveforms Figs 4 and 5
	10		30	15		ns	
	15		20	10		ns	
Hold time J, K \rightarrow CP	5	t _{hold}	25	0		ns	
	10		20	0		ns	
	15		15	5		ns	
Minimum clock pulse width; LOW	5	t _{WCPL}	95	50		ns	
	10		40	20		ns	
	15		30	15		ns	
Minimum S _D , C _D pulse width; HIGH	5	t _{WSDH}	80	40		ns	
	10	t _{WCDH}	40	20		ns	
	15	t _{WCDH}	30	15		ns	
Recovery time for S _D , C _D	5	t _{RSD} , t _{RCD}	40	10		ns	
	10		25	5		ns	
	15		15	0		ns	

A.C. CHARACTERISTICS

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^\circ\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	symbol	min	typ	max	
Maximum clock pulse frequency J = K = HIGH	5	f_{max}	3	6	MHz	} see also waveforms Fig. 4
	10		7	15	MHz	
	15		11	22	MHz	

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$800 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz)
	10	$3900 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_o = output freq. (MHz)
	15	$10800 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	C_L = load capacitance (pF)
			$\Sigma(f_o C_L)$ = sum of outputs
			V_{DD} = supply voltage (V)

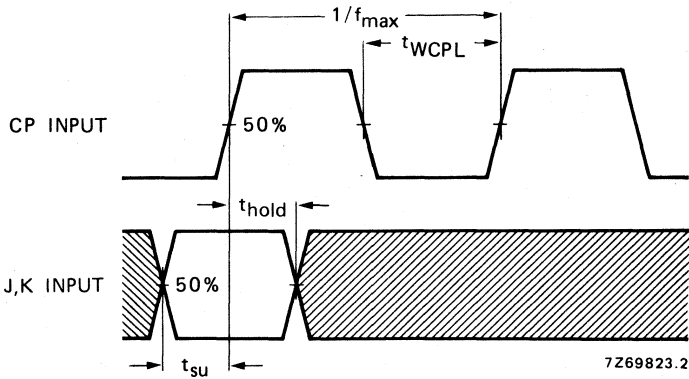


Fig. 4 Waveforms showing set-up times, hold times and minimum clock pulse width. Set-up and hold times are shown as positive values but may be specified as negative values.

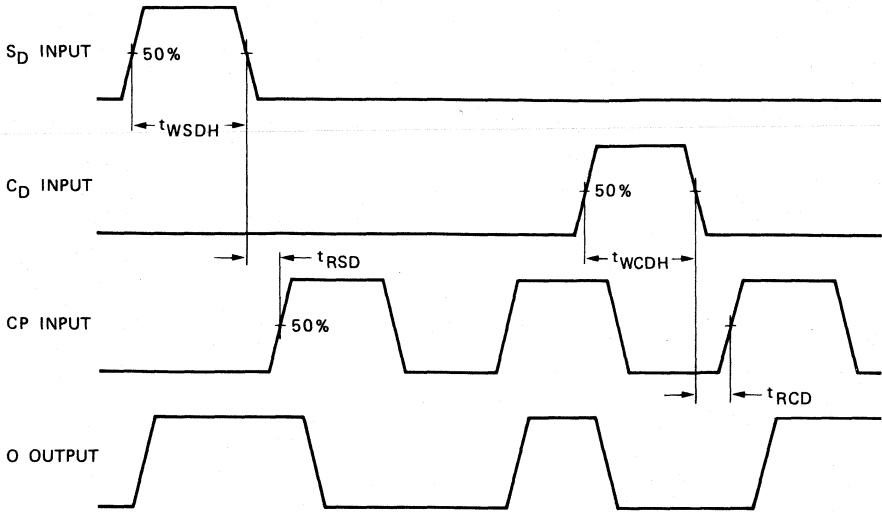


Fig. 5 Waveforms showing recovery times for S_D and C_D; minimum S_D and C_D pulse widths.

APPLICATION INFORMATION

Some examples of applications for the HEF4027B are:

- Registers
- Counters
- Control circuits

1-OF-10 DECODER



The HEF4028B is a 4-bit BCD to 1-of-10 active HIGH decoder. A 1-2-4-8 BCD code applied to inputs A_0 to A_3 causes the selected output to be HIGH, the other nine will be LOW. If desired, the device may be used as a 1-of-8 decoder with enable; 3-bit octal inputs are applied to inputs A_0 , A_1 and A_2 selecting an output O_0 to O_7 . Input A_3 then becomes an active LOW enable, forcing the selected output LOW when A_3 is HIGH. The HEF4028B may also be used as an 8-output (O_0 to O_7) demultiplexer with A_0 to A_2 as address inputs and A_3 as an active LOW data input. The outputs are fully buffered for best performance.

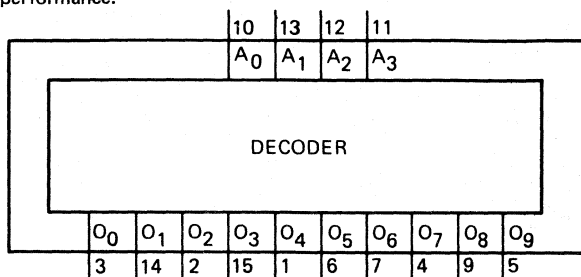


Fig.1 Functional diagram.

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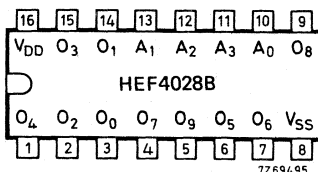


Fig.2 Pinning diagram

HEF4028BP: 16-lead DIL; plastic (SOT-38Z).

HEF4028BD: 16-lead DIL; ceramic (SOT-74).

HEF4028BT: 16-lead flat pack: plastic (SO-16; SOT-109A).

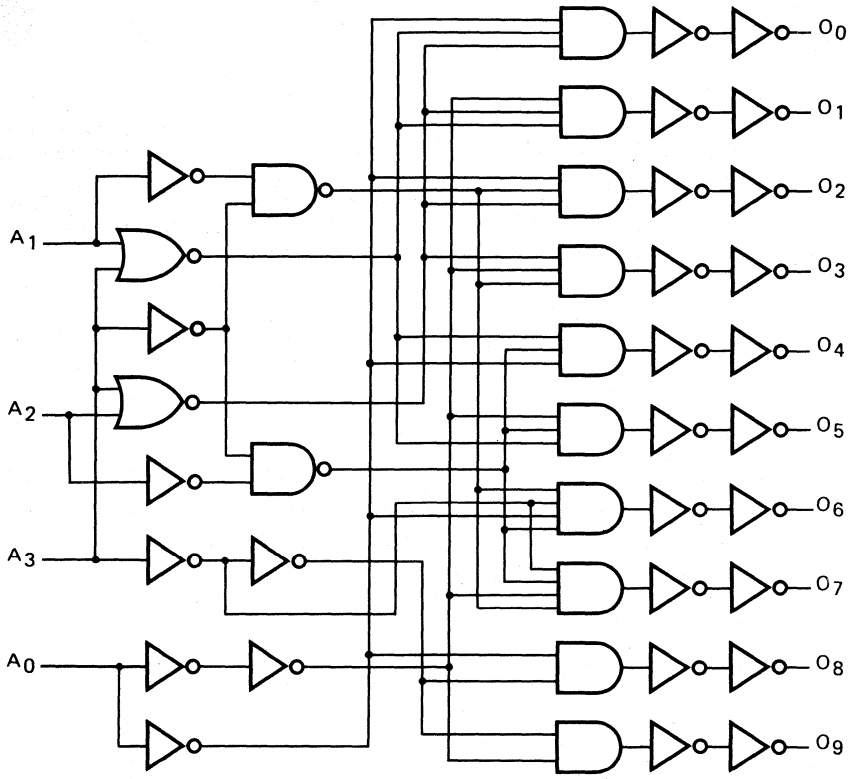
PINNING

 A_0 to A_3 address inputs, 1-2-4-8 BCD O_0 to O_9 outputs (active HIGH)

FAMILY DATA

 I_{DD} LIMITS category MSI

} see Family Specifications



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Fig.3 Logic diagram.

TRUTH TABLE

inputs				outputs									
A ₃	A ₂	A ₁	A ₀	O ₀	O ₁	O ₂	O ₃	O ₄	O ₅	O ₆	O ₇	O ₈	O ₉
L	L	L	L	H	L	L	L	L	L	L	L	L	L
L	L	L	H	L	H	L	L	L	L	L	L	L	L
L	L	H	L	L	L	H	L	L	L	L	L	L	L
L	L	H	H	L	L	L	H	L	L	L	L	L	L
L	H	L	L	L	L	L	L	H	L	L	L	L	L
L	H	L	H	L	L	L	L	L	H	L	L	L	L
L	H	H	L	L	L	L	L	L	L	H	L	L	L
L	H	H	H	L	L	L	L	L	L	L	H	L	L
H	L	L	L	L	L	L	L	L	L	L	L	H	L
H	L	L	H	L	L	L	L	L	L	L	L	L	H
H	L	H	L	L	L	L	L	L	L	L	L	H	L
H	L	H	H	L	L	L	L	L	L	L	L	L	H
H	H	L	L	L	L	L	L	L	L	L	L	L	H
H	H	L	H	L	L	L	L	L	L	L	L	L	H
H	H	H	L	L	L	L	L	L	L	L	L	H	L
H	H	H	H	L	L	L	L	L	L	L	L	L	H
H	L	H	L	L	L	L	L	L	L	L	L	H	L
H	L	H	H	L	L	L	L	L	L	L	L	L	H
H	H	L	L	L	L	L	L	L	L	L	L	L	H
H	H	L	H	L	L	L	L	L	L	L	L	L	H
H	H	H	L	L	L	L	L	L	L	L	L	L	H
H	H	H	H	L	L	L	L	L	L	L	L	L	H

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

* Extraordinary states.



A.C. CHARACTERISTICS

 $V_{SS} = 0 \text{ V}$; $T_{amb} = 25 \text{ }^\circ\text{C}$; $C_L = 50 \text{ pF}$; input transition times $\leq 20 \text{ ns}$

	V_{DD} V	symbol	typ.	max.		typical extrapolation formula	
Propagation delays $A_n \rightarrow O_n$ HIGH to LOW	5	t_{PHL}	110	220	ns	$83 \text{ ns} + (0,55 \text{ ns/pF}) C_L$	
	10		50	95	ns	$39 \text{ ns} + (0,23 \text{ ns/pF}) C_L$	
	15		35	70	ns	$27 \text{ ns} + (0,16 \text{ ns/pF}) C_L$	
	LOW to HIGH	5	t_{PLH}	100	195	ns	$73 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
		10		45	85	ns	$34 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
		15		30	65	ns	$22 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
Output transition times HIGH to LOW	5	t_{THL}	60	120	ns	$10 \text{ ns} + (1,0 \text{ ns/pF}) C_L$	
	10		30	60	ns	$9 \text{ ns} + (0,42 \text{ ns/pF}) C_L$	
	15		20	40	ns	$6 \text{ ns} + (0,28 \text{ ns/pF}) C_L$	
	LOW to HIGH	5	t_{TLH}	60	120	ns	$10 \text{ ns} + (1,0 \text{ ns/pF}) C_L$
		10		30	60	ns	$9 \text{ ns} + (0,42 \text{ ns/pF}) C_L$
		15		20	40	ns	$6 \text{ ns} + (0,28 \text{ ns/pF}) C_L$

	V_{DD} V	typical formula for P (μW)	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
Dynamic power dissipation per package (P)	5	$1\,700 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	10	$7\,500 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$20\,200 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

SYNCHRONOUS UP/DOWN COUNTER, BINARY/DECADE COUNTER



The HEF4029B is a synchronous edge-triggered up/down 4-bit binary/BCD decade counter with a clock input (CP), an active LOW count enable input (\overline{CE}), an up/down control input (UP/ \overline{DN}), a binary/decade control input (BIN/ \overline{DEC}), an overriding asynchronous active HIGH parallel load input (PL), four parallel data inputs (P_0 to P_3), four parallel buffered outputs (O_0 to O_3) and an active LOW terminal count output (\overline{TC}).

Information on P_0 to P_3 is asynchronously loaded into the counter while PL is HIGH, independent of CP.

The counter is advanced one count on the LOW to HIGH transition of CP when \overline{CE} and PL are LOW. The \overline{TC} signal is normally HIGH and goes LOW when the counter reaches its maximum count in the UP mode, or the minimum count in the DOWN mode provided \overline{CE} is LOW.

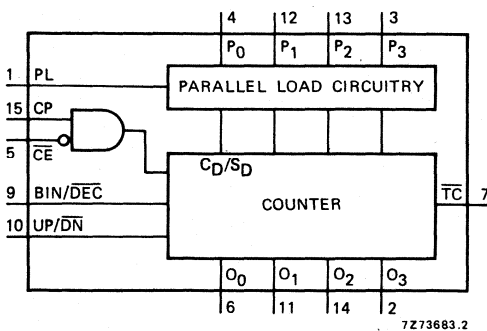


Fig. 1 Functional diagram.

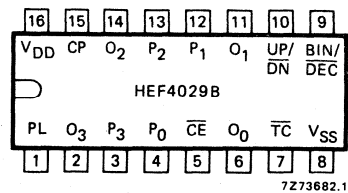


Fig. 2 Pinning diagram.

PINNING

PL	parallel load input
P_0 to P_3	parallel data inputs
BIN/ \overline{DEC}	binary/decade control input
UP/ \overline{DN}	up/down control input
\overline{CE}	count enable input (active LOW)
CP	clock input (LOW to HIGH, edge triggered)
O_0 to O_3	buffered parallel outputs
\overline{TC}	terminal count output (active LOW)

HEF4029BP : 16-lead DIL; plastic (SOT-38Z).

HEF4029BD : 16-lead DIL; ceramic (SOT-74).

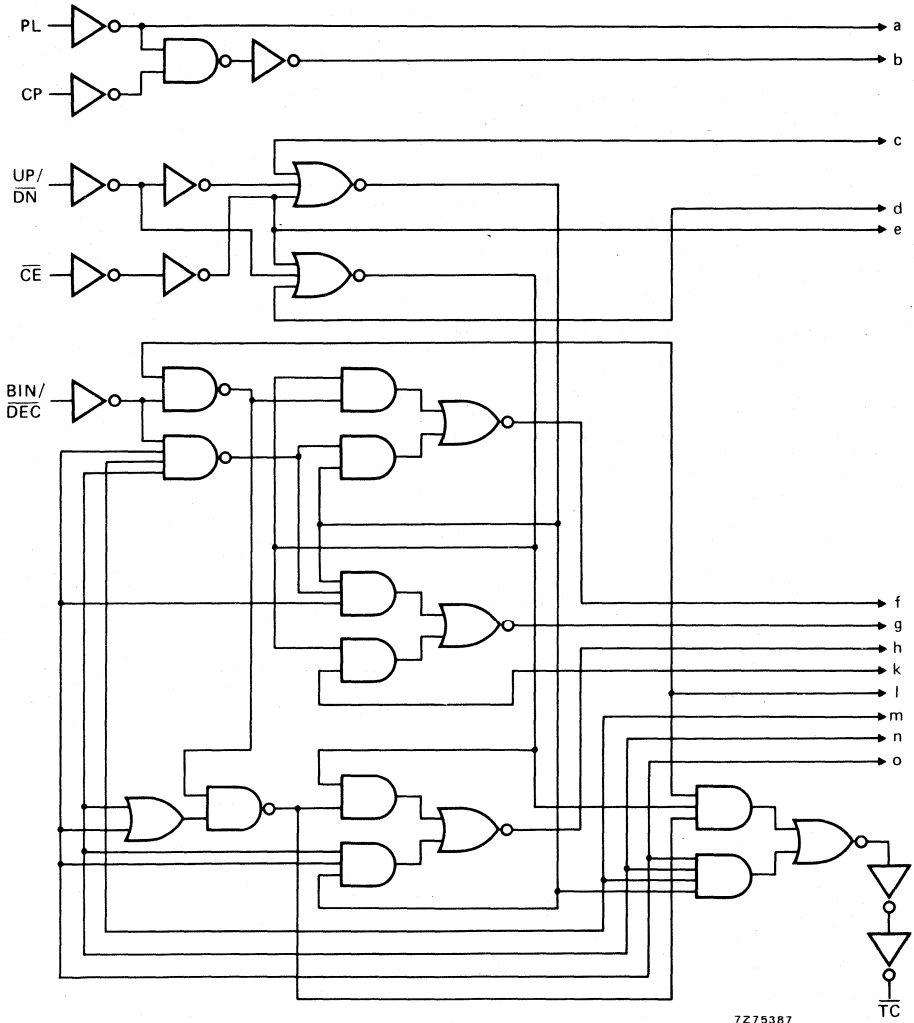
HEF4029BT : 16-lead flat pack; plastic
(SO-16; SOT-109A).

FAMILY DATA

I_{DD} LIMITS category MSI

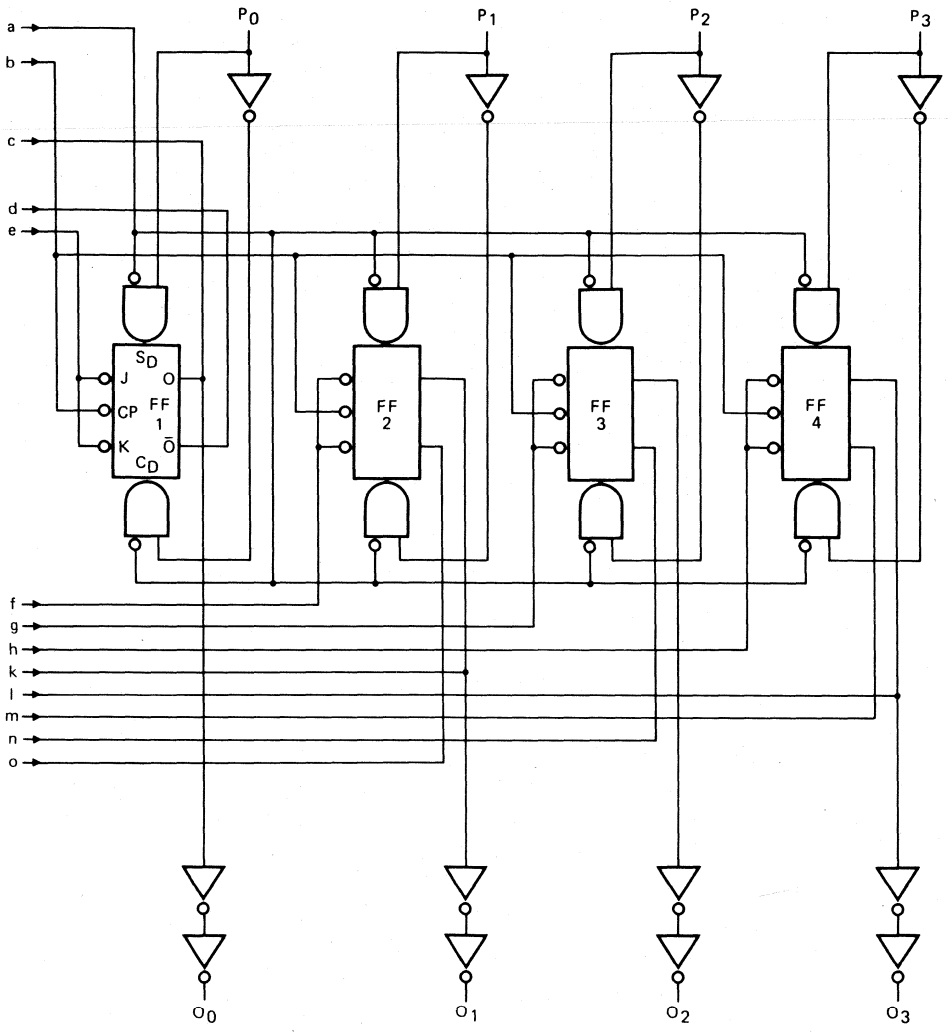
} see Family Specifications

HEF4029B
MSI



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Fig. 3a Logic diagram (continued in Fig. 3b).



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Fig. 3b Logic diagram (continued from Fig. 3a).

FUNCTION TABLE

PL	BIN/DEC	UP/DN	\overline{CE}	CP	mode
H	X	X	X	X	parallel load ($P_n \rightarrow O_n$)
L	X	X	H	X	no change
L	L	L	L	\nearrow	count-down, decade
L	L	H	L	\nearrow	count-up, decade
L	H	L	L	\nearrow	count-down, binary
L	H	H	L	\nearrow	count-up, binary

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

X = state is immaterial

\nearrow = positive-going clock pulse edge

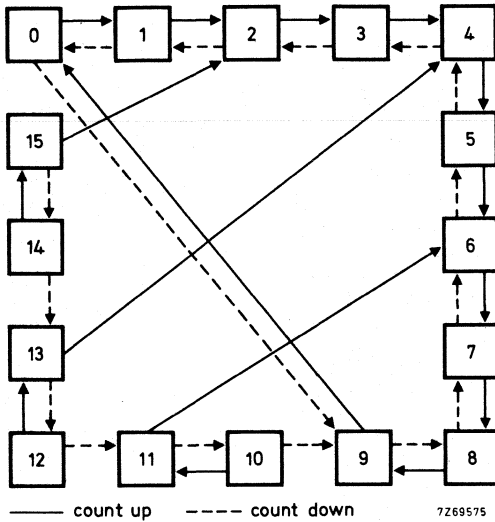


Fig. 4 State diagram; $\overline{\text{BIN/DEC}} = \text{LOW}$.

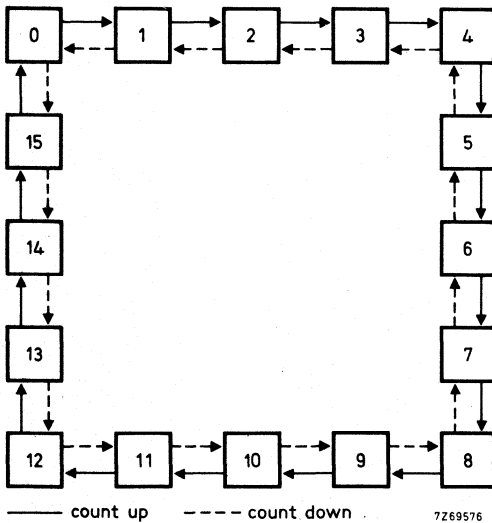


Fig. 5 State diagram; $\overline{\text{BIN/DEC}} = \text{HIGH}$.

Logic equation for terminal count:

$$TC = \overline{\text{CE}} (\overline{\text{BIN/DEC}} \cdot \text{UP} / \overline{\text{DN}} \cdot \text{O}_0 \cdot \text{O}_1 \cdot \text{O}_2 \cdot \text{O}_3 + \overline{\text{BIN/DEC}} \cdot \overline{\text{UP}} / \overline{\text{DN}} \cdot \overline{\text{O}}_0 \cdot \overline{\text{O}}_1 \cdot \overline{\text{O}}_2 \cdot \overline{\text{O}}_3 + \overline{\text{BIN/DEC}} \cdot \overline{\text{UP}} / \overline{\text{DN}} \cdot \text{O}_0 \cdot \text{O}_3 + \overline{\text{BIN/DEC}} \cdot \overline{\text{UP}} / \overline{\text{DN}} \cdot \overline{\text{O}}_0 \cdot \overline{\text{O}}_1 \cdot \overline{\text{O}}_2 \cdot \overline{\text{O}}_3)$$

A.C. CHARACTERISTICS

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	typical formula for P (μW)	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
Dynamic power dissipation per package (P)	5	$1000 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	10	$4500 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$11\,500 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

A.C. CHARACTERISTICS

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	symbol	min.	typ.	max.	typical extrapolation formula	
Propagation delays $CP \rightarrow O_n$ HIGH to LOW	5	t_{PHL}		145	290	ns	$118\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10			55	110	ns	$44\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			40	75	ns	$32\text{ ns} + (0,16\text{ ns/pF}) C_L$
LOW to HIGH	5	t_{PLH}		160	315	ns	$133\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10			60	120	ns	$49\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			40	80	ns	$32\text{ ns} + (0,16\text{ ns/pF}) C_L$
$CP \rightarrow \overline{TC}$ HIGH to LOW	5	t_{PHL}		280	560	ns	$253\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10			105	205	ns	$94\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			70	140	ns	$62\text{ ns} + (0,16\text{ ns/pF}) C_L$
LOW to HIGH	5	t_{PLH}		195	385	ns	$168\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10			75	150	ns	$64\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			55	105	ns	$47\text{ ns} + (0,16\text{ ns/pF}) C_L$
$PL \rightarrow O_n$ HIGH to LOW	5	t_{PHL}		120	240	ns	$93\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10			50	100	ns	$39\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			35	70	ns	$27\text{ ns} + (0,16\text{ ns/pF}) C_L$
LOW to HIGH	5	t_{PLH}		170	335	ns	$143\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10			65	130	ns	$54\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			45	90	ns	$37\text{ ns} + (0,16\text{ ns/pF}) C_L$
$CE \rightarrow \overline{TC}$ HIGH to LOW	5	t_{PHL}		180	360	ns	$153\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10			70	140	ns	$59\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			50	100	ns	$42\text{ ns} + (0,16\text{ ns/pF}) C_L$
LOW to HIGH	5	t_{PLH}		170	335	ns	$143\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10			65	135	ns	$54\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			50	100	ns	$42\text{ ns} + (0,16\text{ ns/pF}) C_L$
Output transition times HIGH to LOW	5	t_{THL}		60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$
	10			30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$
	15			20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$
LOW to HIGH	5	t_{TLH}		60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$
	10			30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$
	15			20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$

A.C. CHARACTERISTICS

 $V_{SS} = 0 \text{ V}$; $T_{amb} = 25 \text{ }^\circ\text{C}$; $C_L = 50 \text{ pF}$; input transition times $\leq 20 \text{ ns}$

	V_{DD} V	symbol	min	typ	max	
Minimum clock pulse width; LOW	5	t_{WCPL}	110	55	ns	see also waveforms Figs 6 and 7
	10		35	20	ns	
	15		25	15	ns	
Minimum PL pulse width; HIGH	5	t_{WPLH}	160	80	ns	
	10		55	25	ns	
	15		35	15	ns	
Recovery time for PL	5	t_{RPL}	150	75	ns	
	10		50	25	ns	
	15		35	20	ns	
Set-up times BIN/ \overline{DEC} \rightarrow CP	5	t_{su}	270	135	ns	
	10		90	45	ns	
	15		60	30	ns	
UP/ \overline{DN} \rightarrow CP	5	t_{su}	300	150	ns	
	10		105	55	ns	
	15		75	35	ns	
\overline{CE} \rightarrow CP	5	t_{su}	120	60	ns	
	10		45	25	ns	
	15		35	20	ns	
P_n \rightarrow PL	5	t_{su}	70	35	ns	
	10		20	10	ns	
	15		10	5	ns	
Hold times BIN/ \overline{DEC} \rightarrow CP	5	t_{hold}	45	-90	ns	
	10		15	-30	ns	
	15		10	-20	ns	
UP/ \overline{DN} \rightarrow CP	5	t_{hold}	15	-135	ns	
	10		0	-50	ns	
	15		-5	-35	ns	
\overline{CE} \rightarrow CP	5	t_{hold}	30	-30	ns	
	10		10	-10	ns	
	15		5	-10	ns	
P_n \rightarrow PL	5	t_{hold}	15	-20	ns	
	10		0	-10	ns	
	15		0	-5	ns	
Maximum clock pulse frequency	5	f_{max}	4	8	MHz	
	10		12	25	MHz	
	15		18	35	MHz	

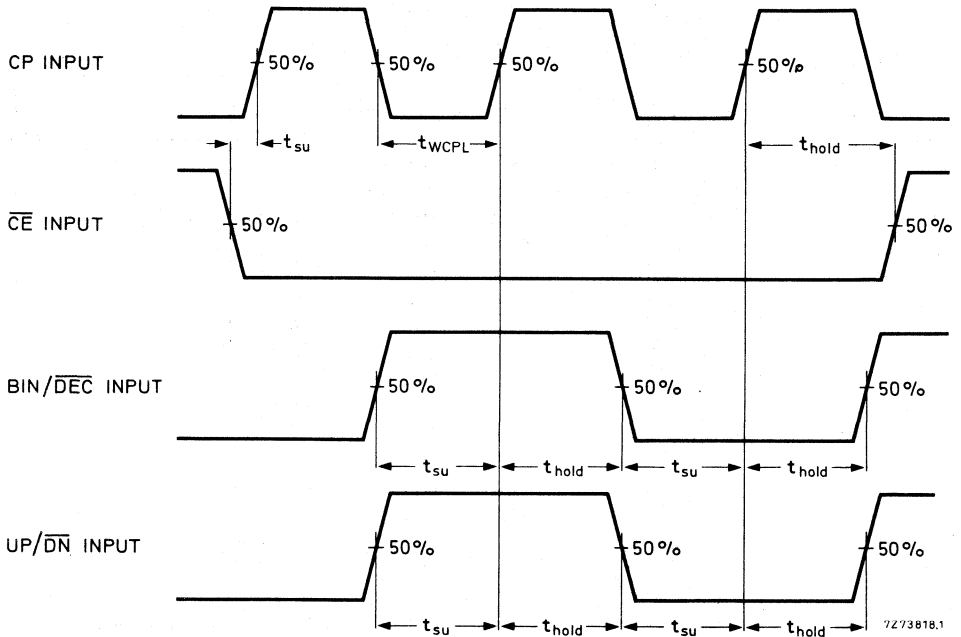


Fig. 6 Waveforms showing minimum pulse width for CP, set-up and hold times for \overline{CE} to CP, BIN/ \overline{DEC} to CP and UP/ \overline{DN} to CP. Set-up and hold times are shown as positive values but may be specified as negative values.

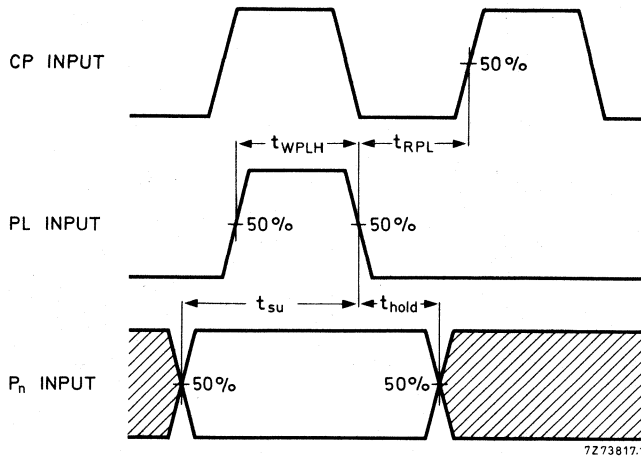
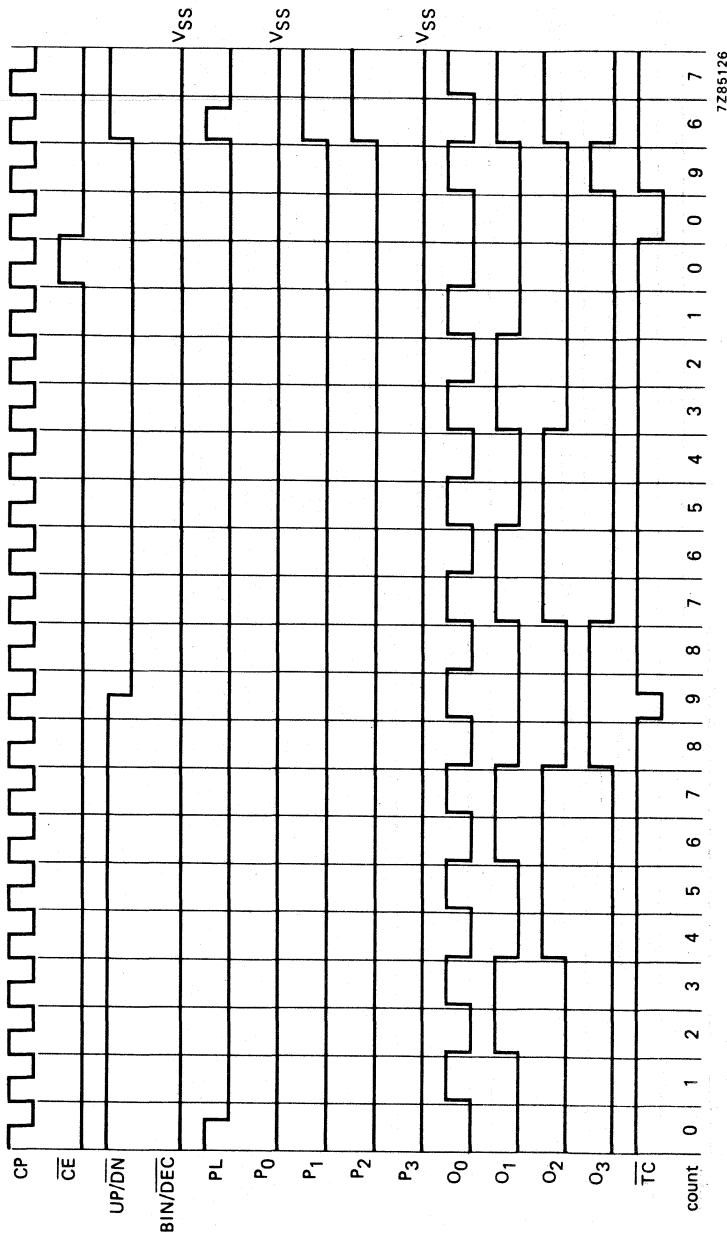


Fig. 7 Waveforms showing minimum pulse width for PL, recovery time for PL, and set-up and hold times for P_n to PL. Set-up and hold times are shown as positive values but may be specified as negative values.



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Fig. 8 Timing diagram; decade mode; P₀ = LOW; P₃ = LOW; BIN/DEC = LOW.

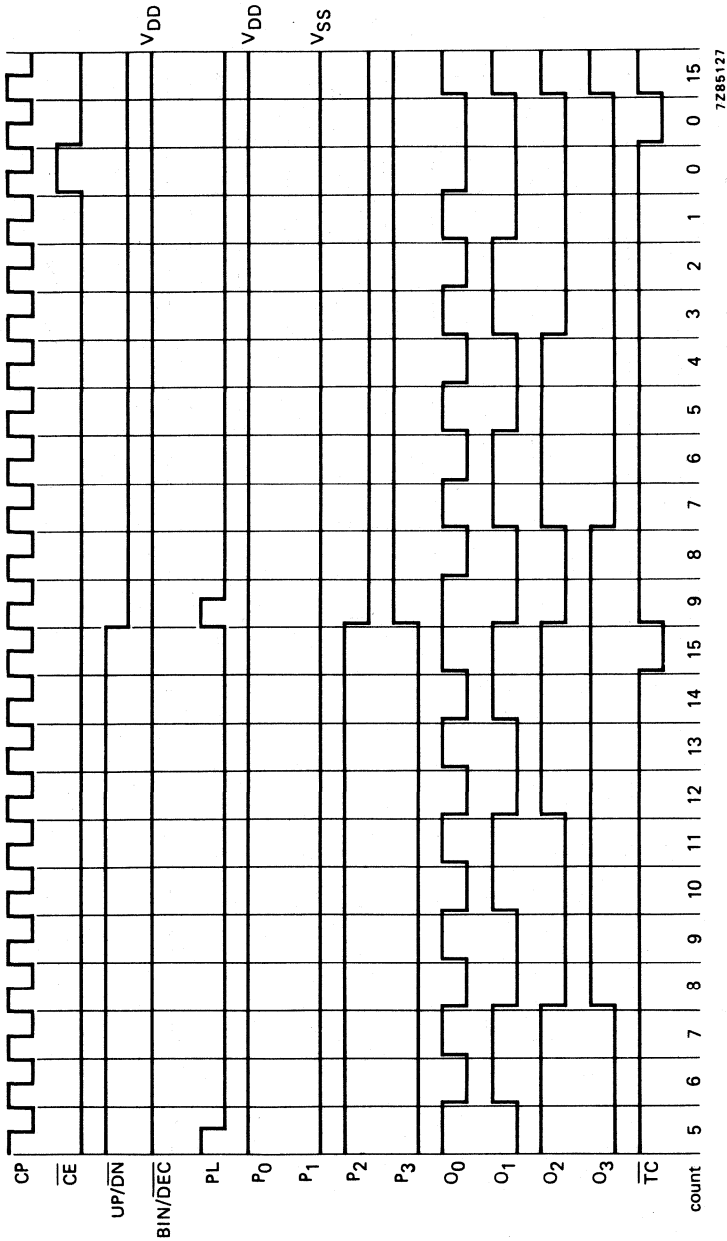


Fig. 9 Timing diagram; binary mode; P₀ = HIGH; P₁ = LOW; BIN/DEC = HIGH.

APPLICATION INFORMATION

Some examples of applications for the HEF4029B are:

- Programmable binary and decade counting/frequency synthesizers - BCD output.
- Analogue-to-digital and digital-to-analogue conversion.
- Up/down binary counting.
- Magnitude and sign generation.
- Up/down decade counting.
- Difference counting.

APPLICATION INFORMATION (continued)

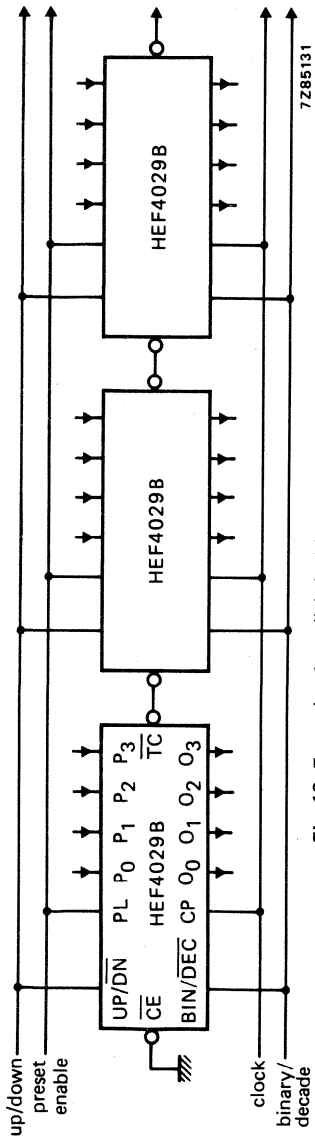


Fig. 10 Example of parallel clocking when cascading HEF4029B ICs.

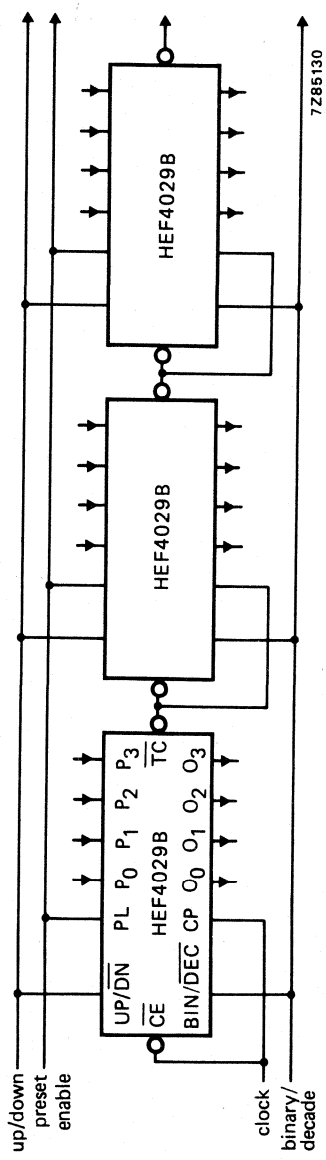


Fig. 11 Example of ripple clocking when cascading HEF4029B ICs. Ripple clocking mode: the up/down control can be changed at any count; the only restriction on changing the up/down control is that the clock input to the first counting stage must be HIGH.

Note

TC lines at all stages after the first may have a negative-going glitch pulse resulting from differential delays of different HEF4029B ICs. These negative-going glitches do not affect proper HEF4029B operation; however if the TC signals are used to trigger other edge-sensitive logic devices, such as flip-flops or counters, the TC signals should be gated with the clock signal using a 2-input OR gate such as HEF4071B.

QUADRUPLE EXCLUSIVE-OR GATE



The HEF4030B provides the positive quadruple exclusive-OR function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

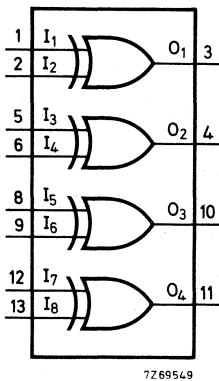


Fig. 1 Functional diagram.

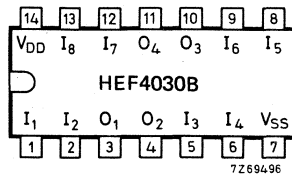


Fig. 2 Pinning diagram.

HEF4030BP: 14-lead DIL; plastic (SOT-27S, T, V).

HEF4030BD: 14-lead DIL; ceramic (SOT-73).

HEF4030BT: 14-lead flat pack; plastic (SO-14; SOT-108A).

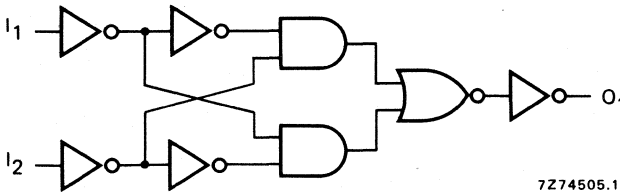


Fig. 3 Logic diagram (one gate).

TRUTH TABLE

I ₁	I ₂	O ₁
L	L	L
H	L	H
L	H	H
H	H	L

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

FAMILY DATA

I_{DD} LIMITS category GATES

} see Family Specifications

A.C. CHARACTERISTICS

 $V_{SS} = 0 \text{ V}$; $T_{amb} = 25 \text{ }^\circ\text{C}$; $C_L = 50 \text{ pF}$; input transition times $\leq 20 \text{ ns}$

	V_{DD} V	symbol	typ.	max.		typical extrapolation formula
Propagation delays $I_n \rightarrow O_n$ HIGH to LOW	5	t _{PHL}	85	175	ns	$57 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
	10		35	75	ns	$23 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
	15		30	55	ns	$22 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
LOW to HIGH	5	t _{PLH}	75	150	ns	$47 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
	10		30	65	ns	$19 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
	15		25	50	ns	$17 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
Output transition times HIGH to LOW	5	t _{THL}	60	120	ns	$10 \text{ ns} + (1,0 \text{ ns/pF}) C_L$
	10		30	60	ns	$9 \text{ ns} + (0,42 \text{ ns/pF}) C_L$
	15		20	40	ns	$6 \text{ ns} + (0,28 \text{ ns/pF}) C_L$
LOW to HIGH	5	t _{TLH}	60	120	ns	$10 \text{ ns} + (1,0 \text{ ns/pF}) C_L$
	10		30	60	ns	$9 \text{ ns} + (0,42 \text{ ns/pF}) C_L$
	15		20	40	ns	$6 \text{ ns} + (0,28 \text{ ns/pF}) C_L$

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$1\,100 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz)
	10	$4\,900 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_o = output freq. (MHz)
	15	$14\,400 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	C_L = load capacitance (pF)
			$\Sigma(f_o C_L)$ = sum of outputs
			V_{DD} = supply voltage (V)

64-STAGE STATIC SHIFT REGISTER



The HEF4031B is an edge-triggered 64-stage static shift register with two serial data inputs (D_A , D_B), a data select input \bar{A}/B , a clock input (CP), a buffered clock output (CO), and buffered outputs from the 64th bit position (O_{63} , \bar{O}_{63}). The output O_{63} is capable of driving one TTL load.

Data from D_A or D_B , as determined by the state of \bar{A}/B , is shifted into the first shift register position and all the data in the register is shifted one position to the right on the LOW to HIGH transition of CP. D_A is selected by a LOW, and D_B by a HIGH on \bar{A}/B . Registers can be cascaded either by connecting all CP inputs together or by driving CP of the most right-hand register with the system clock and connecting CO to CP of the preceding register. When the second technique is used in the recirculating mode, a flip-flop must be used to store O_{63} of the most right-hand register until the most left-hand register is clocked.

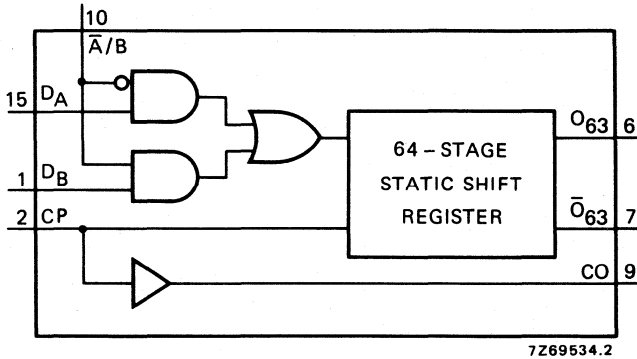


Fig. 1 Functional diagram.

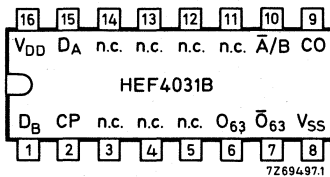


Fig. 2 Pinning diagram.

PINNING

- D_A , D_B data inputs
- \bar{A}/B data select input
- CP clock input (LOW to HIGH edge-triggered)
- CO buffered clock output
- O_{63} buffered output from the 64th stage
- \bar{O}_{63} complementary buffered output from the 64th stage

HEF4031BP: 16-lead DIL; plastic (SOT-38Z).

HEF4031BD: 16-lead DIL; ceramic (SOT-74).

HEF4031BT: 16-lead flat pack; plastic (SO-16; SOT-109A).

FAMILY DATA

I_{DD} LIMITS category LSI

} see Family Specifications.

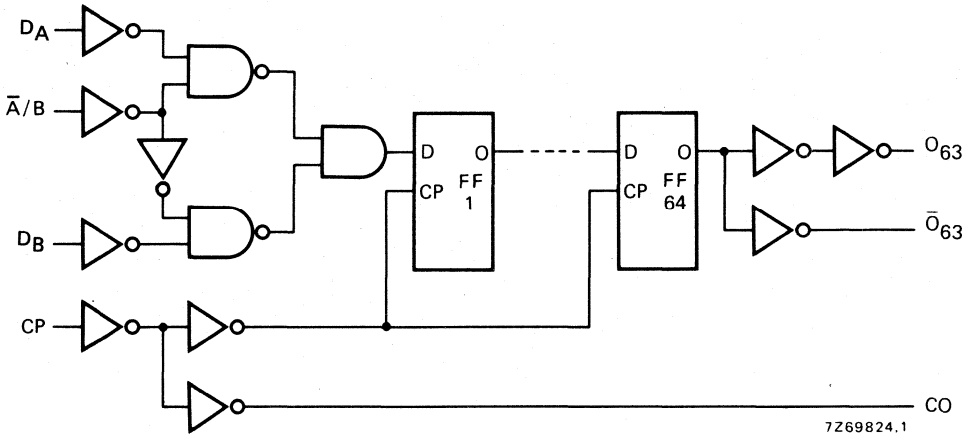


Fig. 3 Logic diagram.

D.C. CHARACTERISTICS

$V_{SS} = 0\text{ V}$; $V_I = V_{SS}$ or V_{DD}

	V_{DD} V	V_{OH} V	V_{OL} V	symbol	T_{amb} (°C)			
					-40 min.	+25 max.	+85 min.	+85 max.
Output (source) current HIGH; O ₆₃	5	4,6		-I _{OH}	1,0	0,85	0,65	mA
	10	9,5		-I _{OH}	3,0	2,5	2,0	mA
	15	13,5		-I _{OH}	10,0	8,5	6,5	mA
Output (sink) current LOW; O ₆₃	5	2,5		-I _{OH}	3,0	2,5	2,0	mA
	4,75		0,4	I _{OL}	2,7	2,3	1,8	mA
	10		0,5	I _{OL}	9,5	8,0	6,3	mA
	15		1,5	I _{OL}	24,0	20,0	16,0	mA

A.C. CHARACTERISTICS

 $V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	symbol	min.	typ.	max.	typical extrapolation formula
Propagation delays						
CP \rightarrow O_{63}	5			180	360 ns	$167\text{ ns} + (0,26\text{ ns/pF}) C_L$
HIGH to LOW	10	tPHL		65	130 ns	$57\text{ ns} + (0,16\text{ ns/pF}) C_L$
	15			45	90 ns	$39\text{ ns} + (0,11\text{ ns/pF}) C_L$
	5			170	340 ns	$148\text{ ns} + (0,45\text{ ns/pF}) C_L$
LOW to HIGH	10	tPLH		65	130 ns	$56\text{ ns} + (0,19\text{ ns/pF}) C_L$
	15			45	90 ns	$39\text{ ns} + (0,13\text{ ns/pF}) C_L$
CP \rightarrow \bar{O}_{63}	5			190	380 ns	$163\text{ ns} + (0,55\text{ ns/pF}) C_L$
HIGH to LOW	10	tPHL		75	150 ns	$64\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			50	100 ns	$42\text{ ns} + (0,16\text{ ns/pF}) C_L$
	5			190	380 ns	$163\text{ ns} + (0,55\text{ ns/pF}) C_L$
LOW to HIGH	10	tPLH		75	150 ns	$64\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			50	100 ns	$42\text{ ns} + (0,16\text{ ns/pF}) C_L$
CP \rightarrow CO	5			70	140 ns	$43\text{ ns} + (0,55\text{ ns/pF}) C_L$
HIGH to LOW	10	tPHL		35	70 ns	$24\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			25	50 ns	$17\text{ ns} + (0,16\text{ ns/pF}) C_L$
	5			55	110 ns	$28\text{ ns} + (0,55\text{ ns/pF}) C_L$
LOW to HIGH	10	tPLH		30	60 ns	$19\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			25	50 ns	$17\text{ ns} + (0,16\text{ ns/pF}) C_L$
Output transition times; O_{63}	5			25	50 ns	$5\text{ ns} + (0,40\text{ ns/pF}) C_L$
HIGH to LOW	10	tTHL		12	24 ns	$3\text{ ns} + (0,18\text{ ns/pF}) C_L$
	15			8	16 ns	$2\text{ ns} + (0,13\text{ ns/pF}) C_L$
	5			40	80 ns	$8\text{ ns} + (0,65\text{ ns/pF}) C_L$
LOW to HIGH	10	tTLH		20	40 ns	$5\text{ ns} + (0,30\text{ ns/pF}) C_L$
	15			13	26 ns	$3\text{ ns} + (0,20\text{ ns/pF}) C_L$
Output transition times; \bar{O}_{63} , CO	5			60	120 ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$
HIGH to LOW	10	tTHL		30	60 ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$
	15			20	40 ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$
	5			60	120 ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$
LOW to HIGH	10	tTLH		30	60 ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$
	15			20	40 ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$

A.C. CHARACTERISTICS

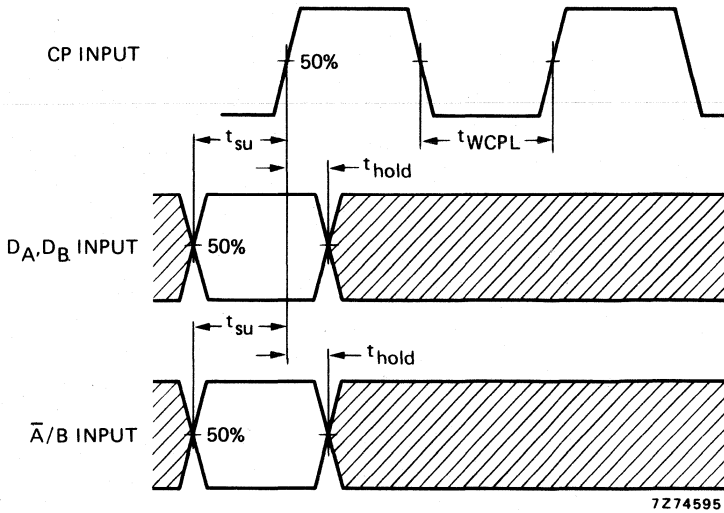
$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	symbol	min.	typ.	max.	typical extrapolation formula
Set-up times $D_A, D_B \rightarrow CP$	5	t_{su}	25	0	ns	} see also waveforms Fig. 4
	10		25	-5	ns	
	15		10	-10	ns	
$\bar{A}/B \rightarrow CP$	5	t_{su}	30	10	ns	
	10		15	0	ns	
	15		10	-5	ns	
Hold times $D_A, D_B \rightarrow CP$	5	t_{hold}	40	10	ns	
	10		40	10	ns	
	15		40	10	ns	
$\bar{A}/B \rightarrow CP$	5	t_{hold}	40	10	ns	
	10		40	10	ns	
	15		40	10	ns	
Minimum clock pulse width; LOW	5	t_{WCPL}	180	90	ns	
	10		70	35	ns	
	15		50	25	ns	
Maximum clock pulse frequency	5	f_{max}	2,5	5	MHz	
	10		7	14	MHz	
	15		10	20	MHz	

A.C. CHARACTERISTICS

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	typical formula for P (μW)	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
Dynamic power dissipation per package (P)	5	$4000 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	10	$19\,000 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$54\,000 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	



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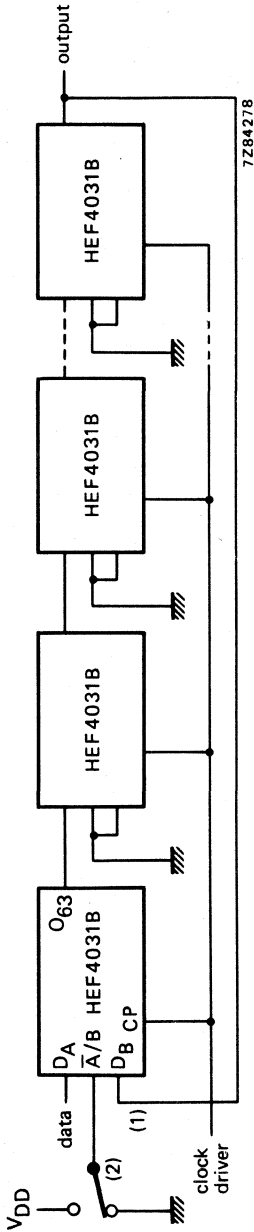
Fig. 4 Waveforms showing minimum clock pulse width, set-up and hold times for D_A , D_B to CP and \bar{A}/B to CP. Set-up and hold times are shown as positive values but may be specified as negative values.

APPLICATION INFORMATION

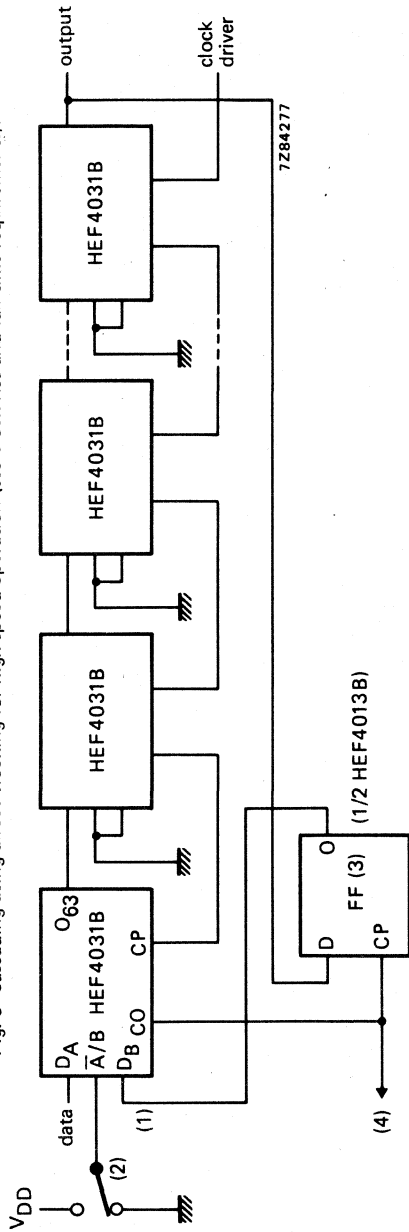
An example of an application for the HEF4031B is:

- Serial shift register.

APPLICATION INFORMATION



(1) Recirculating input.
 (2) Mode control: V_{DD} = recirculation; ground (V_{SS}) = new data.
 Fig. 5 Cascading using direct clocking for high speed operation (see clock rise and fall time requirements).



(1) Recirculating input.
 (2) Mode control: V_{DD} = recirculation; ground (V_{SS}) = new data.
 (3) For recirculation mode only, FF to delay data until first register delayed clocking has occurred.
 (4) Delayed clock-to-clock; new data into first register.
 Fig. 6 Cascading using delayed clocking for reduced clock drive requirements.

4-BIT UNIVERSAL SHIFT REGISTER



The HEF4035B is a fully synchronous edge-triggered 4-bit shift register with a clock input (CP), four synchronous parallel data inputs (P_0 to P_3), two synchronous serial data inputs (J, \bar{K}), a synchronous parallel enable input (PE), buffered parallel outputs from all 4-bit positions (O_0 to O_3), a true/complement input (T/\bar{C}) and an overriding asynchronous master reset input (MR). Each register is of a D-type master-slave flip-flop.

Operation is synchronous (except for MR) and is edge-triggered on the LOW to HIGH transition of the CP input. When PE is HIGH, data is loaded into the register from P_0 to P_3 on the LOW to HIGH transition of CP.

When PE is LOW, data is shifted into the first register position from J and \bar{K} and all the data in the register is shifted one position to the right on the LOW to HIGH transition of CP. D-type entry is obtained by interconnecting J and \bar{K} . When J = HIGH and \bar{K} = LOW the first stage is in the toggle mode. When J = LOW and \bar{K} = HIGH the first stage is in the hold mode.

The outputs (O_0 to O_3) are either inverting or non-inverting, depending on T/\bar{C} state. With T/\bar{C} HIGH, O_0 to O_3 are non-inverting (active HIGH) and when T/\bar{C} is LOW, O_0 to O_3 are inverting (active LOW).

A HIGH on MR resets all four bit positions (O_0 to O_3 = LOW if T/\bar{C} = HIGH, O_0 to O_3 = HIGH if T/\bar{C} = LOW) independent of all other input conditions.

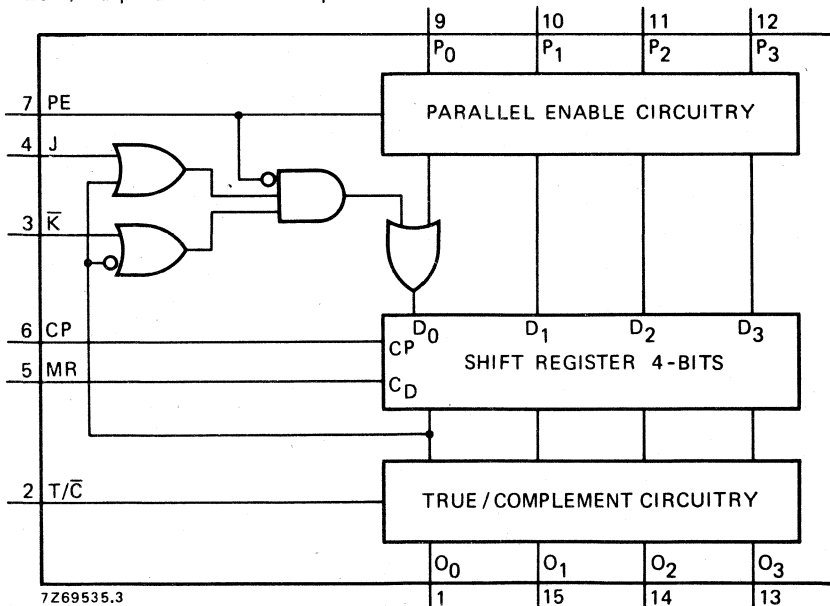


Fig. 1 Functional diagram.

FAMILY DATA

I_{DD} LIMITS category MSI

see Family Specifications

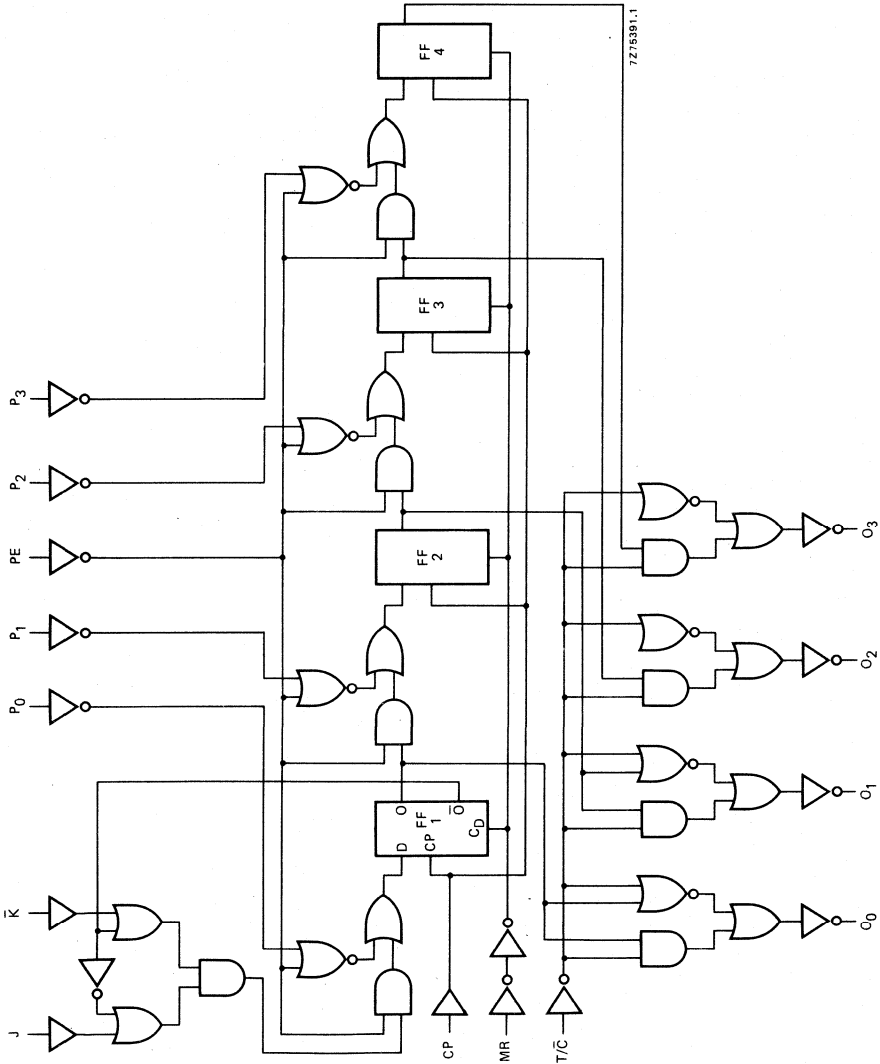


Fig. 2 Logic diagram.

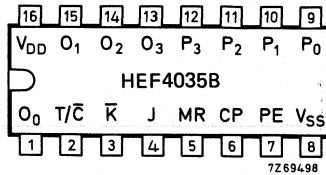


Fig. 3 Pinning diagram.

HEF4035BP: 16-lead DIL; plastic (SOT-38Z).

HEF4035BD: 16-lead DIL; ceramic (SOT-74).

HEF4035BT: 16-lead flat pack; plastic (SO-16; SOT-109A).

PINNING

- | | | | |
|----------------------------------|-----------------------------------|----------------------------------|--|
| PE | parallel enable input | CP | clock input (LOW to HIGH edge-triggered) |
| P ₀ to P ₃ | parallel data inputs | T/ \bar{C} | true/complement input |
| J | first stage J-input (active HIGH) | MR | master reset input |
| \bar{K} | first stage K-input (active LOW) | O ₀ to O ₃ | buffered parallel outputs |

FUNCTION TABLES

Serial operation first stage

inputs				output	mode of operation
CP	J	\bar{K}	MR	O ₀	
\nearrow	H	H	L	H	D flip-flop
\nearrow	L	L	L	L	D flip-flop
\nearrow	H	L	L	\bar{O}_0	toggle
\nearrow	L	H	L	O ₀	no change
X	X	X	H	L	reset

T/ \bar{C} = HIGH; PE = LOW

Parallel operation

CP	inputs				outputs			
	P ₀	P ₁	P ₂	P ₃	O ₀	O ₁	O ₂	O ₃
\nearrow	H	H	H	H	H	H	H	H
\nearrow	L	L	L	L	L	L	L	L

T/ \bar{C} = HIGH; PE = HIGH; MR = LOW

- \nearrow = positive-going transition
- H = HIGH state (the more positive voltage)
- L = LOW state (the less positive voltage)
- X = state is immaterial

A.C. CHARACTERISTICS

 $V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	symbol	min.	typ.	max.	typical extrapolation formula
Propagation delays						
CP \rightarrow O_n	5			170	340 ns	$143\text{ ns} + (0,55\text{ ns/pF}) C_L$
HIGH to LOW	10	tPHL		70	140 ns	$59\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			50	100 ns	$42\text{ ns} + (0,16\text{ ns/pF}) C_L$
	5			150	300 ns	$133\text{ ns} + (0,55\text{ ns/pF}) C_L$
LOW to HIGH	10	tPLH		65	125 ns	$54\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			45	90 ns	$37\text{ ns} + (0,16\text{ ns/pF}) C_L$
	5			175	350 ns	$148\text{ ns} + (0,55\text{ ns/pF}) C_L$
MR \rightarrow O_n	5			175	350 ns	$148\text{ ns} + (0,55\text{ ns/pF}) C_L$
HIGH to LOW	10	tPHL		70	140 ns	$59\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			50	100 ns	$42\text{ ns} + (0,16\text{ ns/pF}) C_L$
	5			160	315 ns	$133\text{ ns} + (0,55\text{ ns/pF}) C_L$
LOW to HIGH	10	tPLH		65	130 ns	$54\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			45	90 ns	$37\text{ ns} + (0,16\text{ ns/pF}) C_L$
	5			115	235 ns	$88\text{ ns} + (0,55\text{ ns/pF}) C_L$
$T/\bar{C} \rightarrow O_n$	5			115	235 ns	$88\text{ ns} + (0,55\text{ ns/pF}) C_L$
HIGH to LOW	10	tPHL		55	105 ns	$44\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			40	80 ns	$32\text{ ns} + (0,16\text{ ns/pF}) C_L$
	5			110	220 ns	$83\text{ ns} + (0,55\text{ ns/pF}) C_L$
LOW to HIGH	10	tPLH		50	100 ns	$39\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			35	75 ns	$27\text{ ns} + (0,16\text{ ns/pF}) C_L$
	5			60	120 ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$
Output transition times						
HIGH to LOW	10	tTHL		30	60 ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$
	15			20	40 ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$
	5			60	120 ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$
LOW to HIGH	10	tTLH		30	60 ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$
	15			20	40 ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$
	5			60	120 ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V _{DD} V	symbol	min.	typ.	max.	
Minimum clock pulse width; LOW	5	t _{WCPL}	90	45	ns	} see also waveforms Figs 4 and 5
	10		35	20	ns	
	15		25	15	ns	
Minimum MR pulse width; HIGH	5	t _{WMRH}	65	30	ns	
	10		30	15	ns	
	15		20	10	ns	
Recovery time for MR	5	t _{RMR}	110	55	ns	
	10		40	20	ns	
	15		30	15	ns	
Set-up times P _n → CP	5	t _{su}	215	105	ns	
	10		80	40	ns	
	15		50	25	ns	
PE → CP	5	t _{su}	200	100	ns	
	10		80	40	ns	
	15		55	25	ns	
J, \bar{K} → CP	5	t _{su}	210	105	ns	
	10		80	40	ns	
	15		50	25	ns	
Hold times P _n → CP	5	t _{hold}	25	10	ns	
	10		20	10	ns	
	15		20	10	ns	
PE → CP	5	t _{hold}	15	-5	ns	
	10		10	-5	ns	
	15		5	-5	ns	
J, \bar{K} → CP	5	t _{hold}	10	-5	ns	
	10		10	0	ns	
	15		10	0	ns	
Maximum clock pulse frequency	5	f _{max}	5	10	MHz	
	10		12	25	MHz	
	15		18	35	MHz	

	V _{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	1100 f _i + Σ(f _o C _L) × V _{DD} ²	f _i = input freq. (MHz)
	10	4700 f _i + Σ(f _o C _L) × V _{DD} ²	f _o = output freq. (MHz)
	15	13 000 f _i + Σ(f _o C _L) × V _{DD} ²	C _L = load cap. (pF)
			Σ(f _o C _L) = sum of outputs
			V _{DD} = supply voltage (V)

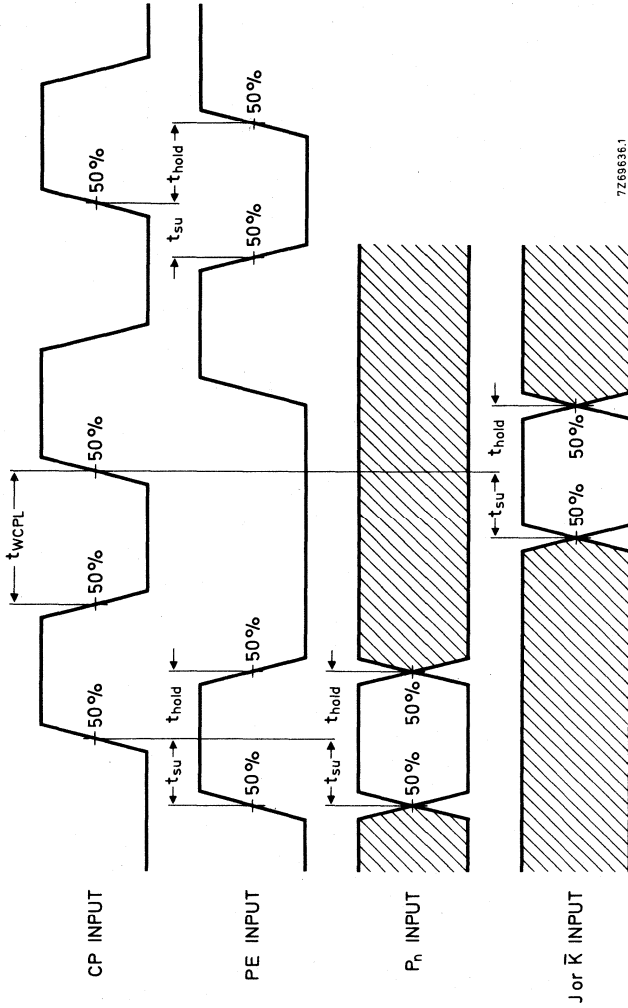


Fig. 4 Waveforms showing minimum clock pulse width, set-up times, hold times. Set-up times and hold times are shown as positive values but may be specified as negative values.

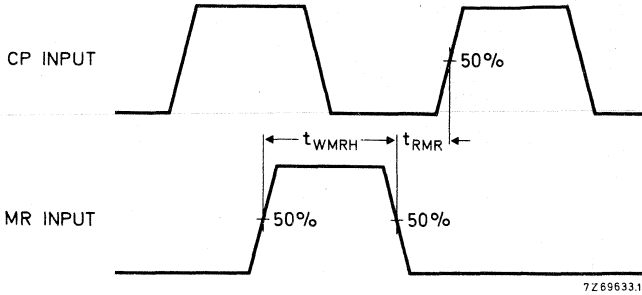


Fig. 5 Waveforms showing minimum MR pulse width and MR recovery time.

APPLICATION INFORMATION

Some examples of applications for the HEF4035B are:

- Counters, registers, arithmetic-unit registers, shift-left/shift-right registers.
- Serial-to-parallel/parallel-to-serial conversions.
- Sequence generation.
- Control circuits.
- Code conversion.

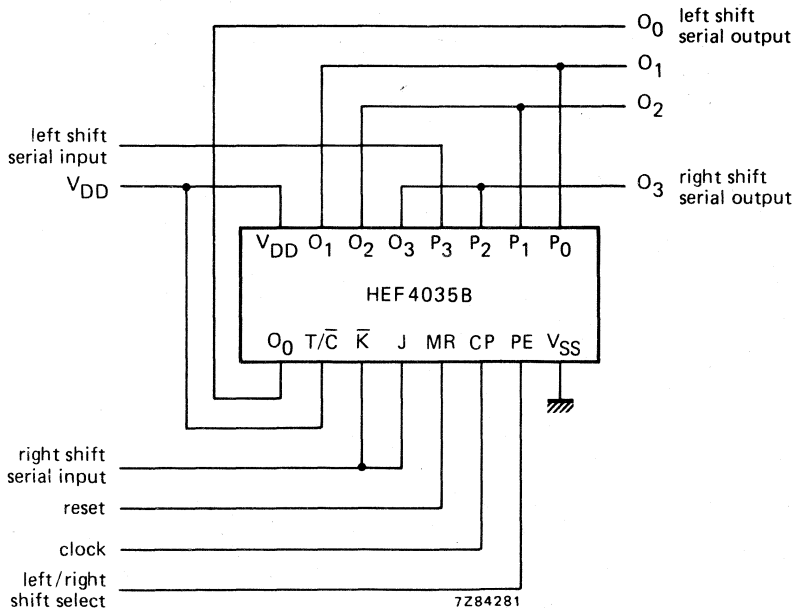


Fig. 6 Shift-left/shift-right register.

12-STAGE BINARY COUNTER



The HEF4040B is a 12-stage binary ripple counter with a clock input (\overline{CP}), an overriding asynchronous master reset input (MR) and twelve fully buffered outputs (O_0 to O_{11}). The counter advances on the HIGH to LOW transition of \overline{CP} . A HIGH on MR clears all counter stages and forces all outputs LOW, independent of \overline{CP} . Each counter stage is a static toggle flip-flop.

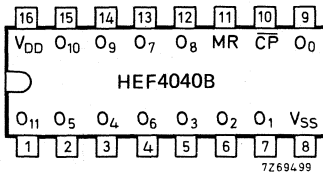
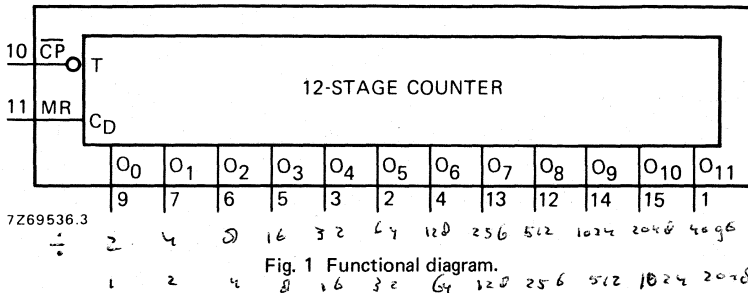


Fig. 2 Pinning diagram.

HEF4040BP: 16-lead DIL; plastic (SOT-38Z).
 HEF4040BD: 16-lead DIL; ceramic (SOT-74).
 HEF4040BT: 16-lead flat pack; plastic (SO-16; SOT-109A).

PINNING

\overline{CP} clock input (HIGH to LOW edge-triggered)
 MR master reset input (active HIGH)
 O_0 to O_{11} parallel outputs

APPLICATION INFORMATION

Some examples of applications for the HEF4040B are:

- Frequency dividing circuits
- Time delay circuits
- Control counters

FAMILY DATA

I_{DD} LIMITS category MSI

see Family Specifications

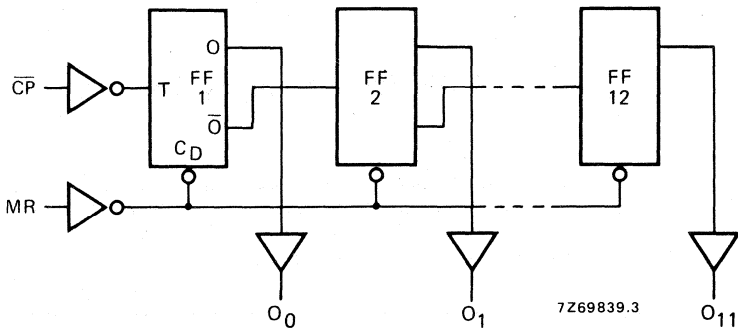


Fig. 3 Logic diagram.

A.C. CHARACTERISTICS

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^\circ\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

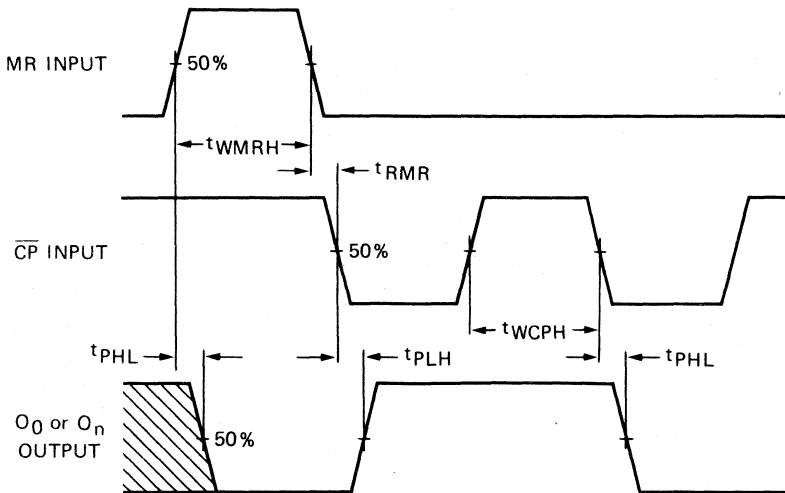
	V_{DD} V	symbol	min.	typ.	max.	typical extrapolation formula		
Propagation delays $\overline{CP} \rightarrow O_0$ HIGH to LOW	5	t _{PHL}		105	210	ns	78 ns + (0,55 ns/pF) C_L	
	10		45	90	ns	34 ns + (0,23 ns/pF) C_L		
	15		30	65	ns	22 ns + (0,16 ns/pF) C_L		
	LOW to HIGH	5	t _{PLH}		105	210	ns	78 ns + (0,55 ns/pF) C_L
		10		50	95	ns	39 ns + (0,23 ns/pF) C_L	
		15		35	70	ns	27 ns + (0,16 ns/pF) C_L	
$O_n \rightarrow O_{n+1}$ HIGH to LOW	5	t _{PHL}		80	160	ns	53 ns + (0,55 ns/pF) C_L	
	10		30	60	ns	19 ns + (0,23 ns/pF) C_L		
	15		20	40	ns	12 ns + (0,16 ns/pF) C_L		
	LOW to HIGH	5	t _{PLH}		70	140	ns	43 ns + (0,55 ns/pF) C_L
		10		25	50	ns	14 ns + (0,23 ns/pF) C_L	
		15		20	40	ns	12 ns + (0,16 ns/pF) C_L	
$MR \rightarrow O_n$ HIGH to LOW	5	t _{PHL}		180	360	ns	153 ns + (0,55 ns/pF) C_L	
	10		90	180	ns	79 ns + (0,23 ns/pF) C_L		
	15		70	140	ns	62 ns + (0,16 ns/pF) C_L		
Output transition times HIGH to LOW	5	t _{THL}		60	120	ns	10 ns + (1,0 ns/pF) C_L	
	10		30	60	ns	9 ns + (0,42 ns/pF) C_L		
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L		
	LOW to HIGH	5	t _{TLH}		60	120	ns	10 ns + (1,0 ns/pF) C_L
		10		30	60	ns	9 ns + (0,42 ns/pF) C_L	
		15		20	40	ns	6 ns + (0,28 ns/pF) C_L	

A.C. CHARACTERISTICS

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	symbol	min.	typ.	max.	
Minimum clock pulse width; HIGH	5	t_{WCPH}	50	25	ns	see also waveforms Fig. 4
	10		25	15	ns	
	15		20	10	ns	
Minimum MR pulse width; HIGH	5	t_{WMRH}	130	65	ns	
	10		95	50	ns	
	15		90	45	ns	
Recovery time for MR	5	t_{RMR}	115	60	ns	
	10		65	35	ns	
	15		55	25	ns	
Maximum clock pulse frequency	5	f_{max}	5	10	MHz	
	10		13	25	MHz	
	15		18	35	MHz	

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$600 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz)
	10	$2800 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_o = output freq. (MHz)
	15	$8200 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	C_L = load cap. (pF)
			$\Sigma(f_o C_L)$ = sum of outputs
			V_{DD} = supply voltage (V)



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Fig. 4 Waveforms showing propagation delays for MR to O_n and CP to O₀, minimum MR and CP pulse widths.

QUADRUPLE TRUE/COMPLEMENT BUFFER



The HEF4041B is a quadruple true/complement buffer which provides both an inverted active LOW output (\bar{O}) and a non-inverted active HIGH output (O) for each input (I).
The buffers exhibit high current output capability suitable for driving TTL or high capacitive loads.

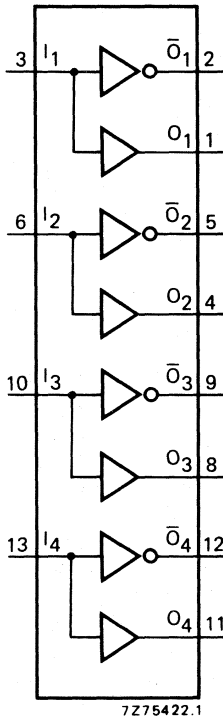


Fig. 1 Functional diagram.

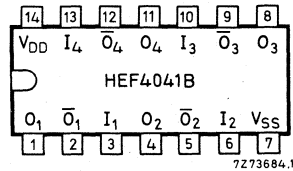


Fig. 2 Pinning diagram.

HEF4041BP: 14-lead DIL; plastic (SOT-27S,T,V).
HEF4041BD: 14-lead DIL; ceramic (SOT-73).
HEF4041BT: 14-lead flat pack; plastic (SO-14; SOT-108A).

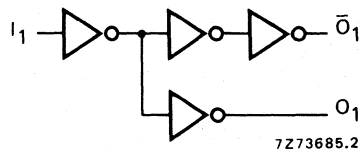


Fig. 3 Logic diagram (one buffer).

APPLICATION INFORMATION

Some examples of applications for the HEF4041B are:

- LOCOS to DTL/TTL converter
- High current sink and source driver

FAMILY DATA

I_{DD} LIMITS category BUFFERS } see Family Specifications

HEF4041B

buffers

D.C. CHARACTERISTICS

$V_{SS} = 0\text{ V}$; $V_I = V_{SS}$ or V_{DD}

	V_{DD} V	V_{OH} V	V_{OL} V	symbol	T_{amb} (°C)				
					-40 min.	max.	+25 min. typ.	+85 min. max.	
Output (source) current HIGH	5	4,6		$-I_{OH}$	1,6	1,3	2,6	1,0	mA
	10	9,5			4,5	3,6	7,0	2,7	mA
	15	13,5			16,0	14,0	30,0	10,0	mA
HIGH	5	2,5		$-I_{OH}$	5,0	4,0	8,0	3,0	mA
Output (sink) current LOW	4,75		0,4	I_{OL}	2,0	1,7	4,0	1,35	mA
	10		0,5		7,5	6,0	12,0	4,5	mA
	15		1,5		23,0	20,0	35,0	15,0	mA

A.C. CHARACTERISTICS

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ °C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	symbol	min.	typ.	max.	typical extrapolation formula	
Propagation delays $I_n \rightarrow O_n$ HIGH to LOW	5	tPHL	30	65	ns	$17\text{ ns} + (0,27\text{ ns/pF}) C_L$	
	10		20	40	ns	$14\text{ ns} + (0,11\text{ ns/pF}) C_L$	
	15		15	30	ns	$12\text{ ns} + (0,08\text{ ns/pF}) C_L$	
	LOW to HIGH	5	tPLH	30	55	ns	$17\text{ ns} + (0,27\text{ ns/pF}) C_L$
		10		15	30	ns	$9\text{ ns} + (0,11\text{ ns/pF}) C_L$
		15		10	20	ns	$7\text{ ns} + (0,08\text{ ns/pF}) C_L$
$I_n \rightarrow \bar{O}_n$ HIGH to LOW	5	tPHL	35	75	ns	$22\text{ ns} + (0,27\text{ ns/pF}) C_L$	
	10		20	40	ns	$14\text{ ns} + (0,11\text{ ns/pF}) C_L$	
	15		15	30	ns	$12\text{ ns} + (0,08\text{ ns/pF}) C_L$	
	LOW to HIGH	5	tPLH	35	75	ns	$22\text{ ns} + (0,27\text{ ns/pF}) C_L$
		10		20	40	ns	$14\text{ ns} + (0,11\text{ ns/pF}) C_L$
		15		15	30	ns	$12\text{ ns} + (0,08\text{ ns/pF}) C_L$
Output transition times $O_n \rightarrow \bar{O}_n$ HIGH to LOW	5	tTHL	25	50	ns	$5\text{ ns} + (0,40\text{ ns/pF}) C_L$	
	10		12	25	ns	$2\text{ ns} + (0,21\text{ ns/pF}) C_L$	
	15		8	20	ns	$1\text{ ns} + (0,14\text{ ns/pF}) C_L$	
	LOW to HIGH	5	tTLH	25	45	ns	$5\text{ ns} + (0,40\text{ ns/pF}) C_L$
		10		12	25	ns	$2\text{ ns} + (0,21\text{ ns/pF}) C_L$
		15		8	20	ns	$1\text{ ns} + (0,14\text{ ns/pF}) C_L$

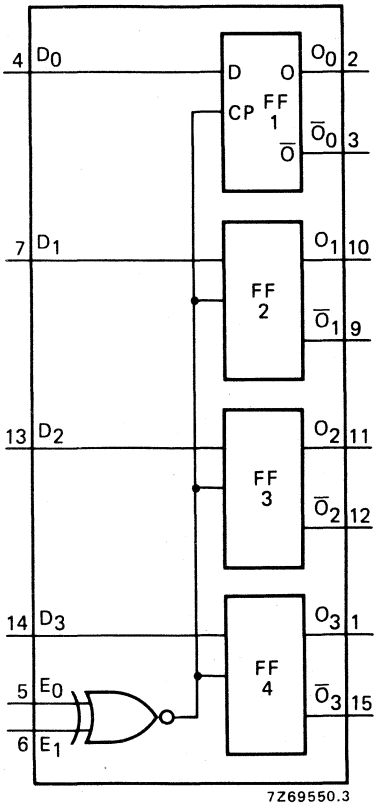
	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$3100 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz)
	10	$12700 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_o = output freq. (MHz)
	15	$33800 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	C_L = load capacitance (pF)
			$\Sigma(f_o C_L)$ = sum of outputs
			V_{DD} = supply voltage (V)

QUADRUPLE D-LATCH



The HEF4042B is a 4-bit latch with four data inputs (D_0 to D_3), four buffered latch outputs (O_0 to O_3), four buffered complementary latch outputs (\bar{O}_0 to \bar{O}_3) and two common enable inputs (E_0 and E_1). Information on D_0 to D_3 is transferred to O_0 to O_3 while both E_0 and E_1 are in the same state, either HIGH or LOW. O_0 to O_3 follow D_0 to D_3 as long as both E_0 and E_1 remain in the same state. When E_0 and E_1 are different, D_0 to D_3 do not affect O_0 to O_3 and the information in the latch is stored.

\bar{O}_0 to \bar{O}_3 are always the complement of O_0 to O_3 . The exclusive-OR input structure allows the choice of either polarity for E_0 and E_1 . With one enable input HIGH, the other enable input is active HIGH; with one enable input LOW, the other enable input is active LOW.



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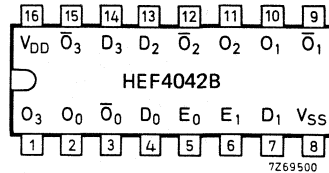


Fig. 2 Pinning diagram.

HEF4042BP: 16-lead DIL; plastic (SOT-38Z).

HEF4042BD: 16-lead DIL; ceramic (SOT-74).

HEF4042BT: 16-lead flat pack; plastic (SO-16; SOT-109A).

PINNING

D_0 to D_3 data inputs

E_0 and E_1 enable inputs

O_0 to O_3 parallel latch outputs

\bar{O}_0 to \bar{O}_3 complementary parallel latch outputs

APPLICATION INFORMATION

Some examples of applications for the HEF4042B are:

- Buffer storage
- Holding register

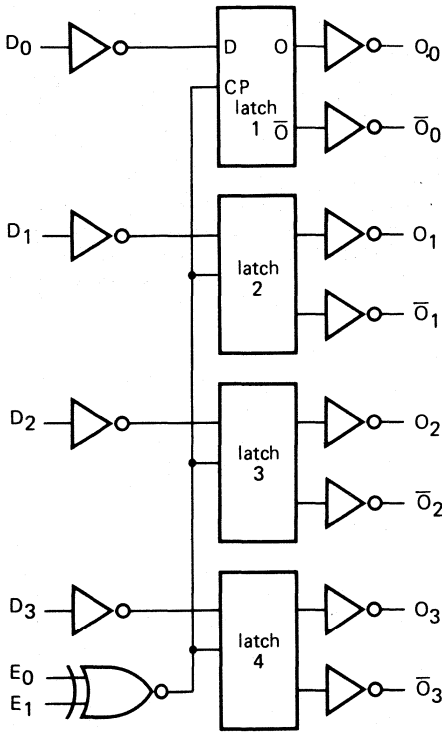
Fig. 1 Functional diagram.

FAMILY DATA

I_{DD} LIMITS category MSI

} see Family Specifications





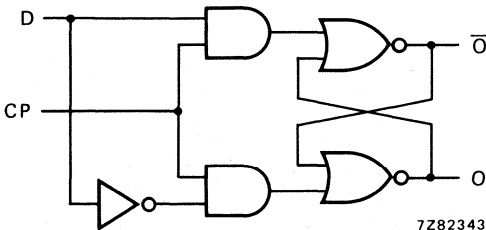
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Fig. 3 Logic diagram.

FUNCTION TABLE

E ₀	E ₁	output O _n
L	L	D _n
L	H	latched
H	L	latched
H	H	D _n

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage).



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Fig. 4 Logic diagram (one latch).

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V _{DD} V	symbol	min.	typ.	max.	typical extrapolation formula	
Propagation delays D → O, \bar{O} HIGH to LOW	5	t _{PHL}		95	190	ns	67 ns + (0,55 ns/pF) C _L
	10		40	80	ns	28 ns + (0,23 ns/pF) C _L	
	15		30	55	ns	22 ns + (0,16 ns/pF) C _L	
LOW to HIGH	5	t _{PLH}		85	175	ns	57 ns + (0,55 ns/pF) C _L
	10		40	75	ns	28 ns + (0,23 ns/pF) C _L	
	15		30	60	ns	22 ns + (0,16 ns/pF) C _L	
E → O, \bar{O} HIGH to LOW	5	t _{PHL}		130	260	ns	102 ns + (0,55 ns/pF) C _L
	10		50	105	ns	38 ns + (0,23 ns/pF) C _L	
	15		35	75	ns	27 ns + (0,16 ns/pF) C _L	
LOW to HIGH	5	t _{PLH}		120	245	ns	92 ns + (0,55 ns/pF) C _L
	10		50	105	ns	38 ns + (0,23 ns/pF) C _L	
	15		35	75	ns	27 ns + (0,16 ns/pF) C _L	
Output transition times HIGH to LOW	5	t _{THL}		60	120	ns	10 ns + (1,0 ns/pF) C _L
	10		30	60	ns	9 ns + (0,42 ns/pF) C _L	
	15		20	40	ns	6 ns + (0,28 ns/pF) C _L	
LOW to HIGH	5	t _{TLH}		60	120	ns	10 ns + (1,0 ns/pF) C _L
	10		30	60	ns	9 ns + (0,42 ns/pF) C _L	
	15		20	40	ns	6 ns + (0,28 ns/pF) C _L	
Set-up time D → E	5	t _{su}	30	10		ns	see also waveforms Figs 5 and 6
	10		20	5		ns	
	15		20	5		ns	
Hold time D → E	5	t _{hold}	15	-5		ns	
	10		15	0		ns	
	15		15	0		ns	
Minimum enable pulse width	5	t _{WE}	90	45		ns	
	10		40	20		ns	
	15		30	15		ns	

	V _{DD} V	typical formula for P (W)	where f _i = input freq. (MHz) f _o = output freq. (MHz) C _L = load capacitance (pF) Σ(f _o C _L) = sum of outputs V _{DD} = supply voltage (V)
Dynamic power dissipation per package (P)	5	3800 f _i + Σ(f _o C _L) × V _{DD} ²	
	10	15700 f _i + Σ(f _o C _L) × V _{DD} ²	
	15	41100 f _i + Σ(f _o C _L) × V _{DD} ²	

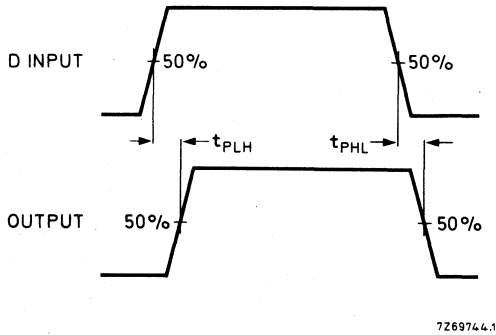
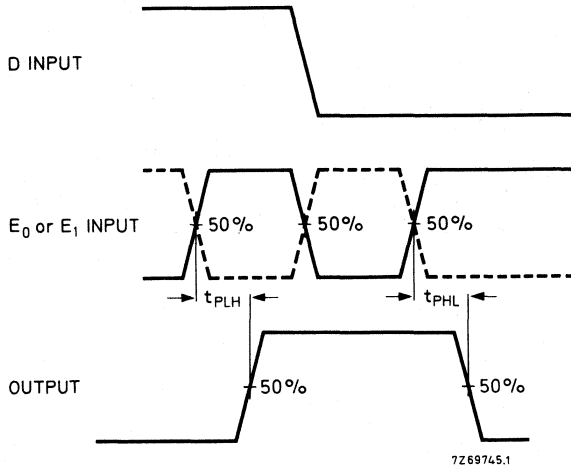


Fig. 5 Waveforms showing propagation delays for D to O, with latch enabled.

Note

Either E₀ or E₁ is held HIGH or LOW while the other enable input is pulsed as the function table shows.

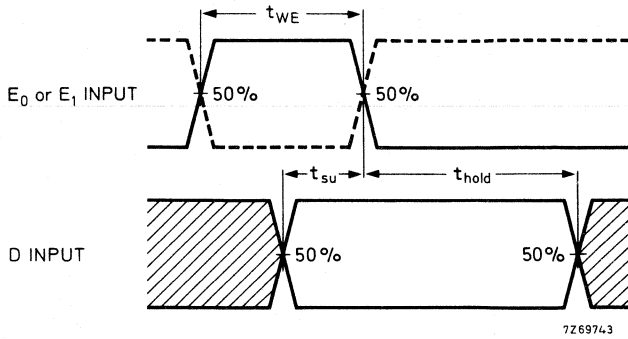


Fig. 6 Waveforms showing minimum enable pulse width, set-up time and hold time for E and D. Set-up and hold-times are shown as positive values but may be specified as negative values.

QUADRUPLE R/S LATCH WITH 3-STATE OUTPUTS



The HEF4043B is a quadruple R/S latch with 3-state outputs with a common output enable input (EO). Each latch has an active HIGH set input (S_0 to S_3), an active HIGH reset input (R_0 to R_3) and an active HIGH 3-state output (O_0 to O_3).

When EO is HIGH, the state of the latch output (O_n) can be determined from the function table below. When EO is LOW, the latch outputs are in the high impedance OFF-state. EO does not affect the state of the latch.

The high impedance off-state feature allows common bussing of the outputs.

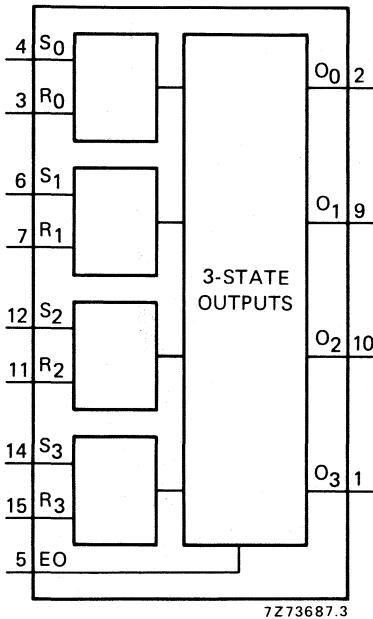


Fig. 1 Functional diagram.

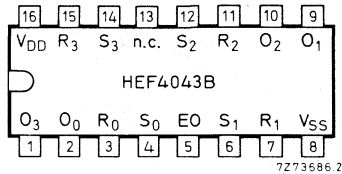


Fig. 2 Pinning diagram.

- HEF4043BP: 16-lead DIL; plastic (SOT-38Z).
- HEF4043BD: 16-lead DIL; ceramic (SOT-74).
- HEF4043BT: 16-lead flat pack; plastic (SO-16; SOT-109A).

PINNING

- EO common output enable input
- S_0 to S_3 set inputs (active HIGH)
- R_0 to R_3 reset inputs (active HIGH)
- O_0 to O_3 3-state buffered latch outputs

FUNCTION TABLE

EO	inputs		output O_n
	S_n	R_n	
L	X	X	Z
H	L	H	L
H	H	X	H
H	L	L	latched

- H = HIGH state (the more positive voltage)
- L = LOW state (the less positive voltage)
- X = state immaterial
- Z = high impedance state

FAMILY DATA

I_{DD} LIMITS category MSI

} see Family Specifications

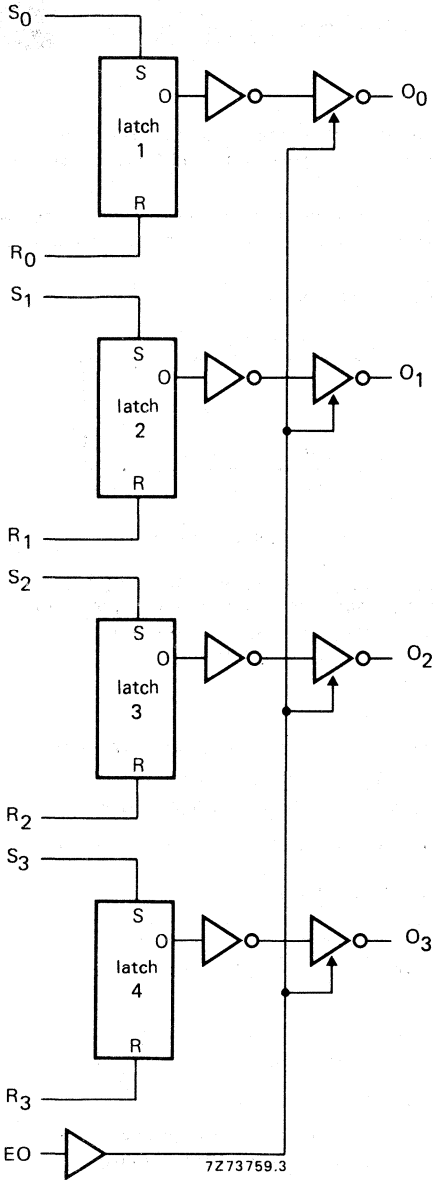


Fig. 3 Logic diagram.

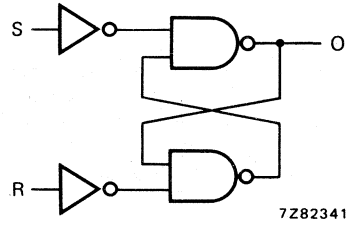


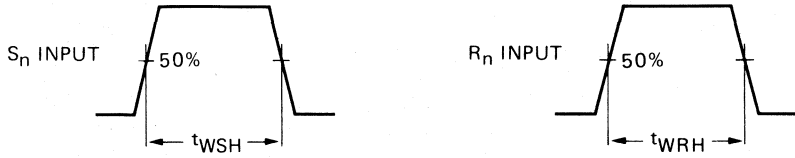
Fig. 4 Logic diagram (one latch).

A.C. CHARACTERISTICS

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^\circ\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	symbol	min.	typ.	max.	typical extrapolation formula					
Propagation delays $R_n \rightarrow O_n$ HIGH to LOW	5	tPHL		90	180 ns	$63\text{ ns} + (0,55\text{ ns/pF}) C_L$					
	10		35	70 ns	$24\text{ ns} + (0,23\text{ ns/pF}) C_L$						
	15		25	50 ns	$17\text{ ns} + (0,16\text{ ns/pF}) C_L$						
$S_n \rightarrow O_n$ LOW to HIGH	5	tPLH		65	135 ns	$38\text{ ns} + (0,55\text{ ns/pF}) C_L$					
	10		25	50 ns	$14\text{ ns} + (0,23\text{ ns/pF}) C_L$						
	15		15	35 ns	$7\text{ ns} + (0,16\text{ ns/pF}) C_L$						
Output transition times	5	tTHL		60	120 ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$					
	10		30	60 ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$						
	15		20	40 ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$						
	5	tTLH		60	120 ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$					
	10		30	60 ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$						
	15		20	40 ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$						
3-state propagation delays											
							Output disable times $EO \rightarrow O_n$ HIGH	5	45	90 ns	
								10	20	35 ns	
								15	10	25 ns	
							LOW	5	50	100 ns	
								10	20	40 ns	
15	10	25 ns									
Output enable times $EO \rightarrow O_n$ HIGH	5	tPZH		25	50 ns						
	10		15	30 ns							
	15		10	25 ns							
	LOW	5	tPZL		40	80 ns					
		10		20	45 ns						
		15		15	35 ns						
Minimum S_n pulse width; HIGH	5	tWSH	30	15	ns	} see also waveforms Fig. 5					
	10		20	10	ns						
	15		16	8	ns						
Minimum R_n pulse width; HIGH	5	tWRH	30	15	ns						
	10		20	10	ns						
	15		16	8	ns						

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$1100 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz)
	10		f_o = output freq. (MHz)
	15		C_L = load capacitance (pF)
			$\Sigma(f_o C_L)$ = sum of outputs
			V_{DD} = supply voltage (V)



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Fig. 5 Waveforms showing minimum S_n and R_n pulse widths.

APPLICATION INFORMATION

An example of application for the HEF4043B is:

- Four-bit storage with output enable

QUADRUPLE R/S LATCH WITH 3-STATE OUTPUTS



The HEF4044B is a quadruple R/S latch with 3-state outputs with a common output enable input (EO). Each latch has an active LOW set input (\bar{S}_0 to \bar{S}_3), an active LOW reset input (\bar{R}_0 to \bar{R}_3) and an active HIGH 3-state output (O_0 to O_3).

When EO is HIGH, the state of the latch output (O_n) can be determined from the function table below. When EO is LOW, the latch outputs are in the high impedance OFF-state. EO does not affect the state of the latch.

The high impedance off-state feature allows common busing of the outputs.

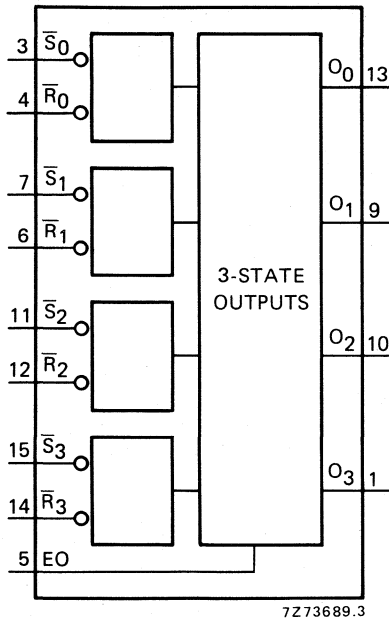


Fig. 1 Functional diagram.

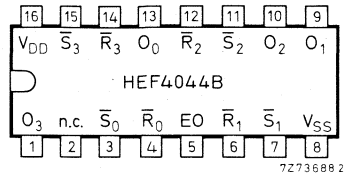


Fig. 2 Pinning diagram.

HEF4044BP: 16-lead DIL; plastic (SOT-38Z).
 HEF4044BD: 16-lead DIL; ceramic (SOT-74).
 HEF4044BT: 16-lead flat pack; plastic (SO-16; SOT-109A).

PINNING

EO common output enable input
 \bar{S}_0 to \bar{S}_3 set inputs (active LOW)
 \bar{R}_0 to \bar{R}_3 reset inputs (active LOW)
 O_0 to O_3 3-state buffered latch outputs

FUNCTION TABLE

EO	inputs		output O_n
	S_n	R_n	
L	X	X	Z
H	L	H	H
H	X	L	L
H	H	H	latched

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

X = state immaterial

Z = high impedance OFF-state

FAMILY DATA

I_{DD} LIMITS category MSI

see Family Specifications

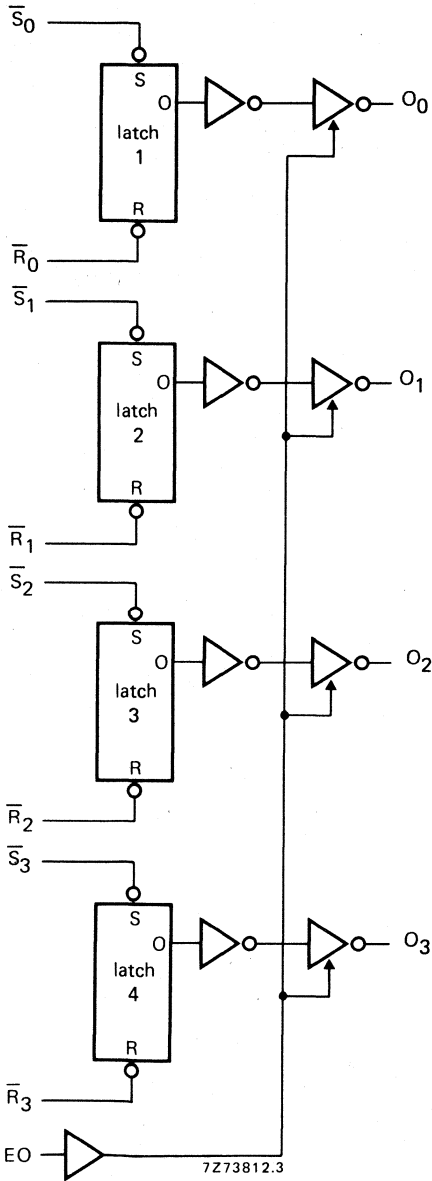


Fig. 3 Logic diagram.

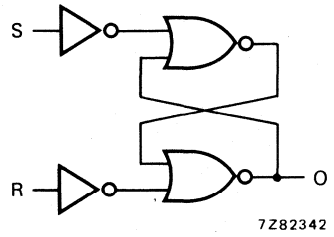


Fig. 4 Logic diagram (one latch).

A.C. CHARACTERISTICS

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^\circ\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	symbol	min.	typ.	max.	typical extrapolation formula	
Propagation delays $\bar{R}_n \rightarrow O_n$ HIGH to LOW	5			90	185	ns	$63\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10	t _{PHL}		40	80	ns	$29\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			30	60	ns	$22\text{ ns} + (0,16\text{ ns/pF}) C_L$
5				90	180	ns	$63\text{ ns} + (0,55\text{ ns/pF}) C_L$
$\bar{S}_n \rightarrow O_n$ LOW to HIGH	10	t _{PLH}		40	80	ns	$29\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			30	60	ns	$22\text{ ns} + (0,16\text{ ns/pF}) C_L$
	5				60	120	ns
Output transition times HIGH to LOW	10	t _{THL}		30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$
	15			20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$
	5				60	120	ns
LOW to HIGH	10	t _{TLH}		30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$
	15			20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$
	3-state propagation delays						
Output disable times $EO \rightarrow O_n$ HIGH	5	t _{PHZ}		50	100	ns	
	10			30	60	ns	
	15			25	50	ns	
LOW	5	t _{PLZ}		30	60	ns	
	10			25	45	ns	
	15			20	40	ns	
Output enable times $EO \rightarrow O_n$ HIGH	5	t _{PZH}		50	100	ns	
	10			25	50	ns	
	15			20	40	ns	
LOW	5	t _{PZL}		50	95	ns	
	10			25	45	ns	
	15			20	35	ns	
Minimum \bar{S}_n pulse width; LOW	5	t _{WSL}		30	15	ns	} see also waveforms Fig. 5
	10			20	10	ns	
	15			16	8	ns	
Minimum \bar{R}_n pulse width; LOW	5	t _{WRL}		30	15	ns	
	10			20	10	ns	
	15			16	8	ns	

	V_{DD} V	typical formula for P (μW)	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
Dynamic power dissipation per package (P)	5	$1300 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	10	$5200 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$12900 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

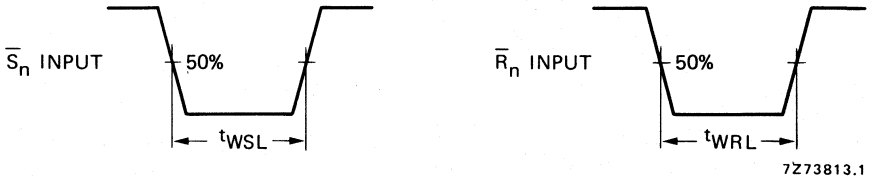


Fig. 5 Waveforms showing minimum \overline{S}_n and \overline{R}_n pulse widths.

APPLICATION INFORMATION

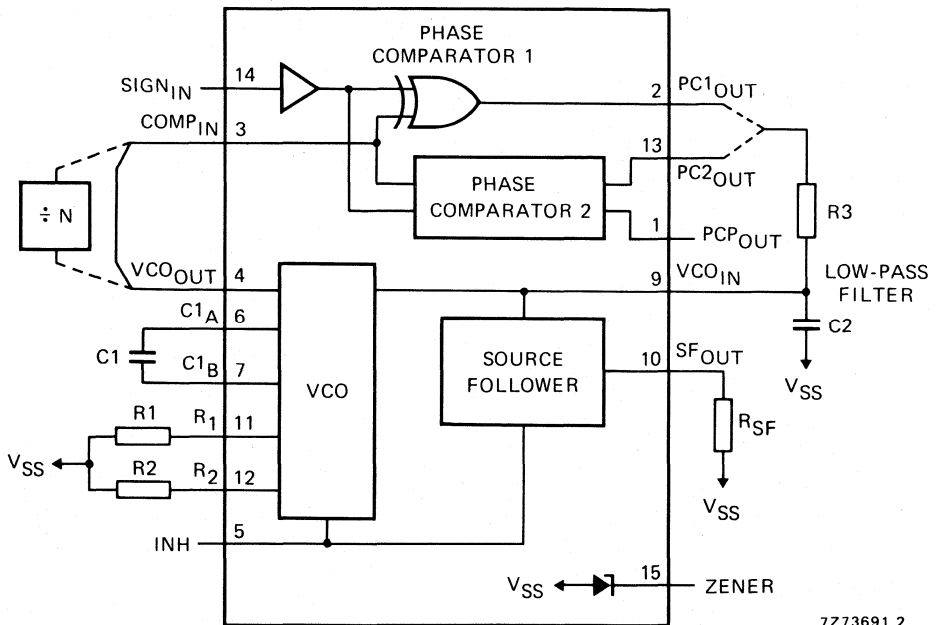
An example of application for the HEF4044B is:

- Four-bit storage with output enable

PHASE-LOCKED LOOP



The HEF4046B is a phase-locked loop circuit that consists of a linear voltage controlled oscillator (VCO) and two different phase comparators with a common signal input amplifier and a common comparator input. A 7 V regulator (zener) diode is provided for supply voltage regulation if necessary. For functional description see further on in this data.



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Fig. 1 Functional diagram.

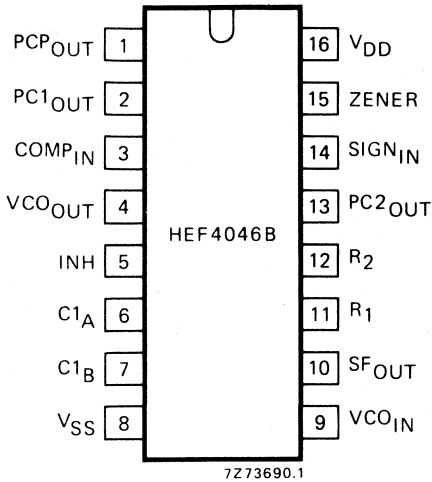
HEF4046BP: 16-lead DIL; plastic (SOT-38Z).

HEF4046BD: 16-lead DIL; ceramic (SOT-74).

HEF4046BT: 16-lead flat pack; plastic (SO-16; SOT-109A).

FAMILY DATA: see Family Specifications

I_{DD} LIMITS category MSI: see further on in this data.



PINNING

1. Phase comparator pulse output
2. Phase comparator 1 output
3. Comparator input
4. VCO output
5. Inhibit input
6. Capacitor C1 connection A
7. Capacitor C1 connection B
8. V_{SS}
9. VCO input
10. Source-follower output
11. Resistor R1 connection
12. Resistor R2 connection
13. Phase comparator 2 output
14. Signal input
15. Zener diode input for regulated supply.

Fig. 2 Pinning diagram.

FUNCTIONAL DESCRIPTION

VCO part

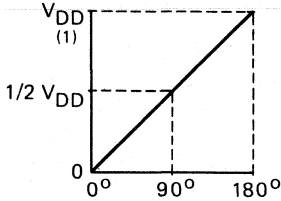
The VCO requires one external capacitor (C1) and one or two external resistors (R1 or R1 and R2). Resistor R1 and capacitor C1 determine the frequency range of the VCO. Resistor R2 enables the VCO to have a frequency off-set if required. The high input impedance of the VCO simplifies the design of low-pass filters; it permits the designer a wide choice of resistor/capacitor ranges. In order not to load the low-pass filter, a source-follower output of the VCO input voltage is provided at pin 10. If this pin (SF_{OUT}) is used, a load resistor (R_{SF}) should be connected from this pin to V_{SS}; if unused, this pin should be left open. The VCO output (pin 4) can either be connected directly to the comparator input (pin 3) or via a frequency divider. A LOW level at the inhibit input (pin 5) enables the VCO and the source follower, while a HIGH level turns off both to minimize stand-by power consumption.

Phase comparators

The phase-comparator signal input (pin 14) can be direct-coupled, provided the signal swing is between the standard HE4000B family input logic levels. The signal must be capacitively coupled to the self-biasing amplifier at the signal input in case of smaller swings. Phase comparator 1 is an EXCLUSIVE-OR network. The signal and comparator input frequencies must have a 50% duty factor to obtain the maximum lock range. The average output voltage of the phase comparator is equal to ½ V_{DD} when there is no signal or noise at the signal input. The average voltage to the VCO input is supplied by the low-pass filter connected to the output of phase comparator 1. This also causes the VCO to oscillate at the centre frequency (f₀). The frequency capture range (2 f_c) is defined as the frequency range of input signals on which the PLL will lock if it was initially out of lock. The frequency lock range (2 f_L) is defined as the frequency range of input signals on which the loop will stay locked if it was initially in lock. The capture range is smaller or equal to the lock range.

With phase comparator 1, the range of frequencies over which the PLL can acquire lock (capture range) depends on the low-pass filter characteristics and this range can be made as large as the lock range. Phase comparator 1 enables the PLL system to remain in lock in spite of high amounts of noise in the input signal. A typical behaviour of this type of phase comparator is that it may lock onto input

frequencies that are close to harmonics of the VCO centre frequency. Another typical behaviour is, that the phase angle between the signal and comparator input varies between 0° and 180° and is 90° at the centre frequency. Figure 3 shows the typical phase-to-output response characteristic.

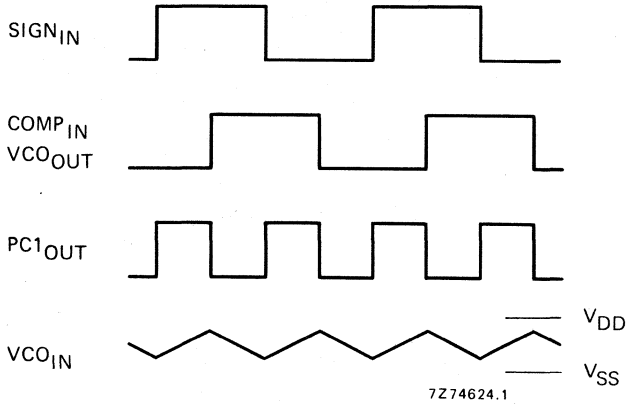


(1) Average output voltage.

Fig.3 Signal-to-comparator inputs phase difference for comparator 1.

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Figure 4 shows the typical waveforms for a PLL employing phase comparator 1 in locked condition of f_0 .



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Fig. 4 Typical waveforms for phase-locked loop employing phase comparator 1 in locked condition of f_0 .

FUNCTIONAL DESCRIPTION (continued)

Phase comparator 2 is an edge-controlled digital memory network. It consists of four flip-flops, control gating and a 3-state output circuit comprising p and n-type drivers having a common output node. When the p-type or n-type drivers are ON, they pull the output up to V_{DD} or down to V_{SS} respectively. This type of phase comparator only acts on the positive-going edges of the signals at $SIGN_{IN}$ and $COMP_{IN}$. Therefore, the duty factors of these signals are not of importance.

If the signal input frequency is higher than the comparator input frequency, the p-type output driver is maintained ON most of the time, and both the n and p-type drivers are OFF (3-state) the remainder of the time. If the signal input frequency is lower than the comparator input frequency, the n-type output driver is maintained ON most of the time, and both the n and p-type drivers are OFF the remainder of the time. If the signal input and comparator input frequencies are equal, but the signal input lags the comparator input in phase, the n-type output driver is maintained ON for a time corresponding to the phase difference. If the comparator input lags the signal input in phase, the p-type output driver is maintained ON for a time corresponding to the phase difference. Subsequently, the voltage at the capacitor of the low-pass filter connected to this phase comparator is adjusted until the signal and comparator inputs are equal in both phase and frequency. At this stable point, both p and n-type drivers remain OFF and thus the phase comparator output becomes an open circuit and keeps the voltage at the capacitor of the low-pass filter constant.

Moreover, the signal at the phase comparator pulse output (PCP_{OUT}) is a HIGH level which can be used for indicating a locked condition. Thus, for phase comparator 2 no phase difference exists between the signal and comparator inputs over the full VCO frequency range. Moreover, the power dissipation due to the low-pass filter is reduced when this type of phase comparator is used because both p and n-type output drivers are OFF for most of the signal input cycle. It should be noted that the PLL lock range for this type of phase comparator is equal to the capture range, independent of the low-pass filter. With no signal present at the signal input, the VCO is adjusted to its lowest frequency for phase comparator 2. Figure 5 shows typical waveforms for a PLL employing this type of phase comparator in locked condition.

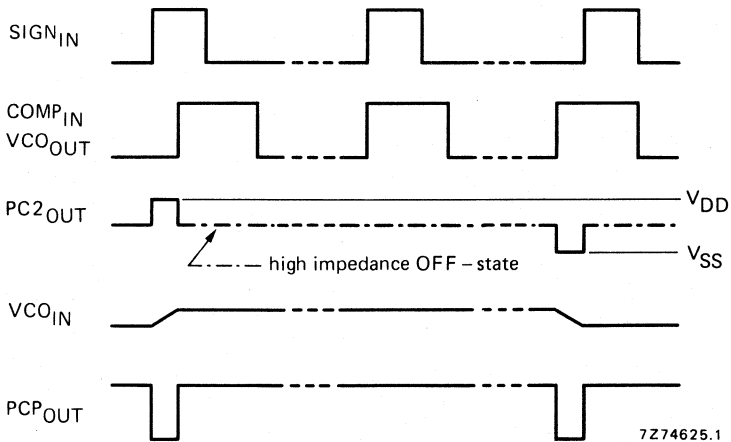
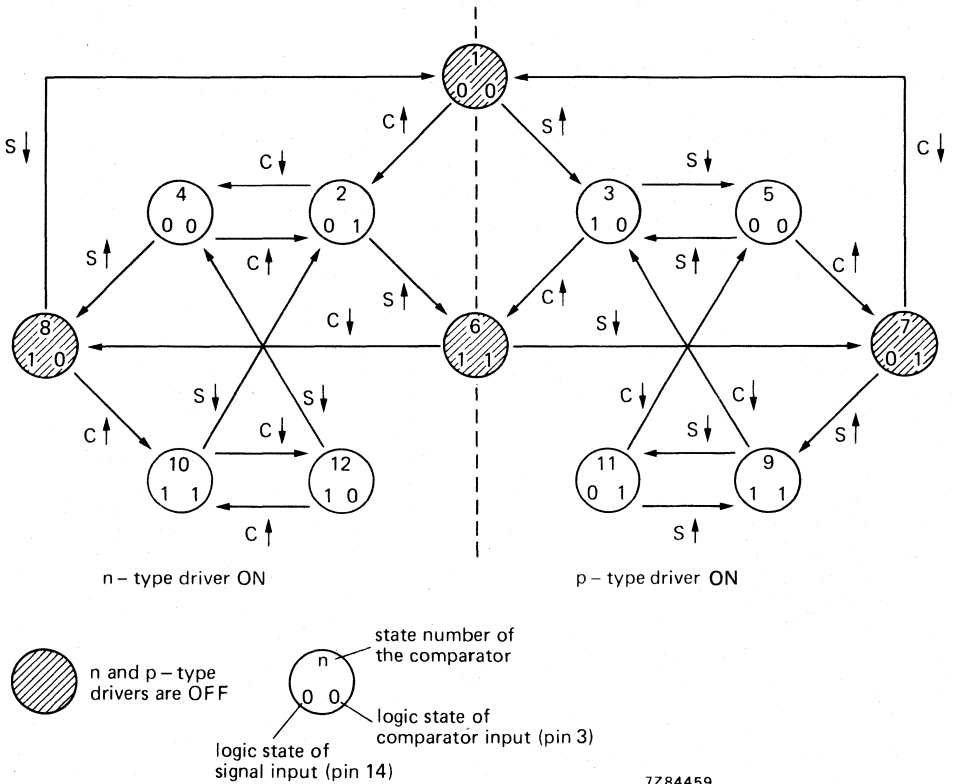


Fig. 5 Typical waveforms for phase-locked loop employing phase comparator 2 in locked condition.

Figure 6 shows the state diagram for phase comparator 2. Each circle represents a state of the comparator. The number at the top, inside each circle, represents the state of the comparator, while the logic state of the signal and comparator inputs are represented by a '0' for a logic LOW or a '1' for a logic HIGH, and they are shown in the left and right bottom of each circle.

The transitions from one to another result from either a logic change at the signal input (S) or the comparator input (C). A positive-going and a negative-going transition are shown by an arrow pointing up or down respectively.

The state diagram assumes that only one transition on either the signal input or comparator input occurs at any instant. States 3, 5, 9 and 11 represent the condition at the output when the p-type driver is ON, while states 2, 4, 10 and 12 determine the condition when the n-type driver is ON. States 1, 6, 7 and 8 represent the condition when the output is in its high impedance OFF state; i.e. both p and n-type drivers are OFF, and the PC_{OUT} output is HIGH. The condition at output PC_{OUT} for all other states is LOW.



S ↑: 0 to 1 transition at the signal input.
 C ↓: 1 to 0 transition at the comparator input.

Fig. 6 State diagram for comparator 2.

D.C. CHARACTERISTICS

V_{SS} = 0 V

	V _{DD} V	symbol	T _{amb} (°C)						
			-40		+25		+85		
			typ.	max.	typ.	max.	typ.	max.	
Supply current (note 1)	5	I _D	—	—	20	—	—	—	μA
	10		—	—	300	—	—	—	μA
	15		—	—	750	—	—	—	μA
Quiescent device current (note 2)	5	I _{DD}	—	20	—	20	—	150	μA
	10		—	40	—	40	—	300	μA
	15		—	80	—	80	—	600	μA

Notes

- Pin 15 open; pin 5 at V_{DD}; pins 3 and 9 at V_{SS}; pin 14 open.
- Pin 15 open; pin 5 at V_{DD}; pins 3 and 9 at V_{SS}; pin 14 at V_{DD}; input current pin 14 not included.

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V _{DD} V	symbol	min.	typ.	max.		
Phase comparators							
Operating supply voltage		V _{DD}	3		15 V		
Input resistance at SIGN _{IN}	5	R _{IN}		750	kΩ	} at self-bias operating point	
	10			220	kΩ		
	15			140	kΩ		
A.C. coupled input sensitivity at SIGN _{IN}	5	V _{IN}		150	mV	} peak-to-peak values; R1 = 10 kΩ; R2 = ∞; C1 = 100 pF; independent of the lock range	
	10			150	mV		
	15			200	mV		
D.C. coupled input sensitivity at SIGN _{IN} ; COMP _{IN}	5	V _{IL}			1,5 V	} full temperature range	
	10				3,0 V		
	15				4,0 V		
	5		V _{IH}	3,5			V
	10			7,0			V
	15			11,0			V
Input current at SIGN _{IN}	5	+ I _{IN}		7	μA	} SIGN _{IN} at V _{DD}	
	10			30	μA		
	15			70	μA		
	5	- I _{IN}		3	μA	} SIGN _{IN} at V _{SS}	
	10			18	μA		
	15			45	μA		

A.C. CHARACTERISTICS $V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	symbol	min.	typ.	max.	
VCO						
Operating supply voltage		V_{DD}	3 5		15 V 15 V	as fixed oscillator only phase-locked loop operation
Power dissipation	5 10 15	P		150 2500 9000	μW μW μW	$f_0 = 10\text{ kHz}$; $R_1 = 1\text{ M}\Omega$; $R_2 = \infty$; V_{COIN} at $\frac{1}{2} V_{DD}$; see also Figs 10 and 11
Maximum operating frequency	5 10 15	f_{max}	0,5 1,0 1,3	1,0 2,0 2,7	MHz MHz MHz	V_{COIN} at V_{DD} ; $R_1 = 10\text{ k}\Omega$; $R_2 = \infty$; $C_1 = 50\text{ pF}$
Temperature/frequency stability	5 10 15			0,22–0,30 0,04–0,05 0,01–0,05	%/°C %/°C %/°C	no frequency offset ($f_{min} = 0$); see also note 1
	5 10 15			0–0,22 0–0,04 0–0,01	%/°C %/°C %/°C	with frequency offset ($f_{min} > 0$); see also note 1
Linearity	5 10 15			0,50 0,25 0,25	% % %	$R_1 > 10\text{ k}\Omega$ } see Fig. 13 $R_1 > 400\text{ k}\Omega$ } and Figs 14 $R_1 = 1\text{ M}\Omega$ } 15 and 16
Duty factor at V_{COOUT}	5 10 15	δ		50 50 50	% % %	
Input resistance at V_{COIN}	5 10 15	R_{IN}		10^6 10^6 10^6	$\text{M}\Omega$ $\text{M}\Omega$ $\text{M}\Omega$	
Source follower						
Offset voltage V_{COIN} minus SF_{OUT}	5 10 15			1,7 2,0 2,1	V V V	$R_{SF} = 10\text{ k}\Omega$; V_{COIN} at $\frac{1}{2} V_{DD}$
	5 10 15			1,5 1,7 1,8	V V V	$R_{SF} = 50\text{ k}\Omega$; V_{COIN} at $\frac{1}{2} V_{DD}$
Linearity	5 10 15			0,3 1,0 1,3	% % %	$R_{SF} > 50\text{ k}\Omega$; see Fig. 13
Zener diode						
Zener voltage		V_Z		7,3	V	$I_Z = 50\text{ }\mu\text{A}$
Dynamic resistance		R_Z		25	Ω	$I_Z = 1\text{ mA}$

Notes

1. Over the recommended component range.

DESIGN INFORMATION

characteristic	using phase comparator 1	using phase comparator 2
No signal on $SIGN_{IN}$	VCO in PLL system adjusts to centre frequency (f_o)	VCO in PLL system adjusts to min. frequency (f_{min})
Phase angle between $SIGN_{IN}$ and $COMP_{IN}$	90° at centre frequency (f_o), approaching 0° and 180° at ends of lock range ($2 f_L$)	always 0° in lock (positive-going edges)
Locks on harmonics of centre frequency	yes	no
Signal input noise rejection	high	low
Lock frequency range ($2 f_L$)	the frequency range of the input signal on which the loop will stay locked if it was initially in lock; $2 f_L = \text{full VCO frequency range} = f_{max} - f_{min}$	
Capture frequency range ($2 f_C$)	the frequency range of the input signal on which the loop will lock if it was initially out of lock depends on low-pass filter characteristics; $f_C < f_L$ $f_C = f_L$	
Centre frequency (f_o)	the frequency of the VCO when VCO_{IN} at $\frac{1}{2}V_{DD}$	

VCO component selection

Recommended range for R1 and R2: 10 k Ω to 1 M Ω ; for C1: 50 pF to any practical value.

1. VCO without frequency offset ($R2 = \infty$).

- Given f_o : use f_o with Fig. 7 to determine R1 and C1.
- Given f_{max} : calculate f_o from $f_o = \frac{1}{2} f_{max}$; use f_o with Fig. 7 to determine R1 and C1.

2. VCO with frequency offset.

- Given f_o and f_L : calculate f_{min} from the equation $f_{min} = f_o - f_L$; use f_{min} with Fig. 8 to determine R2 and C1; calculate

$$\frac{f_{max}}{f_{min}} \text{ from the equation } \frac{f_{max}}{f_{min}} = \frac{f_o + f_L}{f_o - f_L}; \text{ use } \frac{f_{max}}{f_{min}} \text{ with Fig. 9 to determine the ratio } R2/R1 \text{ to}$$

obtain R1.

- Given f_{min} and f_{max} : use f_{min} with Fig. 8 to determine R2 and C1; calculate $\frac{f_{max}}{f_{min}}$; use $\frac{f_{max}}{f_{min}}$

with Fig. 9 to determine R2/R1 to obtain R1.

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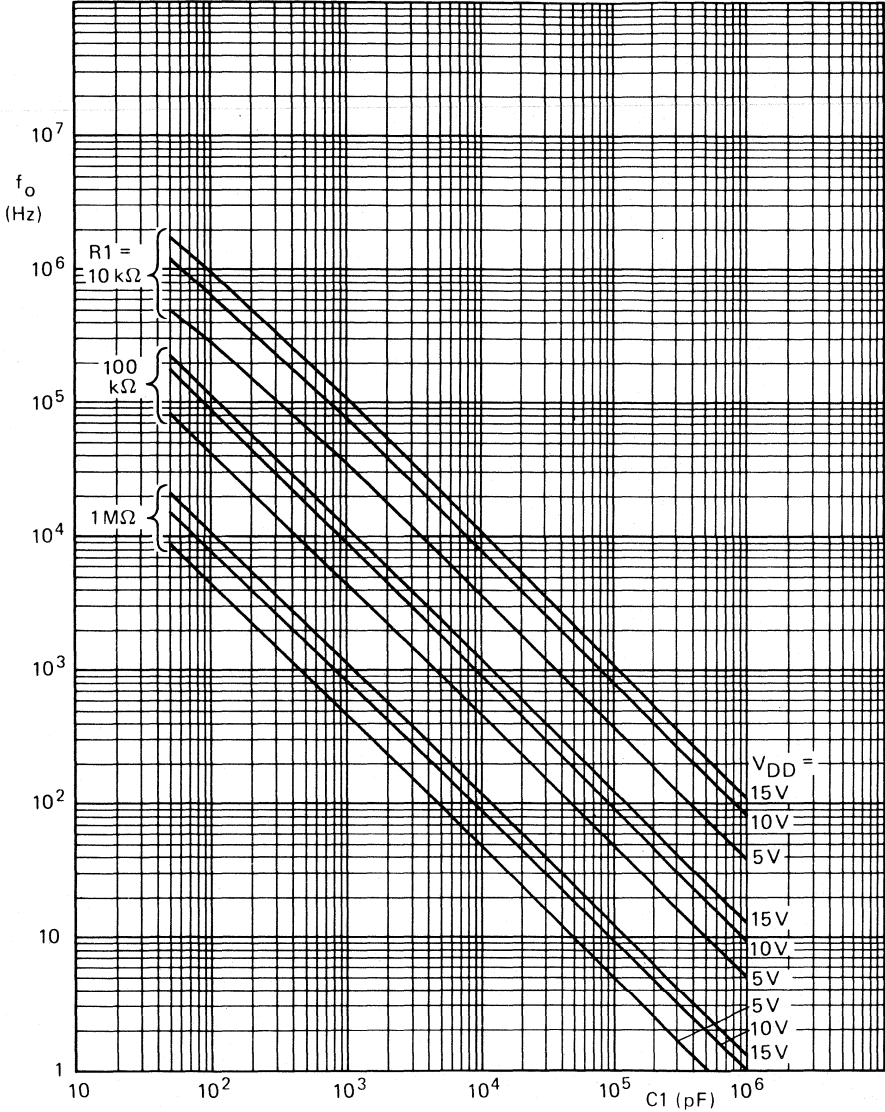


Fig. 7 Typical centre frequency as a function of capacitor C_1 ; $T_{amb} = 25\text{ }^\circ\text{C}$; V_{COIN} at $\frac{1}{2} V_{DD}$; INH at V_{SS} ; $R_2 = \infty$.

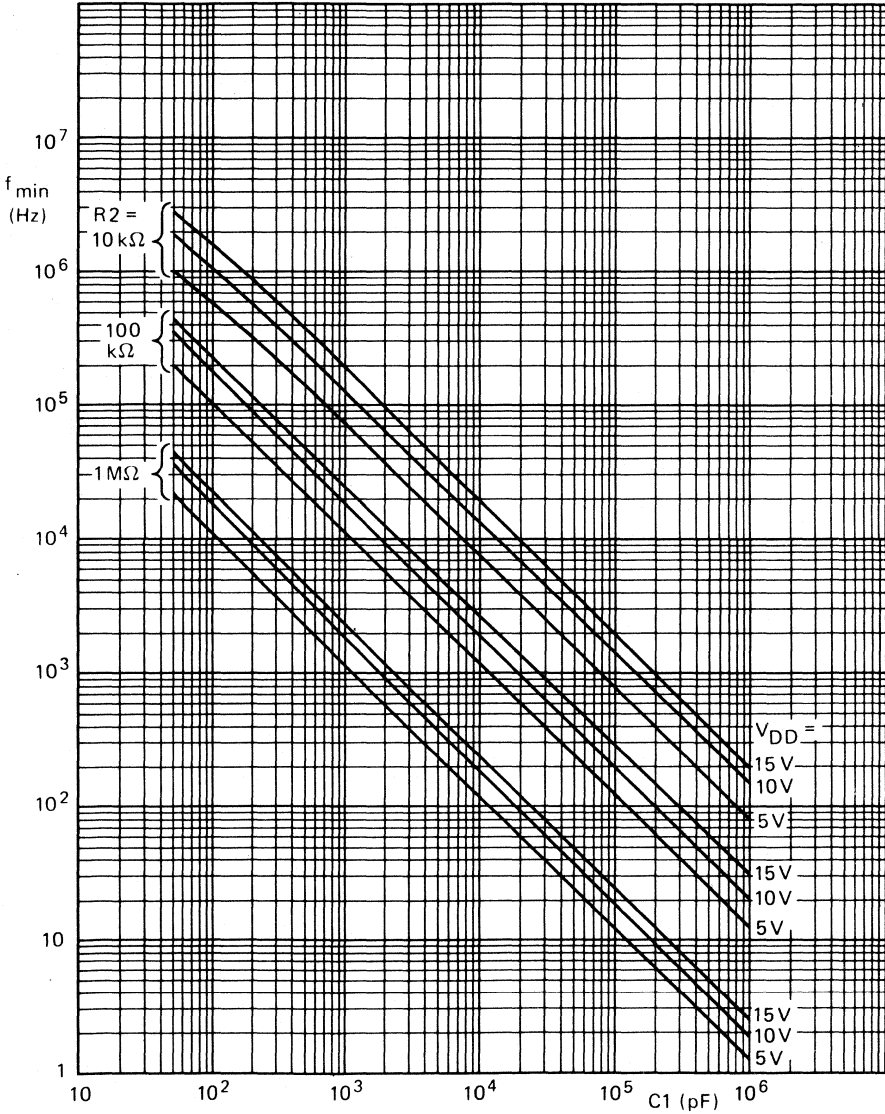


Fig. 8 Typical frequency offset as a function of capacitor C_1 ; $T_{amb} = 25\text{ }^\circ\text{C}$; V_{COIN} at V_{SS} ; I_{NH} at V_{SS} ; $R_1 = \infty$.

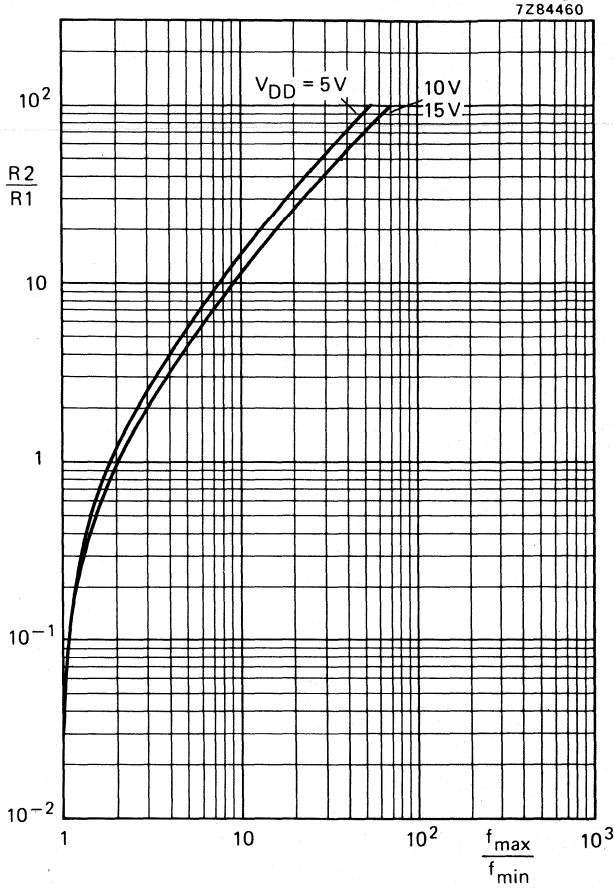


Fig. 9 Typical ratio of R2/R1 as a function of the ratio f_{max}/f_{min} .

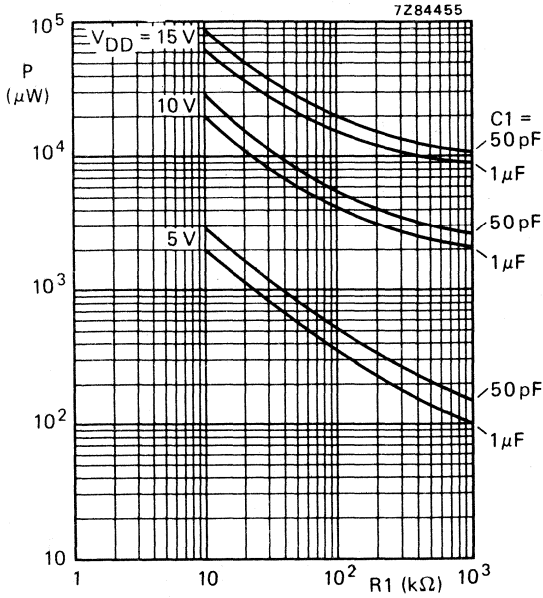


Fig. 10 Power dissipation as a function of R_1 ; $R_2 = \infty$; V_{CO1IN} at $\frac{1}{2} V_{DD}$; $C_L = 50 pF$.

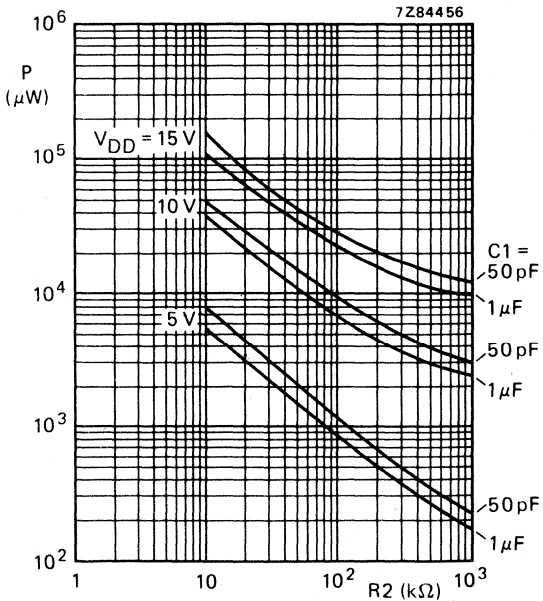


Fig. 11 Power dissipation as a function of R_2 ; $R_1 = \infty$; V_{CO1IN} at V_{SS} (0 V); $C_L = 50 pF$.

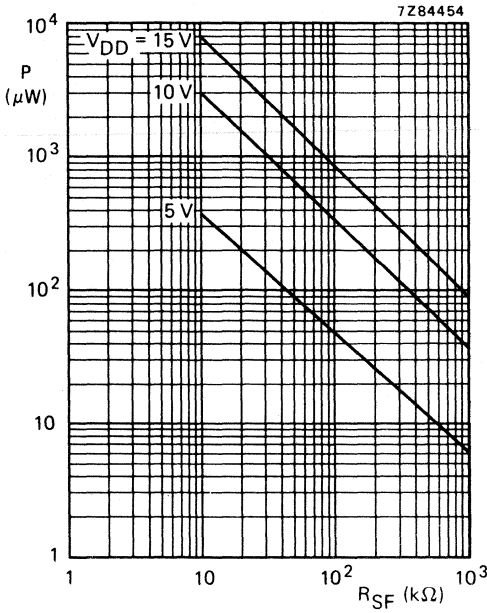


Fig. 12 Power dissipation of source follower as a function of R_{SF} ; V_{COIN} at $\frac{1}{2} V_{DD}$; $R_1 = \infty$; $R_2 = \infty$.

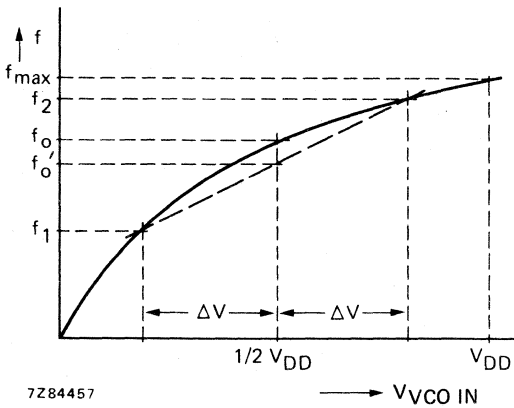


Fig. 13 Definition of linearity (see a.c. characteristics).

For VCO linearity:

$$f'_o = \frac{f_1 + f_2}{2}$$

$$\text{lin.} = \frac{f'_o - f_o}{f'_o} \times 100\%$$

Figure 13 and the above formula also apply to source follower linearity: substitute $V_{SF OUT}$ for f .

$\Delta V = 0,3 \text{ V}$ at $V_{DD} = 5 \text{ V}$

$\Delta V = 2,5 \text{ V}$ at $V_{DD} = 10 \text{ V}$

$\Delta V = 5 \text{ V}$ at $V_{DD} = 15 \text{ V}$

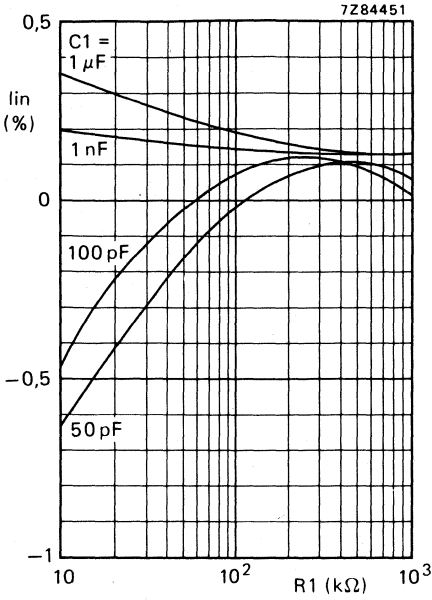


Fig. 14 VCO frequency linearity as a function of R1; R2 = ∞ ; V_{DD} = 5 V.

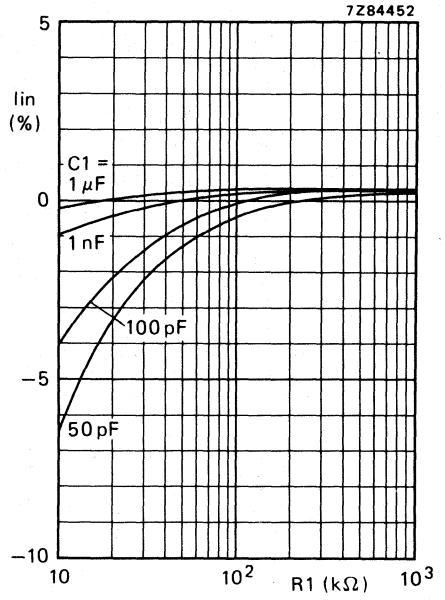


Fig. 15 VCO frequency linearity as a function of R1; R2 = ∞ ; V_{DD} = 10 V.

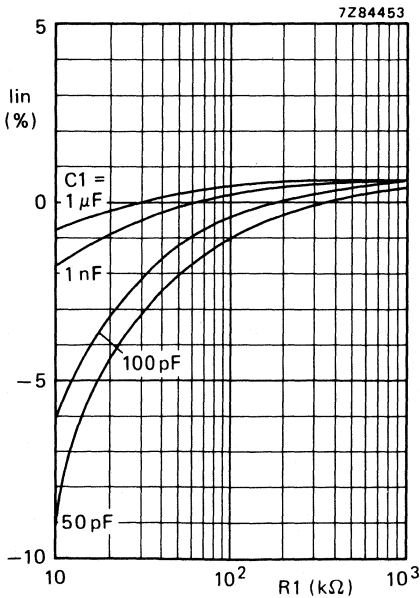


Fig. 16 VCO frequency linearity as a function of R1; R2 = ∞ ; V_{DD} = 15 V.

MONOSTABLE/ASTABLE MULTIVIBRATOR



The HEF4047B consists of a gatable astable multivibrator with logic techniques incorporated to permit positive or negative edge-triggered monostable multivibrator action with retriggering and external counting options.

Inputs include + TRIGGER, - TRIGGER, ASTABLE, $\overline{\text{ASTABLE}}$, RETRIGGER and MR (Master Reset). Buffered outputs are O, $\overline{\text{O}}$ and OSCILLATOR OUTPUT. In all modes of operation an external capacitor (C_t) must be connected between C_{TC} and R_{TC} , and an external resistor (R_t) must be connected between R_{TC} and R_{CTC} (continued on next page).

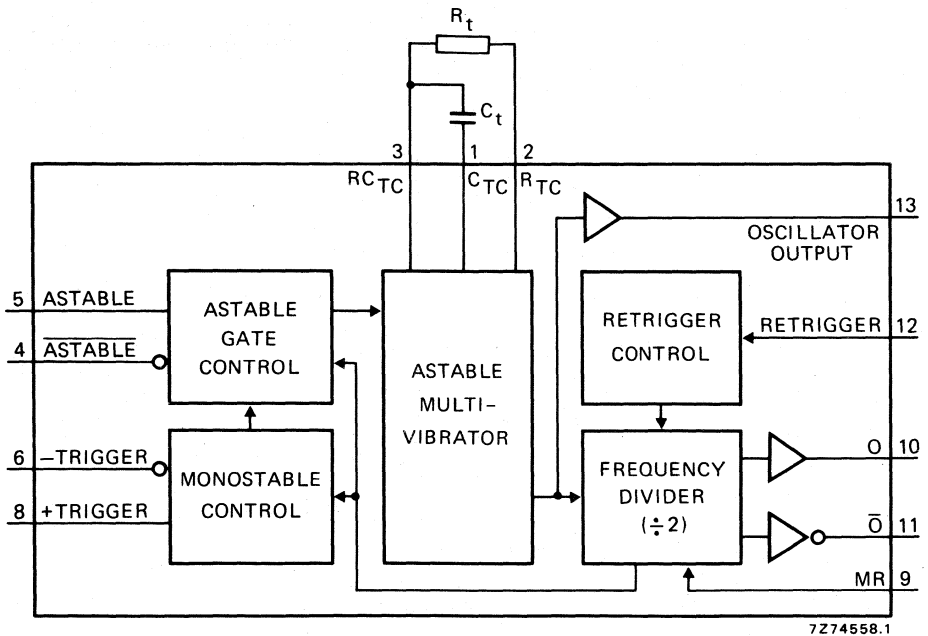


Fig. 1 Functional diagram.

FAMILY DATA

I_{DD} LIMITS category MSI

} see Family Specifications

HEF4047B

MSI

Astable operation is enabled by a HIGH level on the $\overline{\text{ASTABLE}}$ input. The period of the square wave at O and $\overline{\text{O}}$ outputs is a function of the external components employed. 'True' input pulses on the $\overline{\text{ASTABLE}}$ or 'complement' pulses on the ASTABLE input, allow the circuit to be used as a gated multivibrator. The OSCILLATOR OUTPUT period will be half of the O output in the astable mode. However, a 50% duty factor is not guaranteed at this output.

In the monostable mode, positive edge-triggering is accomplished by applying a leading-edge pulse to the + TRIGGER input and a LOW level to the - TRIGGER input. For negative edge-triggering, a trailing-edge pulse is applied to the - TRIGGER and a HIGH level to the + TRIGGER. Input pulses may be of any duration relative to the output pulse. The multivibrator can be retriggered (on the leading-edge only) by applying a common pulse to both the RETRIGGER and + TRIGGER inputs. In this mode the output pulse remains HIGH as long as the input pulse period is shorter than the period determined by the RC components.

An external count down option can be implemented by coupling O to an external 'N' counter and resetting the counter with the trigger pulse. The counter output pulse is fed back to the $\overline{\text{ASTABLE}}$ input and has a duration equal to N times the period of the multivibrator. A HIGH level on the MR input assures no output pulse during an ON-power condition. This input can also be activated to terminate the output pulse at any time. In the monostable mode, a HIGH level or power-ON reset pulse must be applied to MR, whenever V_{DD} is applied.

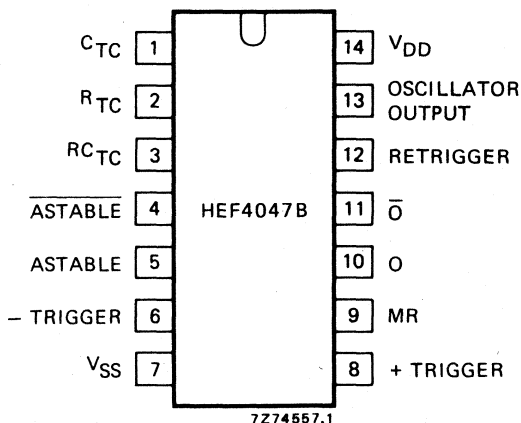
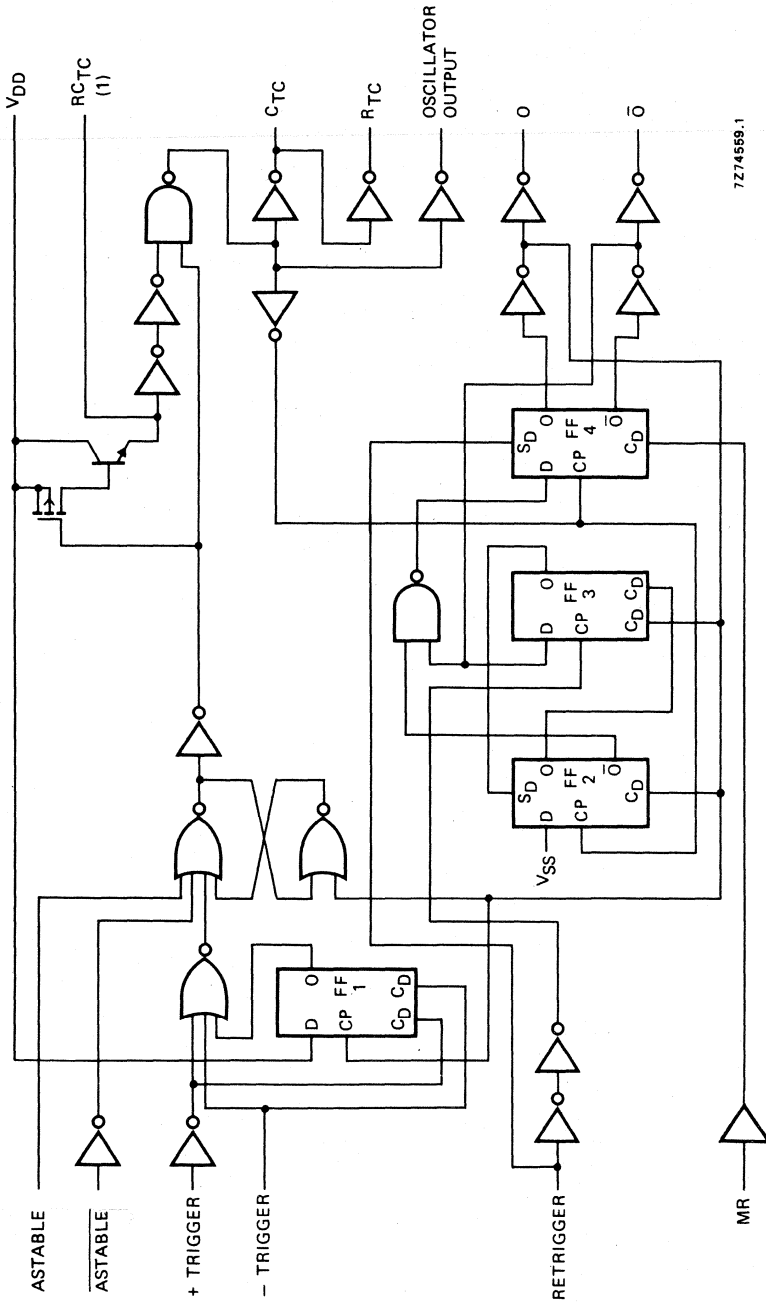


Fig. 2 Pinning diagram.

HEF4047BP : 14-lead DIL; plastic (SOT-27S, T, V)

HEF4047BD : 14-lead DIL; ceramic (SOT-73).

HEF4047BT : 14-lead flat pack; plastic (SO-14; SOT-108A).



7274569.1

(1) Special input protection that allows operating input voltages outside the supply voltage lines. Compared to the standard input protection pin 3 is more sensitive to static discharge; extra handling precautions are recommended.

Fig. 3 Logic diagram.

FUNCTIONAL CONNECTIONS

function	pins connected to			output pulse from pins	output period or pulse width
	V _{DD}	V _{SS}	input pulse		
astable multivibrator					
free running	4, 5, 6, 14	7, 8, 9, 12	—	10, 11, 13	at pins 10, 11: $t_A = 4,40 R_T C_T$ at pin 13: $t_A = 2,20 R_T C_T$
true gating	4, 6, 14	7, 8, 9, 12	5	10, 11, 13	
complement gating	6, 14	5, 7, 8, 9, 12	4	10, 11, 13	
monostable multivibrator					
pos. edge-triggering	4, 14	5, 6, 7, 9, 12	8	10, 11	at pins 10, 11: $t_M = 2,48 R_T C_T$
neg. edge-triggering	4, 8, 14	5, 7, 9, 12	6	10, 11	
retriggerable	4, 14	5, 6, 7, 9	8, 12	10, 11	
external count down*	14	5, 6, 7, 8, 9, 12	—	10, 11	

* Input pulse to RESET of external counting chip; external counting chip output to pin 4.

Note

In all cases, external resistor between pins 2 and 3, external capacitor between pins 1 and 3.

D.C. CHARACTERISTICS

V_{SS} = 0 V; inputs at V_{SS} or V_{DD}

	V _{DD} V	symbol	T _{amb} (°C)				
			—40 max.	+25 min.	+85 max.	+85 max.	
Leakage current pin 3; output transistor OFF	15	I ₃	0,3	—	0,3	1 μA	pin 3 at V _{DD} or V _{SS}

A.C. CHARACTERISTICS

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^\circ\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	symbol	min. typ. max.	typical extrapolation formula
Propagation delays				
<u>ASTABLE, ASTABLE</u>				
→ OSC. OUTPUT	5		95 190	$68\text{ ns} + (0,55\text{ ns/pF}) C_L$
HIGH to LOW	10	t_{PHL}	45 90	$43\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15		30 60	$22\text{ ns} + (0,16\text{ ns/pF}) C_L$
LOW to HIGH	5		85 170	$58\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10	t_{PLH}	40 80	$29\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15		30 60	$22\text{ ns} + (0,16\text{ ns/pF}) C_L$
<u>ASTABLE, $\bar{\text{ASTABLE}}$</u>				
→ O, $\bar{\text{O}}$	5		150 300	$123\text{ ns} + (0,55\text{ ns/pF}) C_L$
HIGH to LOW	10	t_{PHL}	65 130	$54\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15		50 100	$42\text{ ns} + (0,16\text{ ns/pF}) C_L$
LOW to HIGH	5		130 260	$103\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10	t_{PLH}	60 120	$49\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15		45 90	$37\text{ ns} + (0,16\text{ ns/pF}) C_L$
<u>+/- TRIGGER</u>				
→ O, $\bar{\text{O}}$	5		160 320	$133\text{ ns} + (0,55\text{ ns/pF}) C_L$
HIGH to LOW	10	t_{PHL}	65 130	$54\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15		50 100	$42\text{ ns} + (0,16\text{ ns/pF}) C_L$
LOW to HIGH	5		155 310	$128\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10	t_{PLH}	65 130	$54\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15		50 100	$42\text{ ns} + (0,16\text{ ns/pF}) C_L$
<u>+ TRIGGER, RETRIGGER → $\bar{\text{O}}$</u>				
HIGH to LOW	5		65 130	$38\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10	t_{PHL}	30 60	$19\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15		25 50	$17\text{ ns} + (0,16\text{ ns/pF}) C_L$
<u>+ TRIGGER, RETRIGGER → O</u>				
LOW to HIGH	5		95 190	$68\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10	t_{PLH}	40 80	$29\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15		30 60	$22\text{ ns} + (0,16\text{ ns/pF}) C_L$
<u>MR → O</u>				
HIGH to LOW	5		100 200	$83\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10	t_{PHL}	45 90	$34\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15		35 70	$27\text{ ns} + (0,16\text{ ns/pF}) C_L$
<u>MR → $\bar{\text{O}}$</u>				
LOW to HIGH	5		100 200	$83\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10	t_{PLH}	45 90	$34\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15		35 70	$27\text{ ns} + (0,16\text{ ns/pF}) C_L$

A.C. CHARACTERISTICS (continued)
 $V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	symbol	min.	typ.	max.	typical extrapolation formula	
Output transition times HIGH to LOW	5	t_{THL}		60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$
	10		30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$	
	15		20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$	
LOW to HIGH	5	t_{TLH}		60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$
	10		30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$	
	15		20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$	
Minimum MR pulse width; HIGH	5	t_{WMRH}	60	30		ns	
	10		30	15		ns	
	15		20	10		ns	
Minimum input pulse width; any input except MR	5	t_W	220	110		ns	
	10		100	50		ns	
	15		70	35		ns	

APPLICATION INFORMATION**General features:**

- Monostable (one-shot) or astable (free-running) operation
- True and complemented buffered outputs
- Only one external R and C required

Monostable multivibrator features:

- Positive- or negative-edge triggering
- Output pulse width independent of trigger pulse duration
- Retriggerable option for pulse-width expansion
- Long pulse width possible using small RC components by means of external counter provision
- Fast recovery time essentially independent of pulse width
- Pulse-width accuracy maintained at duty cycles approaching 100%

Astable multivibrator features:

- Free-running or gatable operating modes
- 50% duty cycle
- Oscillator output available

1. Astable mode design information

a. Unit-to-unit transfer-voltage variations

The following analysis presents worst-case variations from unit-to-unit as a function of transfer-voltage (V_{TR}) shift for free running (astable) operation.

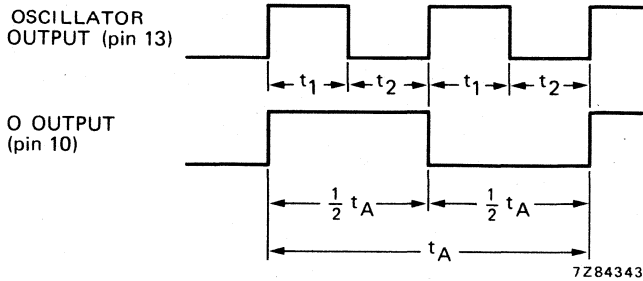


Fig. 4 Astable mode waveforms.

$$t_1 = -R_t C_t \ln \frac{V_{TR}}{V_{DD} + V_{TR}}$$

$$t_2 = -R_t C_t \ln \frac{V_{DD} - V_{TR}}{2V_{DD} - V_{TR}}$$

$$t_A = 2(t_1 + t_2) = -2R_t C_t \ln \frac{(V_{TR})(V_{DD} - V_{TR})}{(V_{DD} + V_{TR})(2V_{DD} - V_{TR})}, \text{ where } t_A = \text{Astable mode pulse width.}$$

Values for t_A are:

	typ. : $V_{TR} = 0,5 V_{DD}$; $t_A = 4,40 R_t C_t$
$V_{DD} = 5 \text{ or } 10 \text{ V}$	{ min. : $V_{TR} = 0,3 V_{DD}$; $t_A = 4,71 R_t C_t$ max. : $V_{TR} = 0,7 V_{DD}$; $t_A = 4,71 R_t C_t$
$V_{DD} = 15 \text{ V}$	{ min. : $V_{TR} = 4 \text{ V}$; $t_A = 4,84 R_t C_t$ max. : $V_{TR} = 11 \text{ V}$; $t_A = 4,84 R_t C_t$

thus if $t_A = 4,40 R_t C_t$ is used, the maximum variation will be (+ 70%; -0,0%) at 10 V.

APPLICATION INFORMATION (continued)

b. Variations due to changes in V_{DD}

In addition to variations from unit-to-unit, the astable period may vary as a function of frequency with respect to V_{DD} .

Typical variations are presented graphically in Figs 5 and 6 with 10 V as a reference.

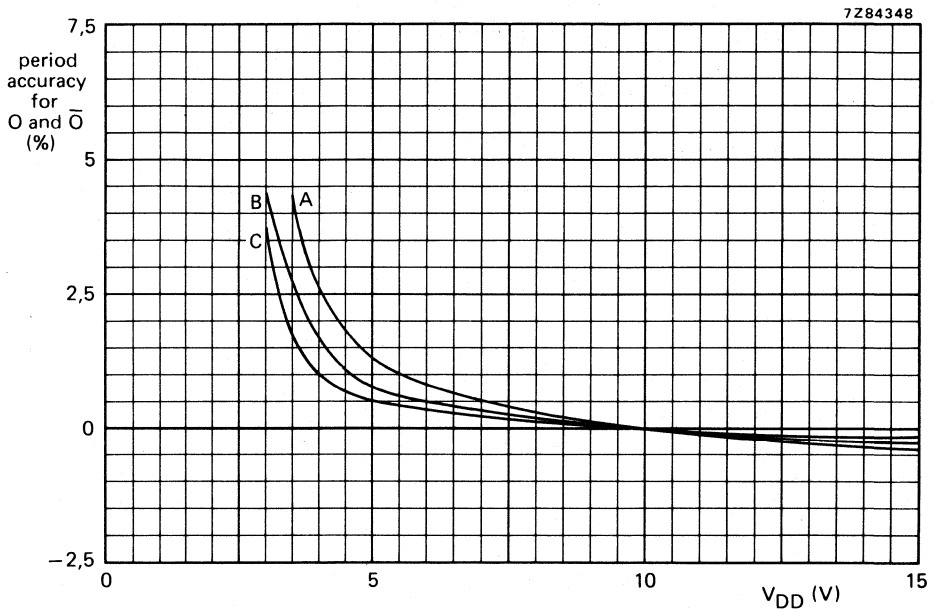


Fig. 5 Typical O and \bar{O} period accuracy as a function of supply voltage; astable mode; $T_{amb} = 25^{\circ}\text{C}$.

curve	f_o kHz	C_t pF	R_t k Ω
A	10	100	220
B	5	100	470
C	1	1000	220

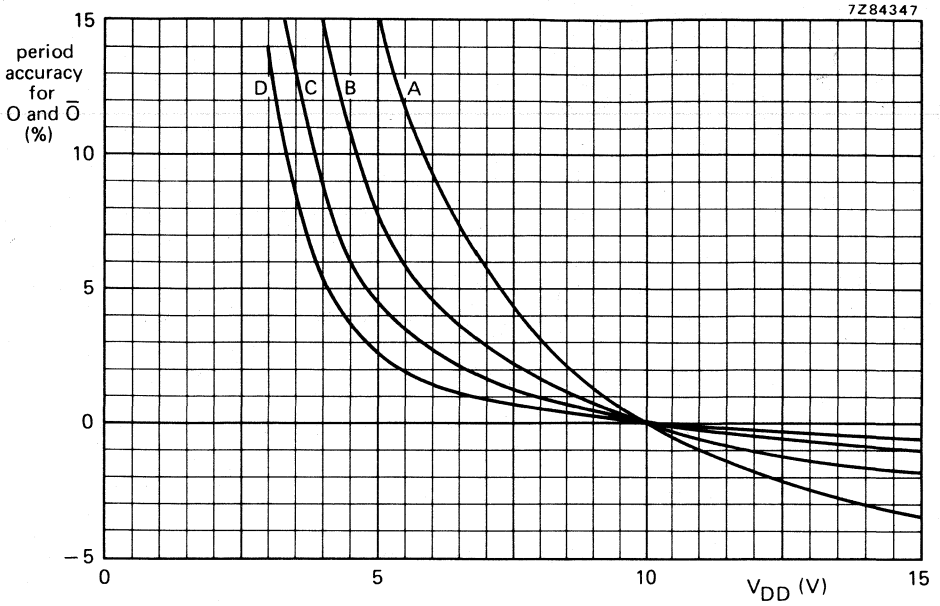


Fig. 6 Typical O and \bar{O} period accuracy as a function of supply voltage; astable mode; $T_{amb} = 25\text{ }^{\circ}\text{C}$.

curve	f_o kHz	C_t pF	R_t k Ω
A	500	10	47
B	225	100	10
C	100	100	22
D	50	100	47

APPLICATION INFORMATION (continued)

2. Monostable mode design information

The following analysis presents worst case variations from unit-to-unit as a function of transfer-voltage (V_{TR}) shift for one-shot (monostable) operation.

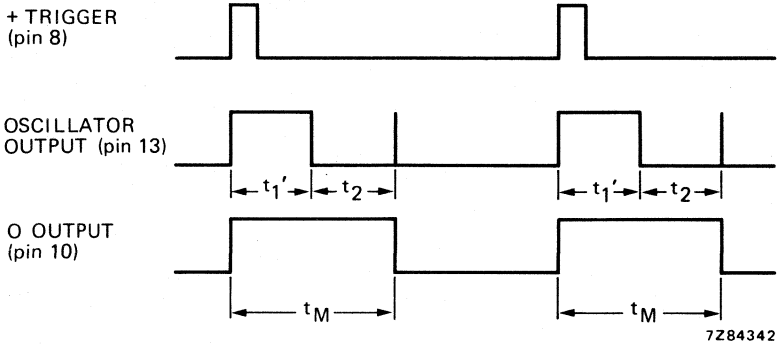


Fig. 7 Monostable waveforms.

$$t_1' = -R_t C_t \ln \frac{V_{TR}}{2V_{DD}}$$

$$t_M = (t_1' + t_2)$$

$$t_M = -R_t C_t \ln \frac{(V_{TR})(V_{DD} - V_{TR})}{(2V_{DD} - V_{TR})(2V_{DD})}, \text{ where } t_M = \text{Monostable mode pulse width.}$$

Values for t_M are:

	typ. : $V_{TR} = 0,5 V_{DD}$; $t_M = 2,48 R_t C_t$
$V_{DD} = 5 \text{ to } 10 \text{ V}$	{ min. : $V_{TR} = 0,3 V_{DD}$; $t_M = 2,78 R_t C_t$
	{ max. : $V_{TR} = 0,7 V_{DD}$; $t_M = 2,52 R_t C_t$
$V_{DD} = 15 \text{ V}$	{ min. : $V_{TR} = 4 \text{ V}$; $t_M = 2,88 R_t C_t$
	{ max. : $V_{TR} = 11 \text{ V}$; $t_M = 2,56 R_t C_t$

thus if $t_M = 2,48 R_t C_t$ is used, the maximum variation will be (+ 12%; -0,0%) at 10 V.

Note

In the astable mode, the first positive half cycle has a duration of t_M ; succeeding durations are $\frac{1}{2} t_A$.

3. Retrigger mode operation

The HEF4047B can be used in the retrigger mode to extend the output pulse duration, or to compare the frequency of an input signal with that of the internal oscillator. In the retrigger mode the input pulse is applied to pins 8 and 12, and the output is taken from pin 10 or 11. Normal monostable action is obtained when one retrigger pulse is applied (Fig. 8).

Extended pulse duration is obtained when more than one pulse is applied. For two input pulses, $t_{RE} = t_1' + t_1 + 2t_2$.

For more than two pulses, t_{RE} (output O), terminates at some variable time, t_D , after the termination of the last retrigger pulse; t_D is variable because t_{RE} (output O) terminates after the second positive edge of the oscillator output appears at flip-flop 4.

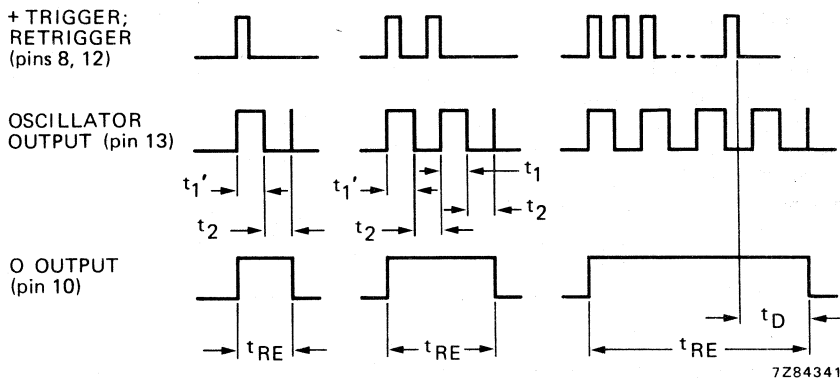


Fig. 8 Retrigger mode waveforms.

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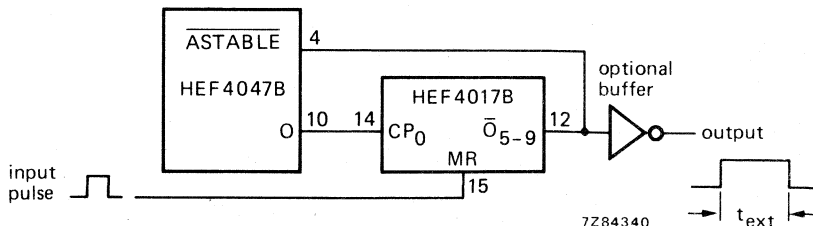
4. External counter option

Time t_M can be extended by any amount with the use of external counting circuitry. Advantages include digitally controlled pulse duration, small timing capacitors for long time periods, and extremely fast recovery time. A typical implementation is shown in Fig. 9.

The pulse duration at the output is:

$$t_{ext} = (N - 1)(t_A) + (t_M + \frac{1}{2} t_A)$$

Where t_{ext} = pulse duration of the circuitry, and N is the number of counts used.



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Fig. 9 Implementation of external counter option.

APPLICATION INFORMATION (continued)**5. Timing component limitations**

The capacitor used in the circuit should be non-polarized and have low leakage (i.e. the parallel resistance of the capacitor should be an order of magnitude greater than the external resistor used).

There is no upper or lower limit for either R_t or C_t value to maintain oscillation.

However, in consideration of accuracy, C_t must be much larger than the inherent stray capacitance in the system (unless this capacitance can be measured and taken into account).

R_t must be much larger than the LOC MOS 'ON' resistance in series with it, which typically is hundreds of ohms.

The recommended values for R_t and C_t to maintain agreement with previously calculated formulae without trimming should be:

$$C_t \geq 100 \text{ pF, up to any practical value,}$$

$$10 \text{ k}\Omega \leq R_t \leq 1 \text{ M}\Omega.$$

6. Power consumption

In the standby mode (monostable or astable), power dissipation will be a function of leakage current in the circuit.

For dynamic operation, the power needed to charge the external timing capacitor C_t is given by the following formulae:

Astable mode: $P = 2 C_t V^2 f$ (f at output pin 13)

$$P = 4 C_t V^2 f \text{ (f at output pins 10 and 11)}$$

Monostable mode: $P = \frac{(2,9 C_t V^2)(\text{duty cycle})}{T}$ (f at output pins 10 and 11)

Because the power dissipation does not depend on R_t , a design for minimum power dissipation would be a small value of C_t . The value of R would depend on the desired period (within the limitations discussed previously).

Typical power consumption in astable mode is shown in Figs 10, 11 and 12.

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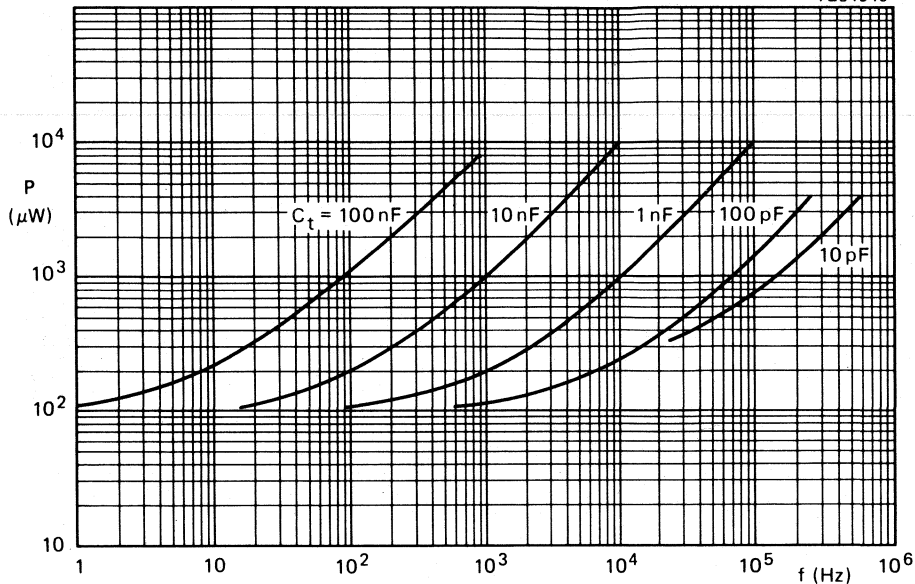


Fig. 10 Power consumption as a function of the output frequency at 0 or $\bar{0}$; $V_{DD} = 5V$; astable mode.

7Z84345

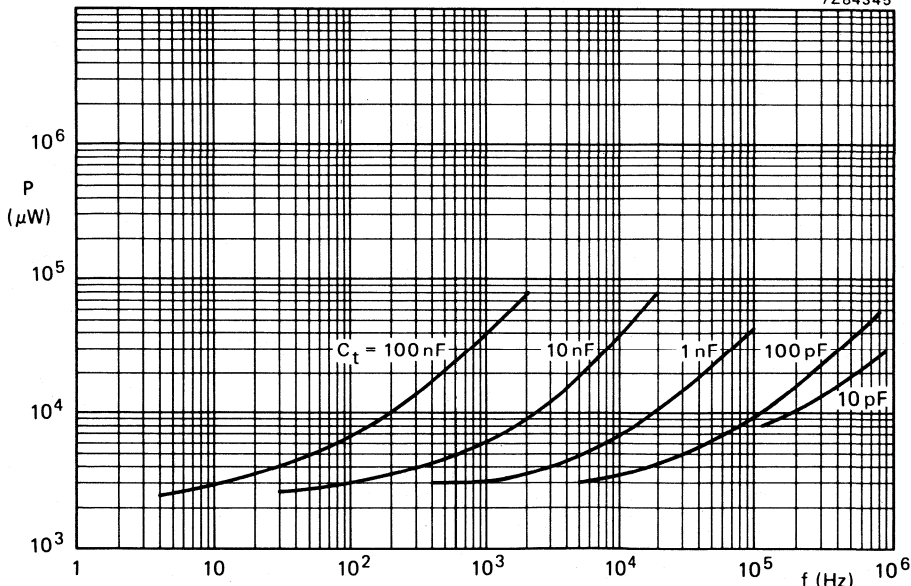


Fig. 11 Power consumption as a function of the output frequency at 0 or $\bar{0}$; $V_{DD} = 10V$; astable mode.

APPLICATION INFORMATION (continued)

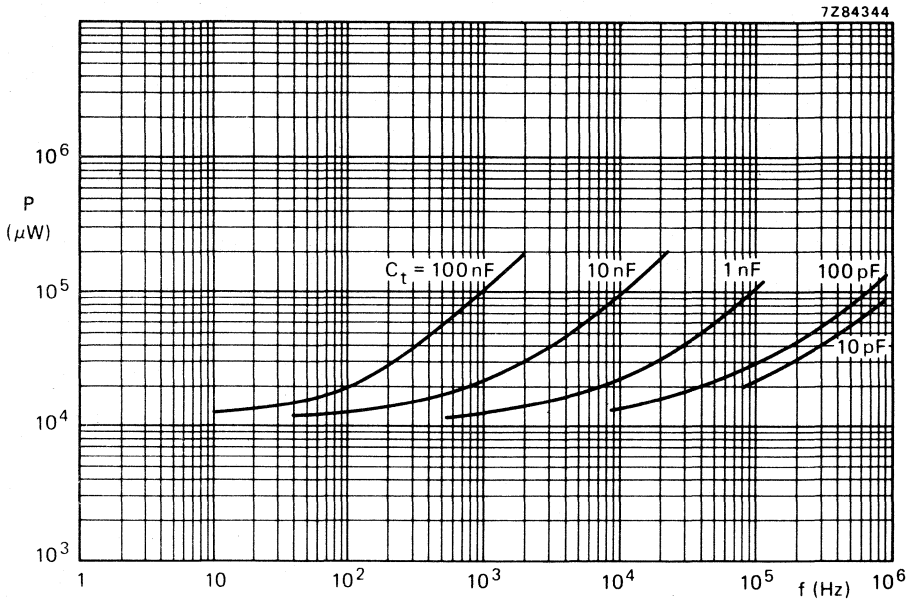


Fig. 12 Power consumption as a function of the output frequency at O or \bar{O} ; $V_{DD} = 15 \text{ V}$; astable mode.

HEX INVERTING BUFFERS



The HEF4049B provides six inverting buffers with high current output capability suitable for driving TTL or high capacitive loads. Since input voltages in excess of the buffers' supply voltage are permitted, the buffers may also be used to convert logic levels of up to 15 V to standard TTL levels. Their guaranteed fan-out into common bipolar logic elements is shown in the table on next page.

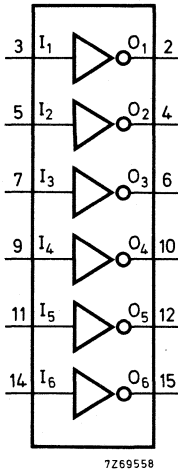


Fig. 1 Functional diagram.

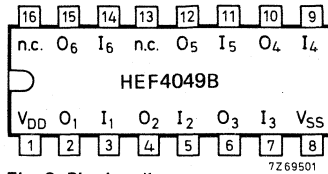


Fig. 2 Pinning diagram.

HEF4049BP: 16-lead DIL; plastic (SOT-38Z).
HEF4049BD: 16-lead DIL; ceramic (SOT-74).
HEF4049BT: 16-lead flat pack; plastic (SO-16; SOT-109A).

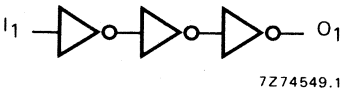


Fig. 3 Logic diagram (one gate).

APPLICATION INFORMATION

Some examples of applications for the HEF4049B are:

- LOCMOS to DTL/TTL converter
- HIGH sink current for driving 2 TTL loads
- HIGH-to-LOW level logic conversion

FAMILY DATA

I_{DD} LIMITS category BUFFERS

} see Family Specifications

HEF4049B

buffers

Guaranteed fan-out in common logic families

driven element	guaranteed fan-out
standard TTL	2
74LS	9
74L	16

Input protection

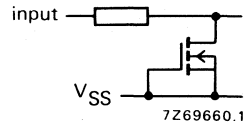


Fig. 4 Input protection circuit that allows input voltages in excess of V_{DD} .

D.C. CHARACTERISTICS $V_{SS} = 0\text{ V}$; $V_I = V_{SS}$ or V_{DD}

	V_{DD} V	V_O V	symbol	$T_{amb}(^{\circ}\text{C})$						
				-40		+25		+85		
				min.	max.	min.	max.	min.	max.	
Output (sink) current LOW	4,75	0,4	I_{OL}	3,5	—	2,9	—	2,3	—	mA
	10	0,5		12,0	—	10,0	—	8,0	—	mA
	15	1,5		24,0	—	20,0	—	16,0	—	mA
Output (source) current HIGH	5	4,6	$-I_{OH}$	0,52	—	0,44	—	0,36	—	mA
	10	9,5		1,3	—	1,1	—	0,9	—	mA
	15	13,5		3,6	—	3,0	—	2,4	—	mA
Output (source) current HIGH	5	2,5	$-I_{OH}$	1,7	—	1,4	—	1,1	—	mA

A.C. CHARACTERISTICS $V_{SS} = 0\text{ V}$; $T_{amb} = 25^{\circ}\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	symbol	typ.		max.	typical extrapolation formula
Propagation delays $I_n \rightarrow O_n$ HIGH to LOW	5	t_{PHL}	50	100	ns	$41\text{ ns} + (0,18\text{ ns/pF}) C_L$
	10		20	45	ns	$16\text{ ns} + (0,08\text{ ns/pF}) C_L$
	15		15	30	ns	$13\text{ ns} + (0,05\text{ ns/pF}) C_L$
LOW to HIGH	5	t_{PLH}	60	125	ns	$33\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10		30	60	ns	$19\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15		25	50	ns	$17\text{ ns} + (0,16\text{ ns/pF}) C_L$
Output transition times HIGH to LOW	5	t_{THL}	25	50	ns	$7\text{ ns} + (0,35\text{ ns/pF}) C_L$
	10		10	20	ns	$3\text{ ns} + (0,14\text{ ns/pF}) C_L$
	15		7	14	ns	$2\text{ ns} + (0,09\text{ ns/pF}) C_L$
LOW to HIGH	5	t_{TLH}	60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$
	10		30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$
	15		20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$3300 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz)
	10	$15\ 500 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_o = output freq. (MHz)
	15	$55\ 200 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	C_L = load capacitance (pF)
			$\Sigma(f_o C_L)$ = sum of outputs
			V_{DD} = supply voltage (V)



HEX NON-INVERTING BUFFERS

The HEF4050B provides six non-inverting buffers with high current output capability suitable for driving TTL or high capacitive loads. Since input voltages in excess of the buffers' supply voltage are permitted, the buffers may also be used to convert logic levels of up to 15 V to standard TTL levels. Their guaranteed fan-out into common bipolar logic elements is shown in the table on next page.

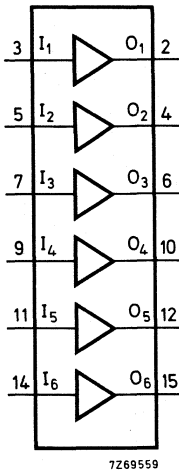


Fig. 1 Functional diagram.

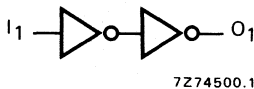


Fig. 3 Logic diagram (one gate).

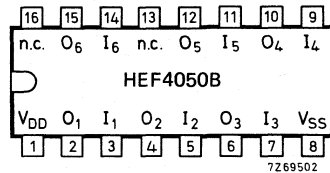


Fig. 2 Pinning diagram.

HEF4050BP: 16-lead DIL; plastic (SOT-38Z).
HEF4050BD: 16-lead DIL; ceramic (SOT-74).
HEF4050BT: 16-lead flat pack; plastic (SO-16; SOT-109A).

APPLICATION INFORMATION

Some examples of applications for the HEF4050B are:

- LOCMOS to DTL/TTL converter
- HIGH sink current for driving 2 TTL loads
- HIGH-to-LOW level logic conversion

FAMILY DATA

I_{DD} LIMITS category BUFFERS

} see Family Specifications

HEF4050B

buffers

Guaranteed fan-out in common logic families

driven element	guaranteed fan-out
standard TTL	2
74LS	9
74L	16

Input protection

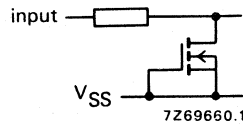


Fig.4 Input protection circuit that allows input voltages in excess of V_{DD} .

D.C. CHARACTERISTICS $V_{SS} = 0\text{ V}$; $V_I = V_{SS}$ or V_{DD}

	V_{DD} V	V_O V	symbol	$T_{amb} (^{\circ}\text{C})$						
				-40		+25		+85		
				min.	max.	min.	max.	min.	max.	
Output (sink) current LOW	4,75	0,4	I_{OL}	3,5	—	2,9	—	2,3	—	mA
	10	0,5		12,0	—	10,0	—	8,0	—	mA
	15	1,5		24,0	—	20,0	—	16,0	—	mA
Output (source) current HIGH	5	4,6	$-I_{OH}$	0,52	—	0,44	—	0,36	—	mA
	10	9,5		1,3	—	1,1	—	0,9	—	mA
	15	13,5		3,6	—	3,0	—	2,4	—	mA
Output (source) current HIGH	5	2,5	$-I_{OH}$	1,7	—	1,4	—	1,1	—	mA

A.C. CHARACTERISTICS $V_{SS} = 0\text{ V}$; $T_{amb} = 25^{\circ}\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	symbol	typ.	max.	typical extrapolation formula
Propagation delays $I_n \rightarrow O_n$ HIGH to LOW	5	t_{PHL}	35	70	26 ns + (0,18 ns/pF) C_L
	10		20	35	16 ns + (0,08 ns/pF) C_L
	15		15	30	12 ns + (0,05 ns/pF) C_L
LOW to HIGH	5	t_{PLH}	55	110	28 ns + (0,55 ns/pF) C_L
	10		25	55	14 ns + (0,23 ns/pF) C_L
	15		20	40	12 ns + (0,16 ns/pF) C_L
Output transition times HIGH to LOW	5	t_{THL}	25	50	7 ns + (0,35 ns/pF) C_L
	10		10	20	3 ns + (0,14 ns/pF) C_L
	15		7	14	2 ns + (0,09 ns/pF) C_L
LOW to HIGH	5	t_{TLH}	60	120	10 ns + (1,0 ns/pF) C_L
	10		30	60	9 ns + (0,42 ns/pF) C_L
	15		20	40	6 ns + (0,28 ns/pF) C_L

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$3\,800 f_i + \sum (f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz)
	10		f_o = output freq. (MHz)
	15		C_L = load capacitance (pF)
			$\sum (f_o C_L)$ = sum of outputs
			V_{DD} = supply voltage (V)

8-CHANNEL ANALOGUE MULTIPLEXER/DEMULTIPLEXER



The HEF4051B is an 8-channel analogue multiplexer/demultiplexer with three address inputs (A_0 to A_2), an active LOW enable input (\bar{E}), eight independent inputs/outputs (Y_0 to Y_7) and a common input/output (Z).

The device contains eight bidirectional analogue switches, each with one side connected to an independent input/output (Y_0 to Y_7) and the other side connected to a common input/output (Z).

With \bar{E} LOW, one of the eight switches is selected (low impedance ON-state) by A_0 to A_2 . With \bar{E} HIGH, all switches are in the high impedance OFF-state, independent of A_0 to A_2 .

V_{DD} and V_{SS} are the supply voltage connections for the digital control inputs (A_0 to A_2 , and \bar{E}). The V_{DD} to V_{SS} range is 3 to 15 V. The analogue inputs/outputs (Y_0 to Y_7 , and Z) can swing between V_{DD} as a positive limit and V_{EE} as a negative limit. $V_{DD}-V_{EE}$ may not exceed 15 V.

For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to V_{SS} (typically ground).

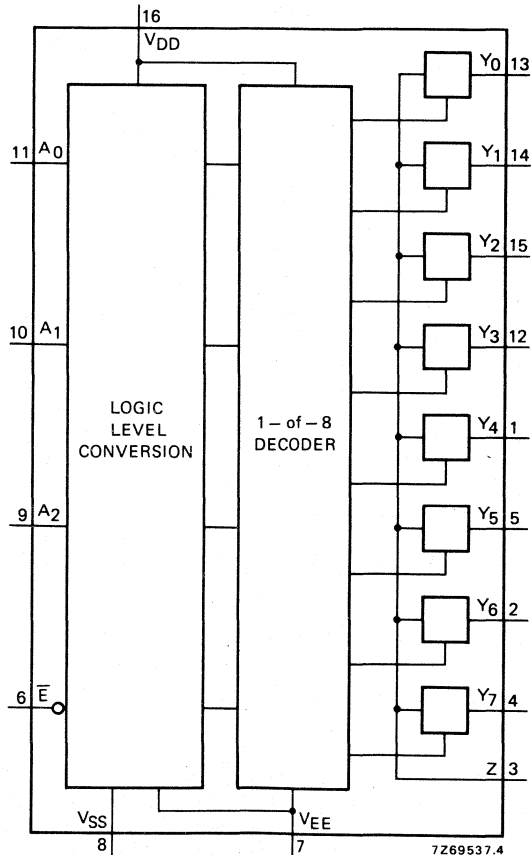


Fig. 1 Functional diagram.

FAMILY DATA

I_{DD} LIMITS category MSI
see Family Specifications

HEF4051B

MSI

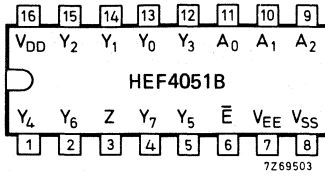


Fig. 2 Pinning diagram.

PINNING

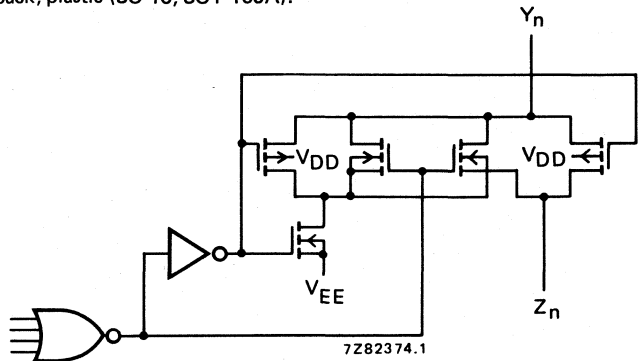
- Y₀ to Y₇ independent inputs/outputs
- A₀ to A₂ address inputs
- E enable input (active LOW)
- Z common input/output

HEF4051BP: 16-lead DIL; plastic (SOT-38Z).

HEF4051BD: 16-lead DIL; ceramic (SOT-74).

HEF4051BT: 16-lead flat pack; plastic (SO-16; SOT-109A).

Fig. 3 Schematic diagram (one switch).



FUNCTION TABLE

E-bar	inputs			channel ON
	A ₂	A ₁	A ₀	
L	L	L	L	Y ₀ -Z
L	L	L	H	Y ₁ -Z
L	L	H	L	Y ₂ -Z
L	L	H	H	Y ₃ -Z
L	H	L	L	Y ₄ -Z
L	H	L	H	Y ₅ -Z
L	H	H	L	Y ₆ -Z
L	H	H	H	Y ₇ -Z
H	X	X	X	none

- H = HIGH state (the more positive voltage)
- L = LOW state (the less positive voltage)
- X = state is immaterial

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (with reference to V_{DD})

V_{EE} -18 to +0,5 V

NOTE

To avoid drawing V_{DD} current out of terminal Z, when switch current flows into terminals Y, the voltage drop across the bidirectional switch must not exceed 0,4 V. If the switch current flows into terminal Z, no V_{DD} current will flow out of terminals Y, in this case there is no limit for the voltage drop across the switch, but the voltages at Y and Z may not exceed V_{DD} or V_{EE}.

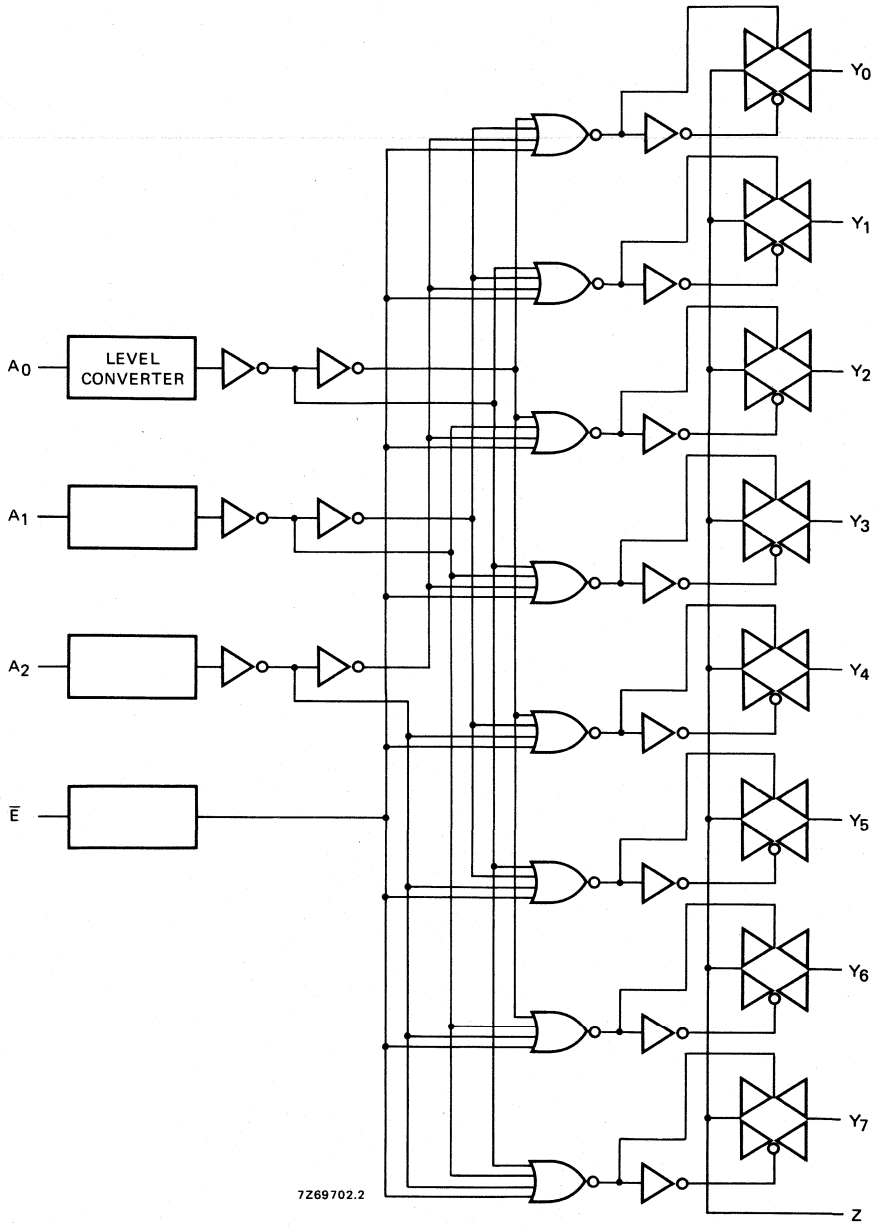


Fig. 4 Logic diagram.

D.C. CHARACTERISTICS

$T_{amb} = 25\text{ }^{\circ}\text{C}$

	$V_{DD}-V_{EE}$ V	symbol	typ.	max.	conditions
ON resistance	5	R_{ON}	350	2500 Ω	} $V_{is} = 0$ to $V_{DD}-V_{EE}$ see Fig. 6
	10		80	245 Ω	
	15		60	175 Ω	
ON resistance	5	R_{ON}	115	340 Ω	} $V_{is} = 0$ see Fig. 6
	10		50	160 Ω	
	15		40	115 Ω	
ON resistance	5	R_{ON}	120	365 Ω	} $V_{is} = V_{DD}-V_{EE}$ see Fig. 6
	10		65	200 Ω	
	15		50	155 Ω	
' Δ ' ON resistance between any two channels	5	ΔR_{ON}	25	— Ω	} $V_{is} = 0$ to $V_{DD}-V_{EE}$ see Fig. 6
	10		10	— Ω	
	15		5	— Ω	
OFF-state leakage current, all channels OFF	5	I_{OZZ}	—	— nA	} \bar{E} at V_{DD}
	10		—	— nA	
	15		—	1000 nA	
OFF-state leakage current, any channel	5	I_{OZY}	—	— nA	} \bar{E} at V_{SS}
	10		—	— nA	
	15		—	200 nA	

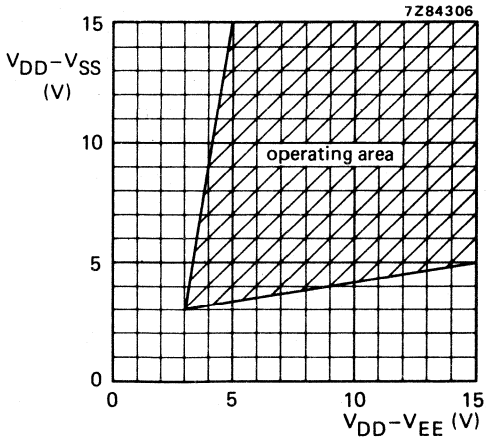


Fig. 5 Operating area as a function of the supply voltages.

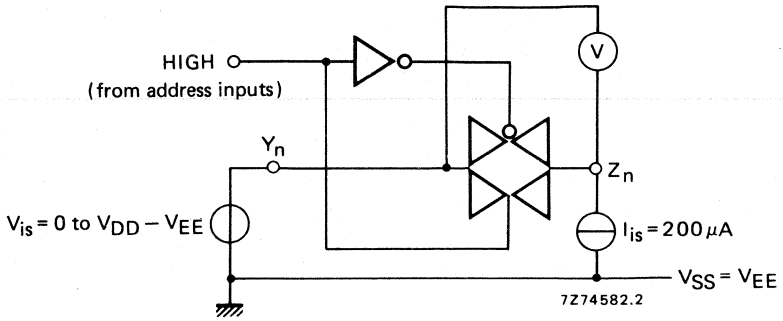


Fig. 6 Test set-up for measuring R_{ON} .

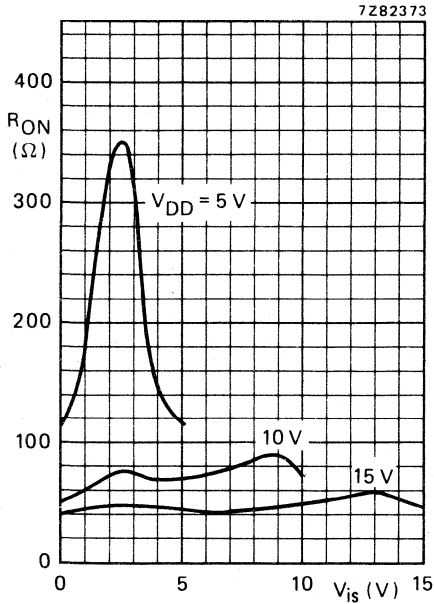


Fig. 7 Typical R_{ON} as a function of input voltage.

$I_{is} = 200 \mu A$
 $V_{SS} = V_{EE} = 0 V$

A.C. CHARACTERISTICS

 $V_{EE} = V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^\circ\text{C}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	typical formula for P (μW)	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
Dynamic power dissipation per package (P)	5	$1\,200 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	10	$5\,700 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$15\,000 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

A.C. CHARACTERISTICS

 $V_{EE} = V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^\circ\text{C}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	symbol	typ. max.		
Propagation delays $V_{is} \rightarrow V_{os}$ HIGH to LOW	5	tPHL	15	25	ns } note 1
	10		5	10	
	15		5	10	
LOW to HIGH	5	tPLH	15	25	ns } note 1
	10		5	10	
	15		5	10	
$A_n \rightarrow V_{os}$ HIGH to LOW	5	tPHL	170	345	ns } note 2
	10		65	125	
	15		50	100	
LOW to HIGH	5	tPLH	160	320	ns } note 2
	10		65	130	
	15		45	90	
Output disable times $\bar{E} \rightarrow V_{os}$ HIGH	5	tPHZ	125	250	ns } note 3
	10		90	180	
	15		85	170	
LOW	5	tPLZ	155	310	ns } note 3
	10		120	240	
	15		115	230	
Output enable times $\bar{E} \rightarrow V_{os}$ HIGH	5	tpZH	190	380	ns } note 3
	10		75	145	
	15		50	100	
LOW	5	tpZL	195	385	ns } note 3
	10		75	145	
	15		50	100	

A.C. CHARACTERISTICS

 $V_{EE} = V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	symbol	typ.	max.	
Distortion, sine-wave response	5		0,25	%	} note 4
	10		0,04	%	
	15		0,04	%	
Crosstalk between any two channels	5		—	MHz	} note 5
	10		1	MHz	
	15		—	MHz	
Crosstalk; enable or address input to output	5		—	mV	} note 6
	10		50	mV	
	15		—	mV	
OFF-state feed-through	5		—	MHz	} note 7
	10		1	MHz	
	15		—	MHz	
ON-state frequency response	5		13	MHz	} note 8
	10		40	MHz	
	15		70	MHz	

NOTES

 V_{is} is the input voltage at a Y or Z terminal, whichever is assigned as input.

 V_{os} is the output voltage at a Y or Z terminal, whichever is assigned as output.

- $R_L = 10\text{ k}\Omega$ to V_{EE} ; $C_L = 50\text{ pF}$ to V_{EE} ; $\bar{E} = V_{SS}$; $V_{is} = V_{DD}$ (square-wave); see Fig. 8.
- $R_L = 10\text{ k}\Omega$; $C_L = 50\text{ pF}$ to V_{EE} ; $\bar{E} = V_{SS}$; $A_n = V_{DD}$ (square-wave); $V_{is} = V_{DD}$ and R_L to V_{EE} for t_{PLH} ; $V_{is} = V_{EE}$ and R_L to V_{DD} for t_{PHL} ; see Fig. 8.
- $R_L = 10\text{ k}\Omega$; $C_L = 50\text{ pF}$ to V_{EE} ; $\bar{E} = V_{DD}$ (square-wave); $V_{is} = V_{DD}$ and R_L to V_{EE} for t_{PHZ} and t_{PZH} ; $V_{is} = V_{EE}$ and R_L to V_{DD} for t_{PLZ} and t_{PZL} ; see Fig. 8.
- $R_L = 10\text{ k}\Omega$; $C_L = 15\text{ pF}$; channel ON; $V_{is} = \frac{1}{2} V_{DD(p-p)}$ (sine-wave, symmetrical about $\frac{1}{2} V_{DD}$); $f_{is} = 1\text{ kHz}$; see Fig. 9.
- $R_L = 1\text{ k}\Omega$; $V_{is} = \frac{1}{2} V_{DD(p-p)}$ (sine-wave, symmetrical about $\frac{1}{2} V_{DD}$); $20 \log \frac{V_{os}}{V_{is}} = -50\text{ dB}$; see Fig. 10.
- $R_L = 10\text{ k}\Omega$ to V_{EE} ; $C_L = 15\text{ pF}$ to V_{EE} ; \bar{E} or $A_n = V_{DD}$ (square-wave); crosstalk is $|V_{os}|$ (peak value); see Fig. 8.
- $R_L = 1\text{ k}\Omega$; $C_L = 5\text{ pF}$; channel OFF; $V_{is} = \frac{1}{2} V_{DD(p-p)}$ (sine-wave, symmetrical about $\frac{1}{2} V_{DD}$); $20 \log \frac{V_{os}}{V_{is}} = -50\text{ dB}$; see Fig. 9.
- $R_L = 1\text{ k}\Omega$; $C_L = 5\text{ pF}$; channel ON; $V_{is} = \frac{1}{2} V_{DD(p-p)}$ (sine-wave, symmetrical about $\frac{1}{2} V_{DD}$); $20 \log \frac{V_{os}}{V_{is}} = -3\text{ dB}$; see Fig. 9.

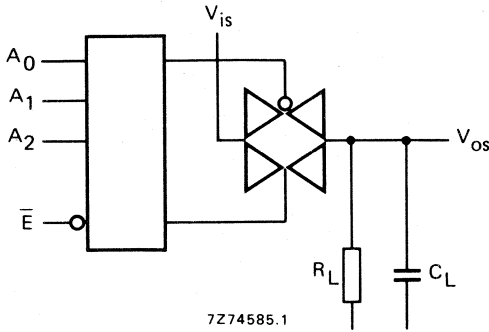


Fig. 8.

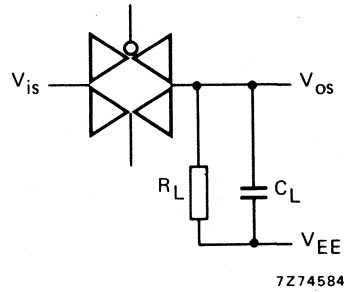


Fig. 9.

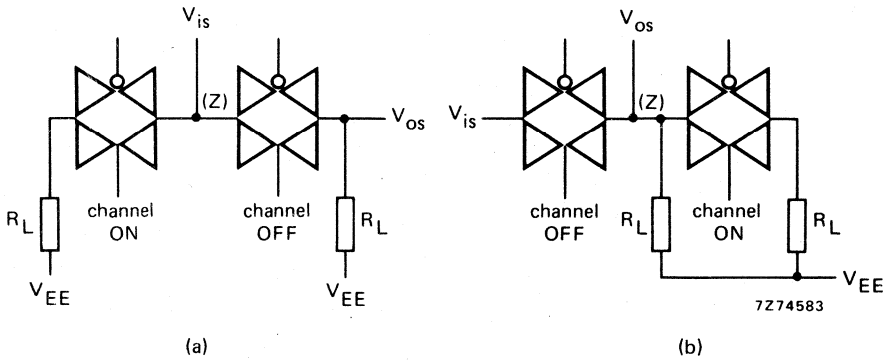


Fig. 10.

APPLICATION INFORMATION

Some examples of applications for the HEF4051B are:

- Analogue multiplexing and demultiplexing.
- Digital multiplexing and demultiplexing.
- Signal gating.

NOTE

If break before make is needed, then it is necessary to use the enable input.

DUAL 4-CHANNEL ANALOGUE MULTIPLEXER/DEMULTIPLEXER

The HEF4052B is a dual 4-channel analogue multiplexer/demultiplexer with common channel select logic. Each multiplexer/demultiplexer has four independent inputs/outputs (Y_0 to Y_3) and a common input/output (Z). The common channel select logic includes two address inputs (A_0 and A_1) and an active LOW enable input (\bar{E}).

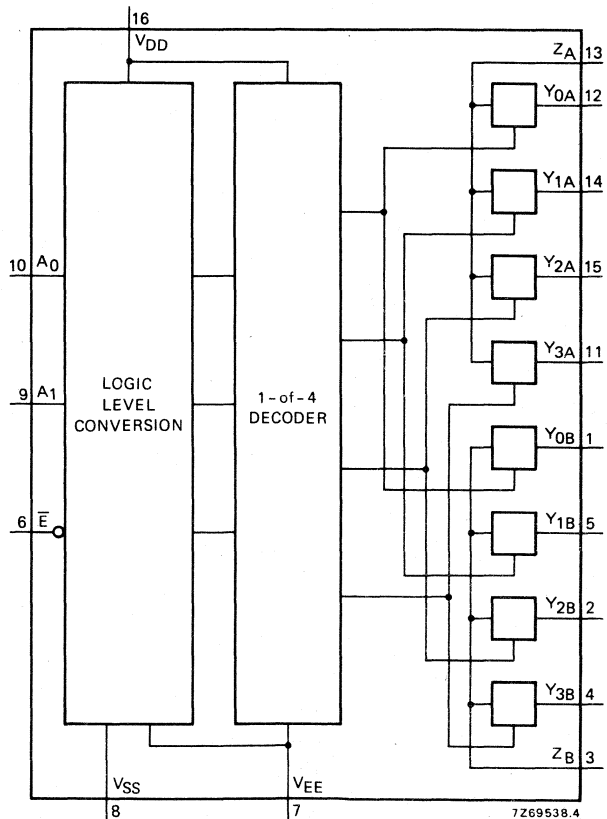
Both multiplexers/demultiplexers contain four bidirectional analogue switches, each with one side connected to an independent input/output (Y_0 to Y_3) and the other side connected to a common input/output (Z).

With \bar{E} LOW, one of the four switches is selected (low impedance ON-state) by A_0 and A_1 . With \bar{E} HIGH, all switches are in the high impedance OFF-state, independent of A_0 and A_1 .

V_{DD} and V_{SS} are the supply voltage connections for the digital control inputs (A_0 , A_1 and \bar{E}). The V_{DD} to V_{SS} range is 3 to 15 V. The analogue inputs/outputs (Y_0 to Y_3 , and Z) can swing between V_{DD} as a positive limit and V_{EE} as a negative limit. $V_{DD} - V_{EE}$ may not exceed 15 V.

For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to V_{SS} (typically ground).

Fig. 1 Functional diagram.



FAMILY DATA

I_{DD} LIMITS category MSI
see Family Specifications

HEF4052B

MSI

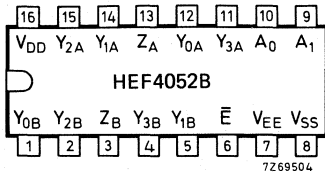


Fig. 2 Pinning diagram.

PINNING

- Y0A to Y3A independent inputs/outputs
- Y0B to Y3B independent inputs/outputs
- A0, A1 address inputs
- \bar{E} enable input (active LOW)
- Z_A, Z_B common inputs/outputs

HEF4052BP: 16-lead DIL; plastic (SOT-38Z).
 HEF4052BD: 16-lead DIL; ceramic (SOT-74).
 HEF4052BT: 16-lead flat pack; plastic (SO-16; SOT-109A).

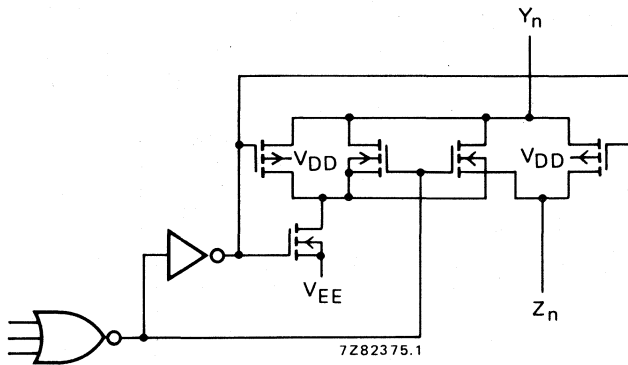


Fig. 3 Schematic diagram (one switch).

FUNCTION TABLE

inputs			channel ON
\bar{E}	A ₁	A ₀	
L	L	L	Y _{0A} -Z _A ; Y _{0B} -Z _B
L	L	H	Y _{1A} -Z _A ; Y _{1B} -Z _B
L	H	L	Y _{2A} -Z _A ; Y _{2B} -Z _B
L	H	H	Y _{3A} -Z _A ; Y _{3B} -Z _B
H	X	X	none

H = HIGH state (the more positive voltage)
 L = LOW state (the less positive voltage)
 X = state is immaterial

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (with reference to V_{DD}) V_{EE} -18 to +0,5 V

NOTE

To avoid drawing V_{DD} current out of terminal Z, when switch current flows into terminals Y, the voltage drop across the bidirectional switch must not exceed 0,4 V. If the switch current flows into terminal Z, no V_{DD} current will flow out of terminals Y, in this case there is no limit for the voltage drop across the switch, but the voltages at Y and Z may not exceed V_{DD} or V_{EE}.

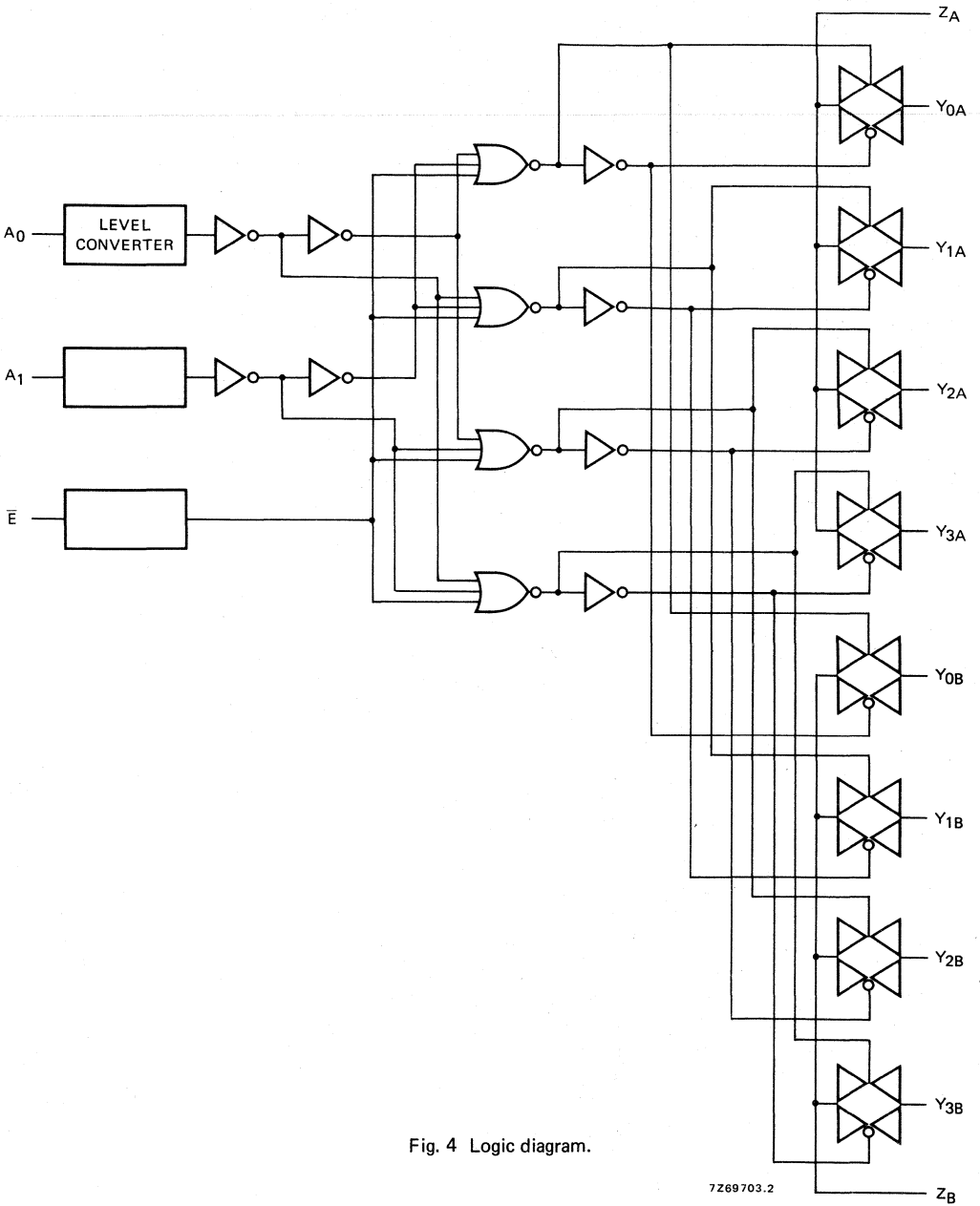


Fig. 4 Logic diagram.

7269703.2

D.C. CHARACTERISTICS

T_{amb} = 25 °C

	$V_{DD}-V_{EE}$ V	symbol	typ.	max.	conditions
ON resistance	5	R _{ON}	350	2500	} $V_{is} = 0$ to $V_{DD}-V_{EE}$ see Fig. 6
	10		80	245	
	15		60	175	
ON resistance	5	R _{ON}	115	340	} $V_{is} = 0$ see Fig. 6
	10		50	160	
	15		40	115	
ON resistance	5	R _{ON}	120	365	} $V_{is} = V_{DD}-V_{EE}$ see Fig. 6
	10		65	200	
	15		50	155	
'Δ' ON resistance between any two channels	5	ΔR _{ON}	25	—	} $V_{is} = 0$ to $V_{DD}-V_{EE}$ see Fig. 6
	10		10	—	
	15		5	—	
OFF-state leakage current, all channels OFF	5	I _{OZZ}	—	—	} \bar{E} at V_{DD}
	10		—	—	
	15		—	1000	
OFF-state leakage current, any channel	5	I _{OZY}	—	—	} \bar{E} at V_{SS}
	10		—	—	
	15		—	200	

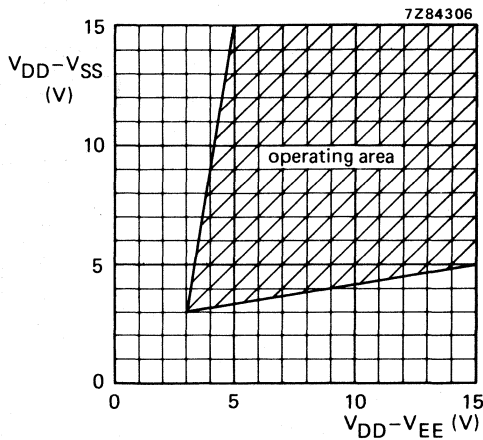


Fig. 5 Operating area as a function of the supply voltages.

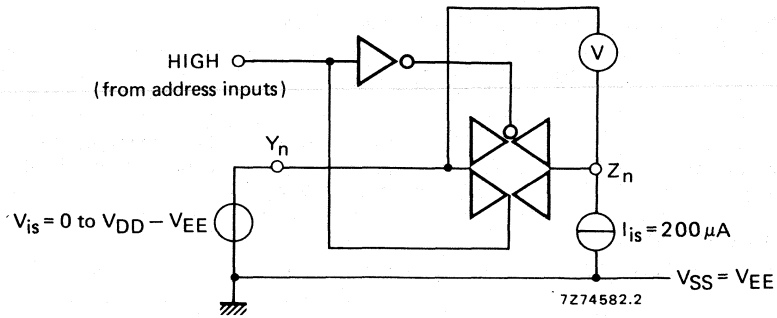


Fig. 6 Test set-up for measuring R_{ON} .

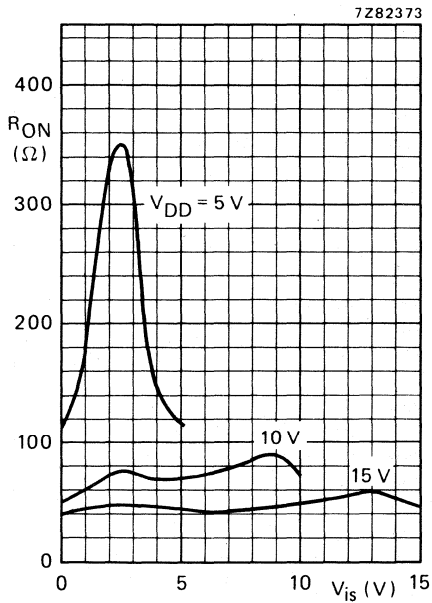


Fig. 7 Typical R_{ON} as a function of input voltage.

$I_{is} = 200 \mu A$
 $V_{SS} = V_{EE} = 0 V$

A.C. CHARACTERISTICS

$V_{EE} = V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^\circ\text{C}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	typical formula for P (μW)	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
Dynamic power dissipation per package (P)	5	$1\ 300\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	10	$6\ 100\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$15\ 600\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

A.C. CHARACTERISTICS

$V_{EE} = V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^\circ\text{C}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	symbol	typ.	max.	
Propagation delays $V_{is} \rightarrow V_{os}$ HIGH to LOW	5	t _{PHL}	10	20	ns } note 1
	10		5	10	
	15		5	10	
LOW to HIGH	5	t _{PLH}	10	20	ns } note 1
	10		5	10	
	15		5	10	
$A_n \rightarrow V_{os}$ HIGH to LOW	5	t _{PHL}	150	305	ns } note 2
	10		65	135	
	15		50	100	
LOW to HIGH	5	t _{PLH}	75	150	ns } note 2
	10		35	75	
	15		30	55	
Output disable times $\bar{E} \rightarrow V_{os}$ HIGH	5	t _{PHZ}	100	205	ns } note 3
	10		90	180	
	15		90	180	
LOW	5	t _{PLZ}	95	190	ns } note 3
	10		90	180	
	15		90	180	
Output enable times $\bar{E} \rightarrow V_{os}$ HIGH	5	t _{PZH}	130	260	ns } note 3
	10		55	115	
	15		45	85	
LOW	5	t _{PZL}	120	240	ns } note 3
	10		50	100	
	15		35	75	

A.C. CHARACTERISTICS

$V_{EE} = V_{SS} = 0\text{ V}$; $T_{\text{amb}} = 25\text{ }^{\circ}\text{C}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	symbol	typ. max.		
Distortion, sine-wave response	5		0,25	%	} note 4
	10		0,04	%	
	15		0,04	%	
Crosstalk between any two channels	5		—	MHz	} note 5
	10		1	MHz	
	15		—	MHz	
Crosstalk; enable or address input to output	5		—	mV	} note 6
	10		50	mV	
	15		—	mV	
OFF-state feed-through	5		—	MHz	} note 7
	10		1	MHz	
	15		—	MHz	
ON-state frequency response	5		13	MHz	} note 8
	10		40	MHz	
	15		70	MHz	

NOTES

V_{is} is the input voltage at a Y or Z terminal, whichever is assigned as input.

V_{os} is the output voltage at a Y or Z terminal, whichever is assigned as output.

- $R_L = 10\text{ k}\Omega$ to V_{EE} ; $C_L = 50\text{ pF}$ to V_{EE} ; $\bar{E} = V_{SS}$; $V_{is} = V_{DD}$ (square-wave); see Fig. 8.
- $R_L = 10\text{ k}\Omega$; $C_L = 50\text{ pF}$ to V_{EE} ; $\bar{E} = V_{SS}$; $A_n = V_{DD}$ (square-wave); $V_{is} = V_{DD}$ and R_L to V_{EE} for t_{pLH} ; $V_{is} = V_{EE}$ and R_L to V_{DD} for t_{pHL} ; see Fig. 8.
- $R_L = 10\text{ k}\Omega$; $C_L = 50\text{ pF}$ to V_{EE} ; $\bar{E} = V_{DD}$ (square-wave); $V_{is} = V_{DD}$ and R_L to V_{EE} for t_{pHZ} and t_{pZH} ; $V_{is} = V_{EE}$ and R_L to V_{DD} for t_{pLZ} and t_{pZL} ; see Fig. 8.
- $R_L = 10\text{ k}\Omega$; $C_L = 15\text{ pF}$; channel ON; $V_{is} = \frac{1}{2} V_{DD(p-p)}$ (sine-wave, symmetrical about $\frac{1}{2} V_{DD}$); $f_{is} = 1\text{ kHz}$; see Fig. 9.
- $R_L = 1\text{ k}\Omega$; $V_{is} = \frac{1}{2} V_{DD(p-p)}$ (sine-wave, symmetrical about $\frac{1}{2} V_{DD}$); $20 \log \frac{V_{os}}{V_{is}} = -50\text{ dB}$; see Fig. 10.
- $R_L = 10\text{ k}\Omega$ to V_{EE} ; $C_L = 15\text{ pF}$ to V_{EE} ; \bar{E} or $A_n = V_{DD}$ (square-wave); crosstalk is $|V_{os}|$ (peak value); see Fig. 8.
- $R_L = 1\text{ k}\Omega$; $C_L = 5\text{ pF}$; channel OFF; $V_{is} = \frac{1}{2} V_{DD(p-p)}$ (sine-wave, symmetrical about $\frac{1}{2} V_{DD}$); $20 \log \frac{V_{os}}{V_{is}} = -50\text{ dB}$; see Fig. 9.
- $R_L = 1\text{ k}\Omega$; $C_L = 5\text{ pF}$; channel ON; $V_{is} = \frac{1}{2} V_{DD(p-p)}$ (sine-wave, symmetrical about $\frac{1}{2} V_{DD}$); $20 \log \frac{V_{os}}{V_{is}} = -3\text{ dB}$; see Fig. 9.

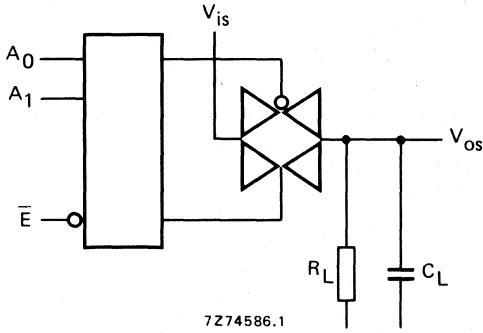


Fig. 8.

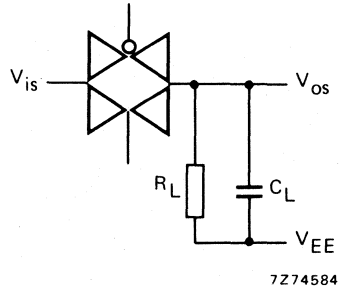


Fig. 9.

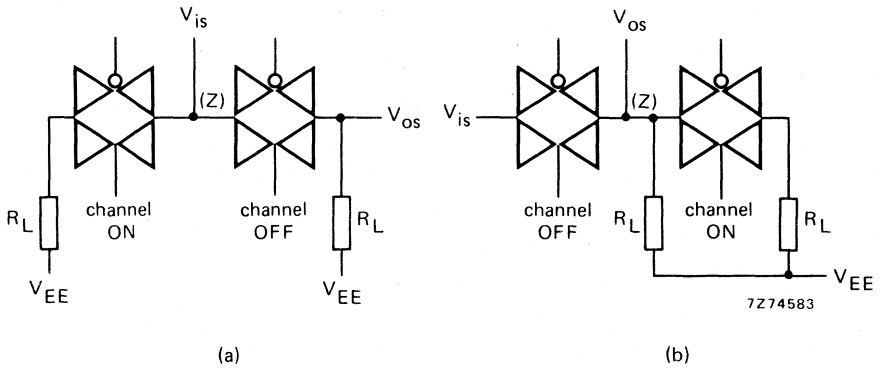


Fig. 10.

APPLICATION INFORMATION

Some examples of applications for the HEF4052B are:

- Analogue multiplexing and demultiplexing.
- Digital multiplexing and demultiplexing.
- Signal gating.

NOTE

If break before make is needed, then it is necessary to use the enable input.

TRIPLE 2-CHANNEL ANALOGUE MULTIPLEXER/DEMULTIPLEXER



The HEF4053B is a triple 2-channel analogue multiplexer/demultiplexer with a common enable input (\bar{E}). Each multiplexer/demultiplexer has two independent inputs/outputs (Y_0 and Y_1), a common input/output (Z), and select inputs (S_n). Each also contains two-bidirectional analogue switches, each with one side connected to an independent input/output (Y_0 and Y_1) and the other side connected to a common input/output (Z).

With \bar{E} LOW, one of the two switches is selected (low impedance ON-state) by S_n . With \bar{E} HIGH, all switches are in the high impedance OFF-state, independent of S_A to S_C .

V_{DD} and V_{SS} are the supply voltage connections for the digital control inputs (S_A to S_C and \bar{E}).

The V_{DD} to V_{SS} range is 3 to 15 V. The analogue inputs/outputs (Y_0 , Y_1 and Z) can swing between V_{DD} as a positive limit and V_{EE} as a negative limit. $V_{DD}-V_{EE}$ may not exceed 15 V.

For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to V_{SS} (typically ground).

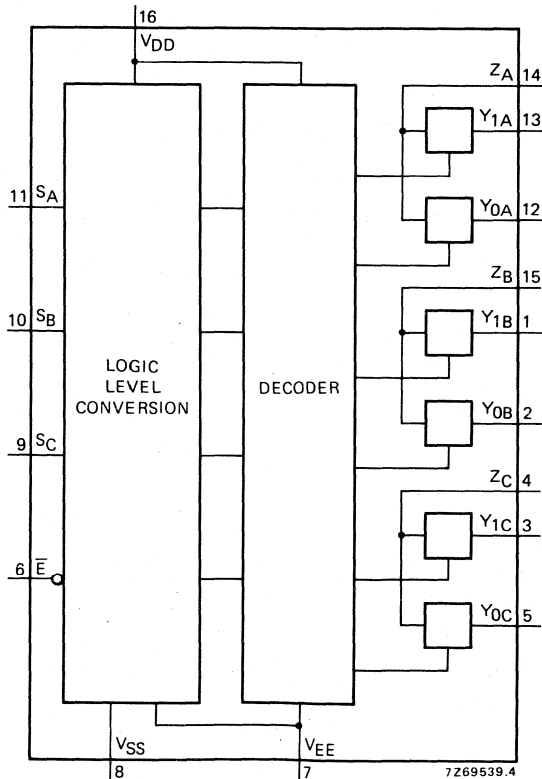


Fig. 1 Functional diagram.

FAMILY DATA

I_{DD} LIMITS category MSI

see Family Specifications

HEF4053B

MSI

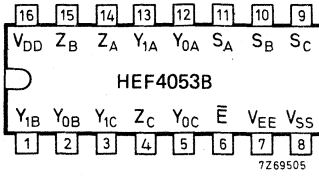


Fig. 2 Pinning diagram.

PINNING

- Y0A to Y0C independent inputs/outputs
- Y1A to Y1C independent inputs/outputs
- SA to SC select inputs
- E-bar enable input (active LOW)
- ZA to ZC common inputs/outputs

- HEF4053BP: 16-lead DIL; plastic (SOT-38Z).
- HEF4053BD: 16-lead DIL; ceramic (SOT-74).
- HEF4053BT: 16-lead flat pack; plastic (SO-16; SOT-109A).

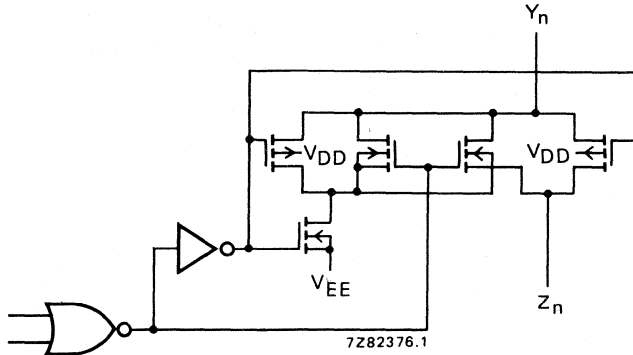


Fig. 3 Schematic diagram (one switch).

FUNCTION TABLE

inputs		channel ON
E-bar	SA	
L	L	Y0A-ZA
L	H	Y1A-ZA
H	X	none

- H = HIGH state (the more positive voltage)
- L = LOW state (the less positive voltage)
- X = state is immaterial

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (with reference to VDD)

V_{EE} -18 to +0,5 V

NOTE

To avoid drawing V_{DD} current out of terminal Z, when switch current flows into terminals Y, the voltage drop across the bidirectional switch must not exceed 0,4 V. If the switch current flows into terminal Z, no V_{DD} current will flow out of terminals Y, in this case there is no limit for the voltage drop across the switch, but the voltages at Y and Z may not exceed V_{DD} or V_{EE}.

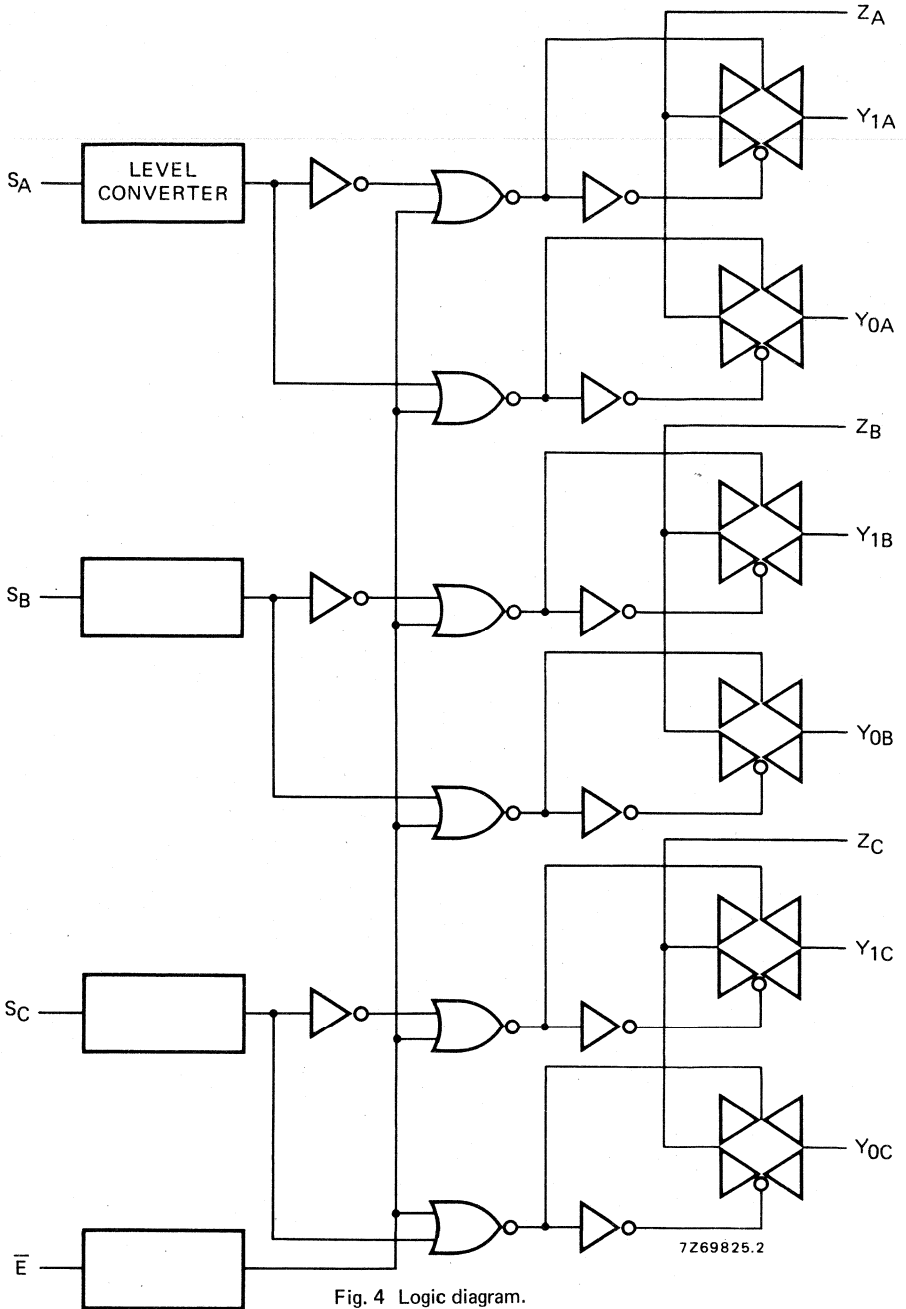


Fig. 4 Logic diagram.

D.C. CHARACTERISTICS

T_{amb} = 25 °C

	$V_{DD}-V_{EE}$ V	symbol	typ.	max.	conditions
ON resistance	5	R _{ON}	350	2500	} $V_{is} = 0$ to $V_{DD}-V_{EE}$ see Fig. 6
	10		80	245	
	15		60	175	
ON resistance	5	R _{ON}	115	340	} $V_{is} = 0$ see Fig. 6
	10		50	160	
	15		40	115	
ON resistance	5	R _{ON}	120	365	} $V_{is} = V_{DD}-V_{EE}$ see Fig. 6
	10		65	200	
	15		50	155	
'Δ' ON resistance between any two channels	5	ΔR _{ON}	25	—	} $V_{is} = 0$ to $V_{DD}-V_{EE}$ see Fig. 6
	10		10	—	
	15		5	—	
OFF-state leakage current, all channels OFF	5	I _{OZZ}	—	—	} \bar{E} at V_{DD}
	10		—	—	
	15		—	1000	
OFF-state leakage current, any channel	5	I _{OZY}	—	—	} \bar{E} at V_{SS}
	10		—	—	
	15		—	200	

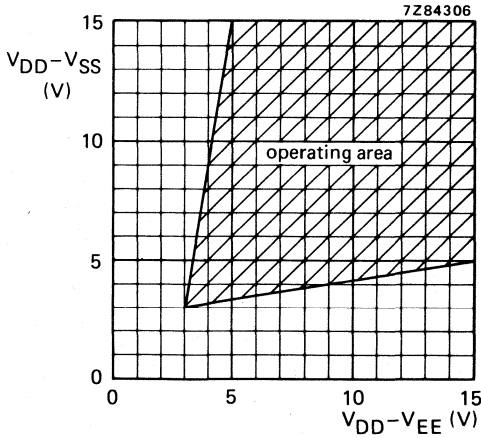


Fig. 5 Operating area as a function of the supply voltages.

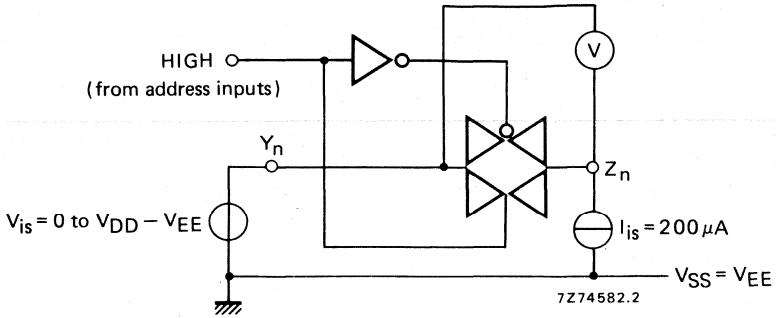


Fig. 6 Test set-up for measuring R_{ON} .

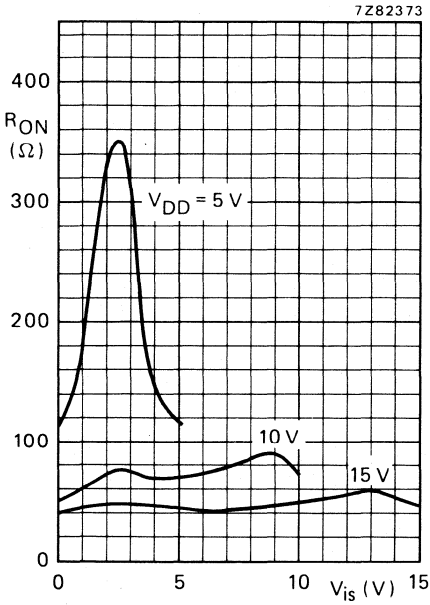


Fig. 7 Typical R_{ON} as a function of input voltage.

$I_{is} = 200 \mu A$
 $V_{SS} = V_{EE} = 0 V$

A.C. CHARACTERISTICS

 $V_{EE} = V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^\circ\text{C}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	typical formula for P (μW)	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
Dynamic power dissipation per package (P)	5	$2\,500 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	10	$11\,500 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$29\,000 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

A.C. CHARACTERISTICS

 $V_{EE} = V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^\circ\text{C}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	symbol	typ.	max.		
Propagation delays $V_{is} \rightarrow V_{os}$ HIGH to LOW	5	t _{PHL}	10	20	ns	} note 1
	10		5	10	ns	
	15		5	10	ns	
LOW to HIGH	5	t _{PLH}	15	30	ns	} note 1
	10		5	10	ns	
	15		5	10	ns	
$S_n \rightarrow V_{os}$ HIGH to LOW	5	t _{PHL}	200	400	ns	} note 2
	10		85	170	ns	
	15		65	130	ns	
LOW to HIGH	5	t _{PLH}	275	555	ns	} note 2
	10		100	200	ns	
	15		65	130	ns	
Output disable times $\bar{E} \rightarrow V_{os}$ HIGH	5	t _{PHZ}	200	400	ns	} note 3
	10		115	230	ns	
	15		110	220	ns	
LOW	5	t _{PLZ}	200	400	ns	} note 3
	10		120	245	ns	
	15		110	215	ns	
Output enable times $\bar{E} \rightarrow V_{os}$ HIGH	5	t _{PZH}	260	525	ns	} note 3
	10		95	190	ns	
	15		65	130	ns	
LOW	5	t _{PZL}	280	565	ns	} note 3
	10		105	205	ns	
	15		70	140	ns	

A.C. CHARACTERISTICS

 $V_{EE} = V_{SS} = 0\text{ V}$; $T_{\text{amb}} = 25\text{ }^{\circ}\text{C}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	symbol	typ.	max.	
Distortion, sine-wave response	5		0,25	%	} note 4
	10		0,04	%	
	15		0,04	%	
Crosstalk between any two channels	5		—	MHz	} note 5
	10		1	MHz	
	15		—	MHz	
Crosstalk; enable or address input to output	5		—	mV	} note 6
	10		50	mV	
	15		—	mV	
OFF-state feed-through	5		—	MHz	} note 7
	10		1	MHz	
	15		—	MHz	
ON-state frequency response	5		13	MHz	} note 8
	10		40	MHz	
	15		70	MHz	

NOTES

 V_{is} is the input voltage at a Y or Z terminal, whichever is assigned as input. V_{os} is the output voltage at a Y or Z terminal, whichever is assigned as output.

- $R_L = 10\text{ k}\Omega$ to V_{EE} ; $C_L = 50\text{ pF}$ to V_{EE} ; $\bar{E} = V_{SS}$; $V_{is} = V_{DD}$ (square-wave); see Fig. 8.
- $R_L = 10\text{ k}\Omega$; $C_L = 50\text{ pF}$ to V_{EE} ; $\bar{E} = V_{SS}$; $S_n = V_{DD}$ (square-wave); $V_{is} = V_{DD}$ and R_L to V_{EE} for t_{PLH} ; $V_{is} = V_{EE}$ and R_L to V_{DD} for t_{PHL} ; see Fig. 8.
- $R_L = 10\text{ k}\Omega$; $C_L = 50\text{ pF}$ to V_{EE} ; $\bar{E} = V_{DD}$ (square-wave); $V_{is} = V_{DD}$ and R_L to V_{EE} for t_{PHZ} and t_{PZH} ; $V_{is} = V_{EE}$ and R_L to V_{DD} for t_{PLZ} and t_{PZL} ; see Fig. 8.
- $R_L = 10\text{ k}\Omega$; $C_L = 15\text{ pF}$; channel ON; $V_{is} = \frac{1}{2} V_{DD(p-p)}$ (sine-wave, symmetrical about $\frac{1}{2} V_{DD}$); $f_{is} = 1\text{ kHz}$; see Fig. 9.
- $R_L = 1\text{ k}\Omega$; $V_{is} = \frac{1}{2} V_{DD(p-p)}$ (sine-wave, symmetrical about $\frac{1}{2} V_{DD}$);
 $20 \log \frac{V_{os}}{V_{is}} = -50\text{ dB}$; see Fig. 10.
- $R_L = 10\text{ k}\Omega$ to V_{EE} ; $C_L = 15\text{ pF}$ to V_{EE} ; \bar{E} or $S_n = V_{DD}$ (square-wave); crosstalk is $|V_{os}|$ (peak value); see Fig. 8.
- $R_L = 1\text{ k}\Omega$; $C_L = 5\text{ pF}$; channel OFF; $V_{is} = \frac{1}{2} V_{DD(p-p)}$ (sine-wave, symmetrical about $\frac{1}{2} V_{DD}$);
 $20 \log \frac{V_{os}}{V_{is}} = -50\text{ dB}$; see Fig. 9.
- $R_L = 1\text{ k}\Omega$; $C_L = 5\text{ pF}$; channel ON; $V_{is} = \frac{1}{2} V_{DD(p-p)}$ (sine-wave, symmetrical about $\frac{1}{2} V_{DD}$);
 $20 \log \frac{V_{os}}{V_{is}} = -3\text{ dB}$; see Fig. 9.

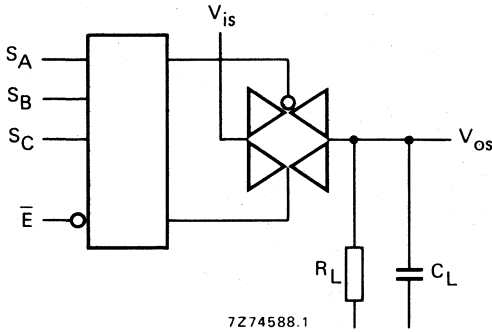


Fig. 8.

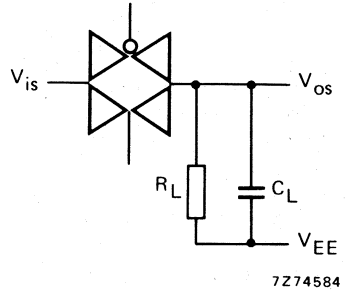


Fig. 9.

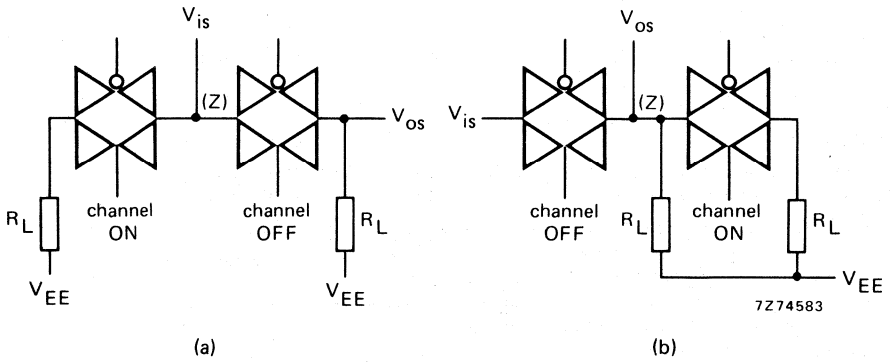


Fig. 10.

APPLICATION INFORMATION

Some examples of applications for the HEF4053B are:

- Analogue multiplexing and demultiplexing.
- Digital multiplexing and demultiplexing.
- Signal gating.

NOTE

If break before make is needed, then it is necessary to use the enable input.

DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

HEF4059B

LSI

PROGRAMMABLE DIVIDE-BY-N COUNTER

The HEF4059B is a divide-by-n counter which can be programmed to divide an input frequency by any number n from 3 to 15 999. The output signal is a one clock-cycle wide pulse and occurs at a rate equal to the input frequency divided by n . The single output (O) has TTL drive capability. The down counter is preset by 16 jam inputs (J1 to J16); continued on next page.

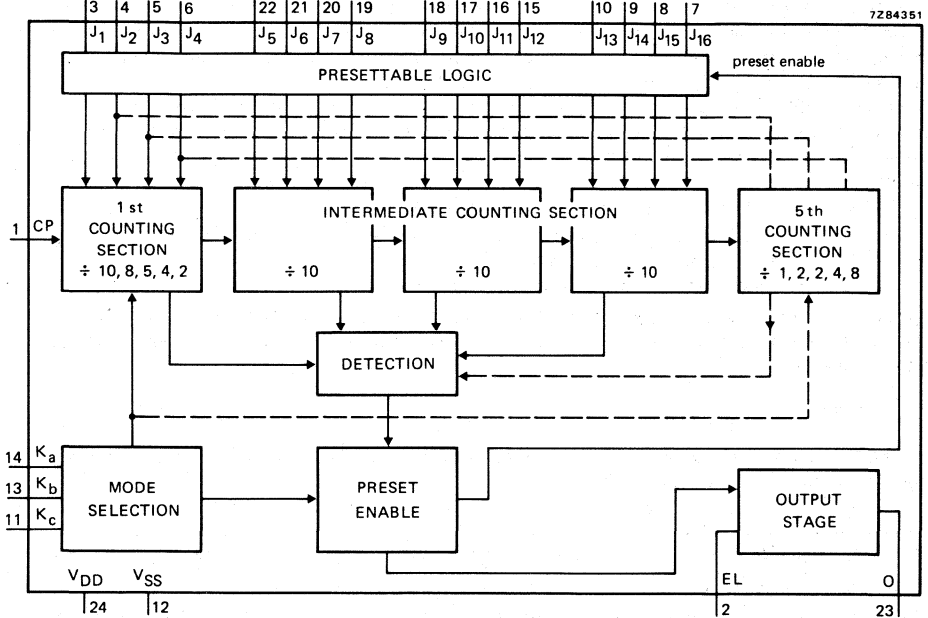


Fig. 1 Functional block diagram.

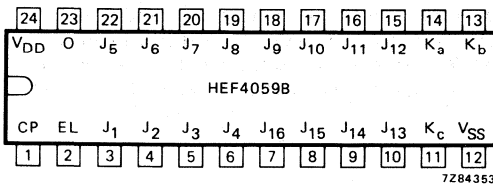


Fig. 2 Pinning diagram.

PINNING

- CP clock input
- K_a, K_b, K_c mode select inputs
- J1 to J16 programmable jam inputs (BCD)
- EL latch enable input
- O divide-by-n output

HEF4059BP: 24-lead DIL; plastic (SOT-101A).
HEF4059BD: 24-lead DIL; ceramic (SOT-94).

FAMILY DATA

I_{DD} LIMITS category LSI

see Family Specifications

The three mode selection inputs K_A , K_B and K_C determine the modulus ('divide-by' number) of the first and last counting sections in accordance with Table 1.

Every time the first (fastest) counting section goes through one cycle, it reduces, by 1, the number that has been preset (jammed) into the three decades of the intermediate counting section and into the last counting section (which consists of flip-flops that are not needed for operating the first counting section).

For example, in the $\div 2$ mode, only one flip-flop is needed in the first counting section. Therefore the last (5th) counting section has three flip-flops that can be preset to a maximum count of seven with a place value of thousands.

This counting mode is selected when K_A , K_B and K_C are set to HIGH. In this case input J_1 is used to preset the first counting section and J_2 to J_4 are used to preset the last (5th) counting section.

If $\div 10$ mode is desired for the first section, K_A is set HIGH, K_B to HIGH and K_C to LOW. The jam inputs J_1 to J_4 are used to preset the first counting section and there is no last counting section. The intermediate counting section consists of three cascaded BCD decade ($\div 10$) counters, presettable by means of the jam inputs J_5 to J_{16} .

When clock pulses are applied to the clock input after a number n has been preset into the counter, the counter counts down until the DETECTION circuit detects the zero state. At this time the PRESET ENABLE circuit is enabled to preset again the number n into the counter and to produce an output pulse.

The preset of the counter to a desired $\div n$ is achieved as follows:

$$n = (\text{MODE}^*) (1000 \times \text{decade 5 preset} + 100 \times \text{decade 4 preset} + 10 \times \text{decade 3 preset} + 1 \times \text{decade 2 preset}) + \text{decade 1 preset}.$$

* MODE = first counting section divider (10, 8, 5, 4 or 2).

To calculate preset values for any n count, divide the n count by the selected mode. The resultant is the corresponding preset values of the 5th to the 2nd decade with the remainder being equal to the 1st decade value.

$$\text{preset value} = \frac{n}{\text{mode}}.$$

If $n = 8479$, and the selected mode = 5, the preset value = $8479 \div 5 = 1695$ with a remainder of 4, thus the jam inputs must be set as follows:

4				1		5			9				6			
J ₁	J ₂	J ₃	J ₄	J ₅	J ₆	J ₇	J ₈	J ₉	J ₁₀	J ₁₁	J ₁₂	J ₁₃	J ₁₄	J ₁₅	J ₁₆	
L	L	H	H	H	L	H	L	H	L	L	H	L	H	H	L	

The mode select inputs permit frequency-synthesizer channel separations of 10, 12, 5, 20, 25 and 50 parts. These inputs set the maximum value of n at 9999 (when the first counting section divides by 5 or 10) or at 15999 (when the first counting section divides by 8, 4 or 2).

The three decades of the intermediate counting section can be preset to a binary 15 instead of a binary 9. In this case the first cycle of a counter consists of 15 count pulses, the next cycles consisting of 10 count pulses. Thus the place value of the three decades are still 1, 10 and 100. For example, in the $\div 8$ mode, the number from which the intermediate counting section begins to count-down can be preset to:

3rd decade:	1500
2nd decade:	150
1st decade:	15
	1665

The last counting section can be preset to a maximum of 1, with a place value of 1000. The total of these numbers (2665) times 8 equals 21 320. The first counting section can be preset to a maximum of 7. Therefore, 21 327 is the maximum possible count in the ÷ 8 mode. The highest count of the various modes is shown in Table 1, in the column entitled 'extended counter range'. Control inputs K_B and K_C can be used to initiate and lock the counter in the 'master preset' mode. In this condition the flip-flops in the counter are preset in accordance with the jam inputs and the counter remains in that mode as long as K_B and K_C both remain LOW. The counter begins to run down from the preset state when a counting mode other than the 'master preset' mode is selected. Whenever the 'master preset' mode is used, control signals $K_B = L$ and $K_C = L$ must be applied for at least 3 full clock pulses. After the master preset mode inputs have been changed to one of the counting modes, the next positive-going clock transition changes an internal flip-flop so that the count-down can begin at the second positive-going clock transition. Thus, after a 'master preset' mode, there is always one extra count before the output goes HIGH. Figure 3 illustrates the operation of the counter in mode ÷ 8 starting from the preset state 3.

DEVELOPMENT SAMPLE DATA

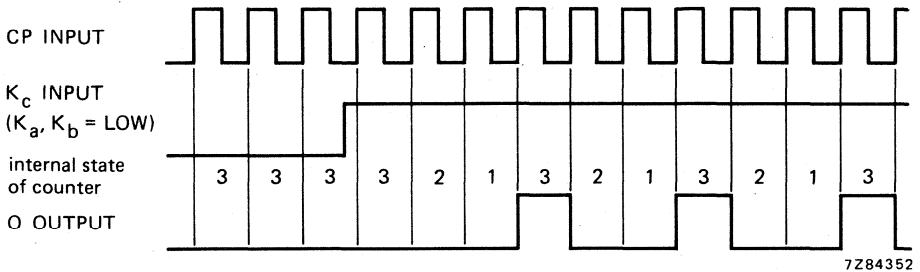


Fig. 3 Total count of 3.

If the 'master preset' mode is started two clock cycles or less before an output pulse, the output pulse will appear at the time due. If the 'master preset' mode is not used the counter is preset in accordance with the 'jam inputs' when the output pulse appears. A HIGH level at the latch enable input (EL) will cause the counter output to remain in the HIGH state until EL input returns to LOW. If the EL input is LOW, the output pulse will remain HIGH for only one cycle of the clock input signal. When $K_a = L, K_b = H, K_c = L$ and $EL = L$, the counter operates in the 'preset inhibit' mode, with which the dividend of the counter is fixed to 10 000, independent of the state of the jam inputs. When in the same state of mode select inputs $EL = H$, the counter operates in the normal ÷ 10 mode, however, without the latch operation at the output. Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

Table 1

latch enable input	mode select inputs			first counting section			last counting section			counter range	
	EL	K _a	K _b	K _c	MODE divides by	max. preset state	jam inputs used	MODE divides by	max. preset state	jam inputs used	design max.
X	H	H	H	2	1	J ₁	8	7	J ₂ J ₃ J ₄	15 999	17 331
X	L	H	H	4	3	J ₁ J ₂	4	3	J ₃ J ₄	15 999	18 663
X	H	L	H	5	4	J ₁ J ₂ J ₃	2	1	J ₄	9 999	13 329
X	L	L	H	8	7	J ₁ J ₂ J ₃	2	1	J ₄	15 999	21 327
X	H	H	L	10	9	J ₁ J ₂ J ₃ J ₄	1	0	—	9 999	16 659
H	L	H	L	10	9	J ₁ J ₂ J ₃ J ₄	1	0	—	9 999	16 659
L	L	H	L	preset inhibit			preset inhibit			fixed 10 000	—
X	X	L	L	master preset			master preset			—	—

D.C. CHARACTERISTICS $V_{SS} = 0 V$

	V_{DD} V	symbol	T_{amb} (°C)			unit	
			-40 min.	+25 min.	+85 min.		
Output (sink) current LOW	4,75	I_{OL}	2,7	2,3	1,8	mA	$V_O = 0,4 V; V_I = 0$ or 4,75 V
	10		9,5	8	6,3	mA	$V_O = 0,5 V; V_I = 0$ or 10 V
	15		24	20	16	mA	$V_O = 1,5 V; V_I = 0$ or 15 V
Output (source) current HIGH	5	$-I_{OH}$	0,8	0,7	0,5	mA	$V_O = 4,6 V; V_I = 0$ or 5 V
	10		2,4	2	1,6	mA	$V_O = 9,5 V; V_I = 0$ or 10 V
	15		8,4	7	5,6	mA	$V_O = 13,5 V; V_I = 0$ or 15 V
Output (source) current HIGH	5	$-I_{OH}$	2,4	2	1,6	mA	$V_O = 2,5 V; V_I = 0$ or 5 V

A.C. CHARACTERISTICS

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	symbol	typ.	max.	typical extrapolation formula
Propagation delays CP \rightarrow O	5	t _{PHL}	110	ns	
	10		60	ns	
	15		45	ns	
HIGH to LOW	5	t _{PLH}	110	ns	
	10		60	ns	
	15		45	ns	
LOW to HIGH	5	t _{THL}	30	ns	
	10		15	ns	
	15		10	ns	
Output transition times HIGH to LOW	5	t _{TLH}	45	ns	
	10		25	ns	
	15		16	ns	

DEVELOPMENT SAMPLE DATA

DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

HEF4060B
MSI

**14-STAGE RIPPLE-CARRY BINARY COUNTER/DIVIDER
AND OSCILLATOR**

The HEF4060B is a 14-stage ripple-carry binary counter/divider and oscillator with three oscillator terminals (RS, R_{TC} and C_{TC}), ten buffered outputs (O₃ to O₉ and O₁₁ to O₁₃) and an overriding asynchronous master reset input (MR). The oscillator configuration allows design of either RC or crystal oscillator circuits. The oscillator may be replaced by an external clock signal at input RS. The counter advances on the negative-going transition of RS. A HIGH level on MR resets the counter (O₃ to O₉ and O₁₁ to O₁₃ = LOW), independent of other input conditions.

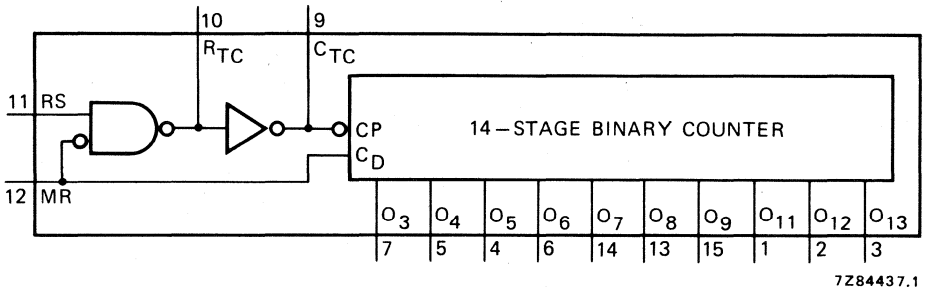
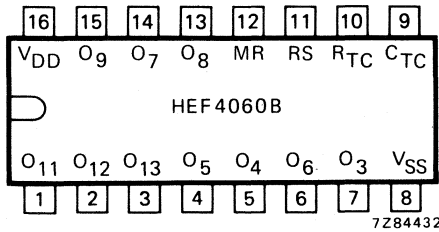


Fig. 1 Functional diagram.



PINNING

- MR master reset
- RS clock input/oscillator pin
- R_{TC} oscillator pin
- C_{TC} external capacitor connection
- O₃ to O₉ } counter outputs
- O₁₁ to O₁₃ }

Fig. 2 Pinning diagram.

- HEF4060BP : 16-lead DIL; plastic (SOT-38Z).
- HEF4060BD : 16-lead DIL; ceramic (SOT-74).
- HEF4060BT : 16-lead flat pack; plastic (SO-16; SOT-109A).

FAMILY DATA

I_{DD} LIMITS category MSI

see Family Specifications

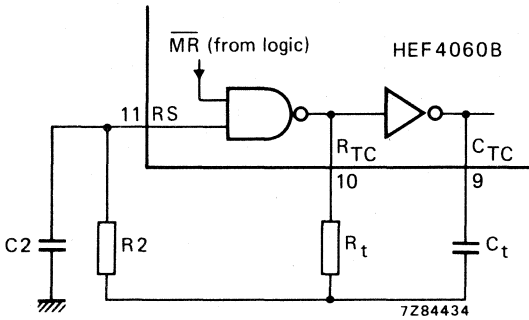
A.C. CHARACTERISTICS

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

DEVELOPMENT SAMPLE DATA

	V_{DD} V	symbol	min.	typ.	max.	typical extrapolation formula
Propagation delays						
RS \rightarrow O ₃	5			480		ns
HIGH to LOW	10	t _{PHL}		260		ns
	15			160		ns
	5			480		ns
LOW to HIGH	10	t _{PLH}		260		ns
	15			160		ns
O _n \rightarrow O _{n+1}	5			120		ns
HIGH to LOW	10	t _{PHL}		65		ns
	15			40		ns
	5			120		ns
LOW to HIGH	10	t _{PLH}		65		ns
	15			40		ns
MR \rightarrow O _n	5			180		ns
HIGH to LOW	10	t _{PHL}		100		ns
	15			70		ns
Output transition times	5			60	120	ns
HIGH to LOW	10	t _{THL}		30	60	ns
	15			20	40	ns
	5			60	120	ns
LOW to HIGH	10	t _{TLH}		30	60	ns
	15			20	40	ns
Minimum clock pulse width input RS	5			100		ns
HIGH	10	t _{WRSH}		60		ns
	15			40		ns
Minimum MR pulse width; HIGH	5			100		ns
	10	t _{WMRH}		60		ns
	15			40		ns
Maximum clock pulse frequency input RS	5			6		MHz
	10	f _{max}		12		MHz
	15			16		MHz

RC oscillator



Typical formula for oscillator frequency:

$$f_{osc} = \frac{1}{2,3 \times R_t \times C_t}$$

Fig. 4 External component connection for RC oscillator.

Timing component limitations

The oscillator frequency is mainly determined by $R_t C_t$, provided $R_t \ll R_2$ and $R_2 C_2 \ll R_t C_t$. The function of R_2 is to minimize the influence of the forward voltage across the input protection diodes on the frequency. The stray capacitance C_2 should be kept as small as possible. In consideration of accuracy, C_t must be larger than the inherent stray capacitance. R_t must be larger than the LOCMOS 'ON' resistance in series with it, which typically is 500Ω at $V_{DD} = 5 V$, 300Ω at $V_{DD} = 10 V$ and 200Ω at $V_{DD} = 15 V$.

The recommended values for these components to maintain agreement with the typical oscillation formula are:

- $C_t \geq 100 \text{ pF}$, up to any practical value,
- $10 \text{ k}\Omega \leq R_t \leq 1 \text{ M}\Omega$.

Typical crystal oscillator circuit

In Fig. 5, R_2 is the power limiting resistor. For starting and maintaining oscillation a minimum transconductance is necessary.

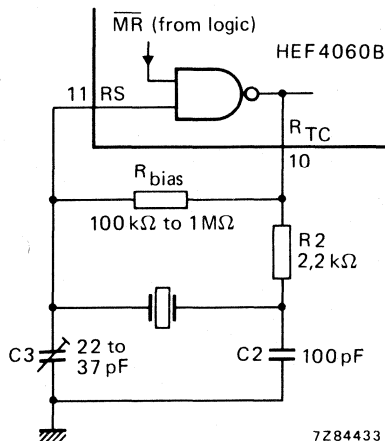


Fig. 5 External component connection for crystal oscillator.

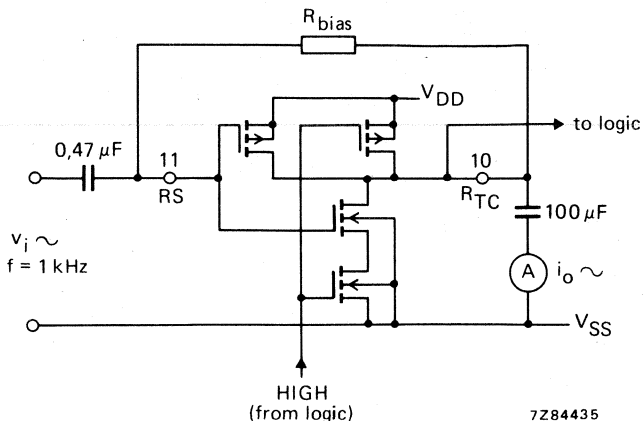


Fig. 6 Test set-up for measuring forward transconductance $g_{fs} = di_o/dv_i$ at v_o is constant (see also graph Fig. 7).

DEVELOPMENT SAMPLE DATA

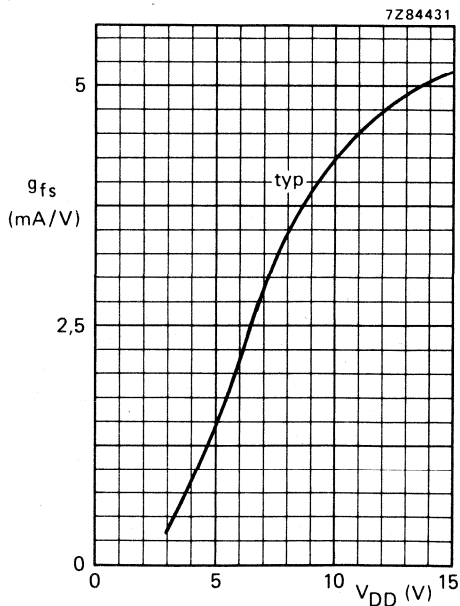


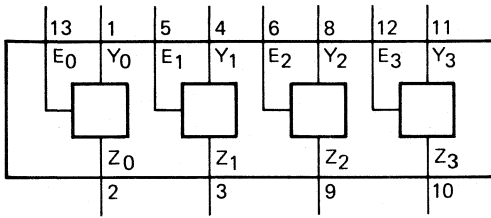
Fig. 7 Typical forward transconductance g_{fs} as a function of the supply voltage for the gate input RS and output R_{TC} (see Fig. 6) at $T_{amb} = 25\text{ }^{\circ}\text{C}$.

QUADRUPLE BILATERAL SWITCHES



The HEF4066B has four independent bilateral analogue switches (transmission gates). Each switch has two input/output terminals (Y/Z) and an active HIGH enable input (E). When E is connected to V_{DD} a low impedance bidirectional path between Y and Z is established (ON condition). When E is connected to V_{SS} the switch is disabled and a high impedance between Y and Z is established (OFF condition).

The HEF4066B is pin compatible with the HEF4016B but exhibits a much lower ON resistance. In addition the ON resistance is relatively constant over the full input signal range.



7Z69571.2

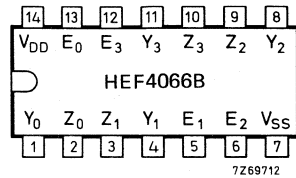
Fig. 1 Functional diagram.

PINNING

E_0 to E_3 enable inputs

Y_0 to Y_3 input/output terminals

Z_0 to Z_3 input/output terminals



7Z69712

Fig. 2 Pinning diagram.

HEF4066BP: 14-lead DIL; plastic (SOT-27S, T, V).

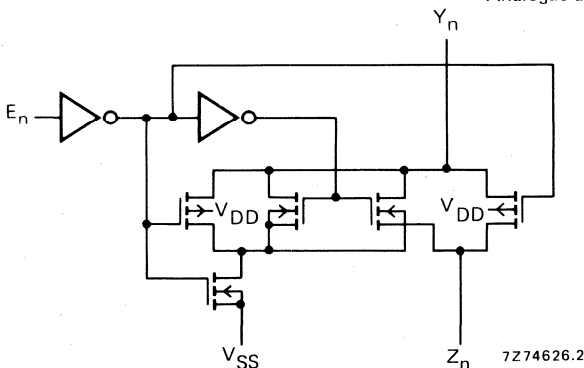
HEF4066BD: 14-lead DIL; ceramic (SOT-73).

HEF4066BT: 14-lead flat pack;
plastic (SO-14; SOT-108A).

APPLICATION INFORMATION

An example of application for the HEF4066B is:

- Analogue and digital switching



7Z74626.2

Fig. 3 Schematic diagram (one switch).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Power dissipation per switch

P max. 100 mW

For other RATINGS see Family Specifications

D.C. CHARACTERISTICS

T_{amb} = 25 °C

	V _{DD} V	symbol	min.	typ.	max.	conditions
ON resistance	5	R _{ON}	—	350	2500	} E _n at V _{DD} V _{is} = V _{SS} to V _{DD} see Fig. 4
	10		—	80	245	
	15		—	60	175	
ON resistance	5	R _{ON}	—	115	340	} E _n at V _{DD} V _{is} = V _{SS} see Fig. 4
	10		—	50	160	
	15		—	40	115	
ON resistance	5	R _{ON}	—	120	365	} E _n at V _{DD} V _{is} = V _{DD} see Fig. 4
	10		—	65	200	
	15		—	50	155	
'Δ' ON resistance between any two channels	5	ΔR _{ON}	—	25	—	} E _n at V _{DD} V _{is} = V _{SS} to V _{DD} see Fig. 4
	10		—	10	—	
	15		—	5	—	
OFF state leakage current, any channel OFF	5	I _{OZ}	—	—	—	} E _n at V _{SS}
	10		—	—	nA	
	15		—	—	200	
E _n input voltage LOW	5	V _{IL}	1	2,25	—	} I _{is} = 10 μA see Fig. 9
	10		2	4,50	—	
	15		2	6,75	—	

	V _{DD} V	symbol	T _{amb} (°C)			conditions
			-40 max.	+25 max.	+85 max.	
Quiescent device current	5	I _{DD}	1,0	1,0	7,5	} V _{SS} = 0; all valid input combinations; V _I = V _{SS} or V _{DD}
	10		2,0	2,0	15,0	
	15		4,0	4,0	30,0	
Input leakage current at E _n	15	± I _{IN}	—	300	1000	E _n at V _{SS} or V _{DD}

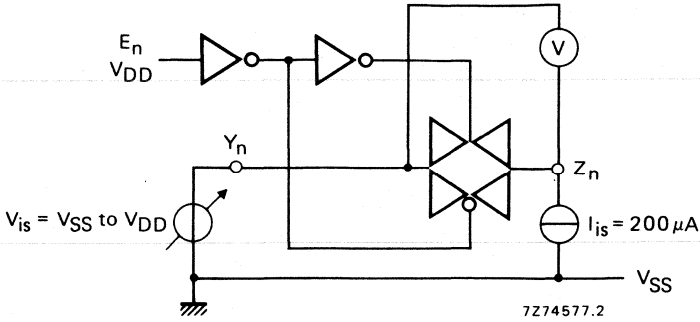


Fig. 4 Test set-up for measuring R_{ON} .

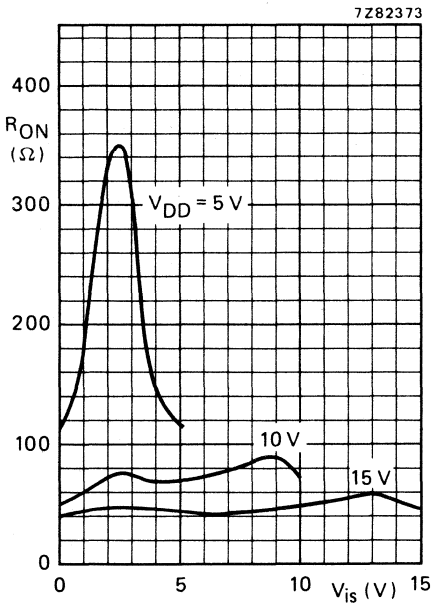


Fig. 5 Typical R_{ON} as a function of input voltage.

E_n at V_{DD}
 $I_{is} = 200 \mu A$
 $V_{SS} = 0 V$

NOTE

To avoid drawing V_{DD} current out of terminal Z, when switch current flows into terminals Y, the voltage drop across the bidirectional switch must not exceed 0,4 V. If the switch current flows into terminal Z, no V_{DD} current will flow out of terminals Y, in this case there is no limit for the voltage drop across the switch, but the voltages at Y and Z may not exceed V_{DD} or V_{SS} .

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ≤ 20 ns

	V _{DD} V	symbol	typ.	max.		
Propagation delays V _{is} → V _{os} HIGH to LOW	5	t _{PHL}	10	20	ns	} note 1
	10		5	10	ns	
	15		5	10	ns	
LOW to HIGH	5	t _{PLH}	10	20	ns	} note 1
	10		5	10	ns	
	15		5	10	ns	
Output disable times E _n → V _{os} HIGH	5	t _{PHZ}	80	160	ns	} note 2
	10		65	130	ns	
	15		60	120	ns	
LOW	5	t _{PLZ}	80	160	ns	} note 2
	10		70	140	ns	
	15		70	140	ns	
Output enable times E _n → V _{os} HIGH	5	t _{PZH}	40	80	ns	} note 2
	10		20	40	ns	
	15		15	30	ns	
LOW	5	t _{PZL}	45	90	ns	} note 2
	10		20	40	ns	
	15		15	30	ns	
Distortion, sine-wave response	5		0,25		%	} note 3
	10		0,04		%	
	15		0,04		%	
Crosstalk between any two channels	5		—		MHz	} note 4
	10		1		MHz	
	15		—		MHz	
Crosstalk; enable input to output	5		—		mV	} note 5
	10		50		mV	
	15		—		mV	
OFF-state feed-through	5		—		MHz	} note 6
	10		1		MHz	
	15		—		MHz	
ON-state frequency response	5		—		MHz	} note 7
	10		90		MHz	
	15		—		MHz	
	V _{DD} V	typical formula for P (μW)			where	
Dynamic power dissipation per package (P)	5	800 f _i + Σ(f _o C _L) × V _{DD} ²			f _i = input freq. (MHz)	
	10	3 500 f _i + Σ(f _o C _L) × V _{DD} ²			f _o = output freq. (MHz)	
	15	10 100 f _i + Σ(f _o C _L) × V _{DD} ²			C _L = load capacitance (pF)	
					Σ(f _o C _L) = sum of outputs	
					V _{DD} = supply voltage (V)	

NOTES

V_{is} is the input voltage at a Y or Z terminal, whichever is assigned as input.

V_{os} is the output voltage at a Y or Z terminal, whichever is assigned as output.

1. $R_L = 10\text{ k}\Omega$ to V_{SS} ; $C_L = 50\text{ pF}$ to V_{SS} ; $E_n = V_{DD}$; $V_{is} = V_{DD}$ (square-wave); see Figs 6 and 10.
2. $R_L = 10\text{ k}\Omega$; $C_L = 50\text{ pF}$ to V_{SS} ; $E_n = V_{DD}$ (square-wave);
 $V_{is} = V_{DD}$ and R_L to V_{SS} for t_{PHZ} and t_{PZH} ;
 $V_{is} = V_{SS}$ and R_L to V_{DD} for t_{PLZ} and t_{PZL} ; see Figs 6 and 11.
3. $R_L = 10\text{ k}\Omega$; $C_L = 15\text{ pF}$; $E_n = V_{DD}$; $V_{is} = \frac{1}{2} V_{DD(p-p)}$ (sine-wave, symmetrical about $\frac{1}{2} V_{DD}$);
 $f_{is} = 1\text{ kHz}$; see Fig. 7.
4. $R_L = 1\text{ k}\Omega$; $V_{is} = \frac{1}{2} V_{DD(p-p)}$ (sine-wave, symmetrical about $\frac{1}{2} V_{DD}$);
 $20 \log \frac{V_{os(B)}}{V_{is(A)}} = -50\text{ dB}$; $E_n(A) = V_{SS}$; $E_n(B) = V_{DD}$; see Fig. 8.
5. $R_L = 10\text{ k}\Omega$ to V_{SS} ; $C_L = 15\text{ pF}$ to V_{SS} ; $E_n = V_{DD}$ (square-wave); crosstalk is $|V_{os}|$ (peak value);
 see Fig. 6.
6. $R_L = 1\text{ k}\Omega$; $C_L = 5\text{ pF}$; $E_n = V_{SS}$; $V_{is} = \frac{1}{2} V_{DD(p-p)}$ (sine-wave, symmetrical about $\frac{1}{2} V_{DD}$);
 $20 \log \frac{V_{os}}{V_{is}} = -50\text{ dB}$; see Fig. 7.
7. $R_L = 1\text{ k}\Omega$; $C_L = 5\text{ pF}$; $E_n = V_{DD}$; $V_{is} = \frac{1}{2} V_{DD(p-p)}$ (sine-wave, symmetrical about $\frac{1}{2} V_{DD}$);
 $20 \log \frac{V_{os}}{V_{is}} = -3\text{ dB}$; see Fig. 7.

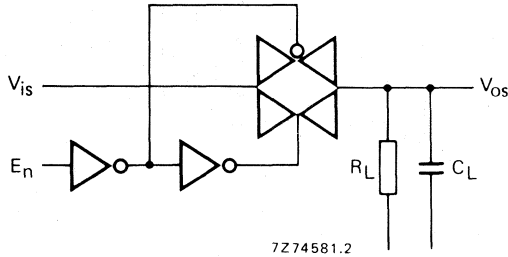


Fig. 6.

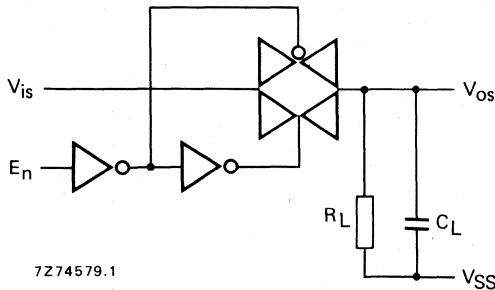


Fig. 7.

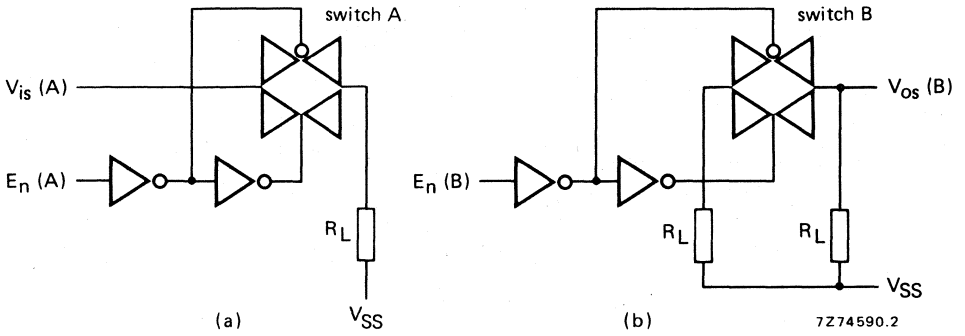


Fig. 8.

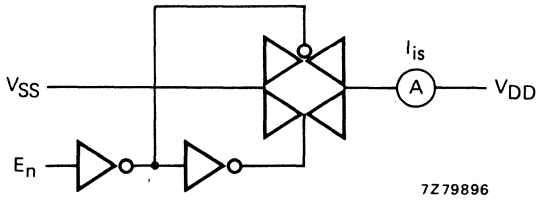


Fig. 9.

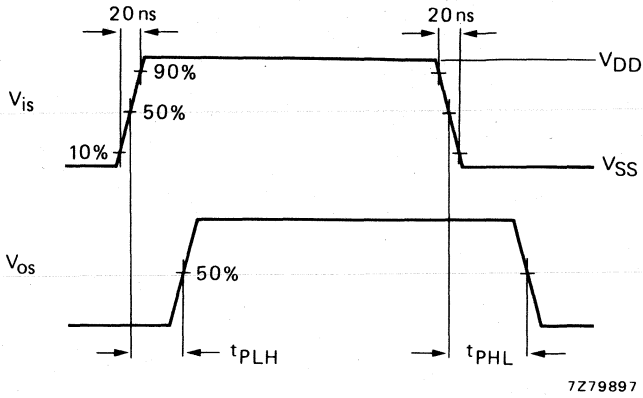
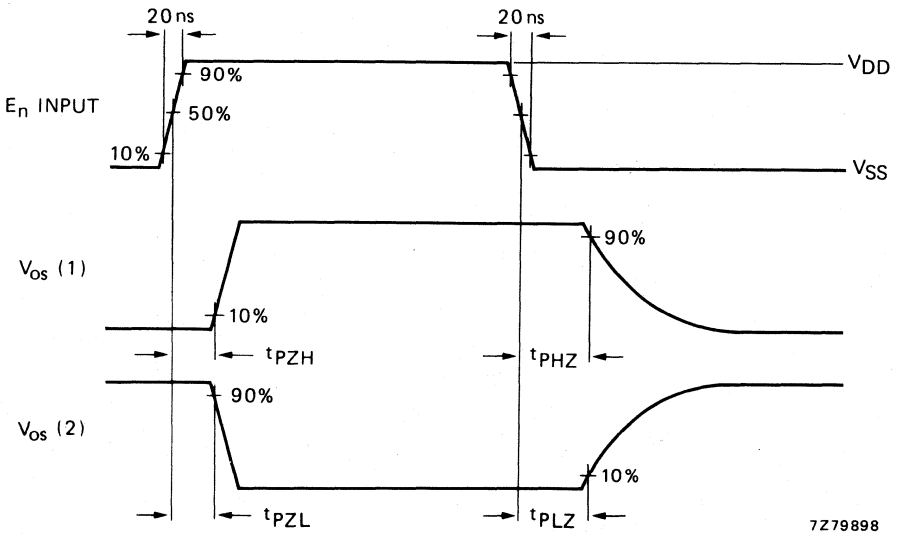


Fig. 10 Waveforms showing propagation delays from V_{is} to V_{os} .



(1) V_{is} at V_{DD} ; (2) V_{is} at V_{SS} .

Fig. 11 Waveforms showing output disable and enable times.

16-CHANNEL ANALOGUE MULTIPLEXER/DEMULTIPLEXER



The HEF4067B is a 16-channel analogue multiplexer/demultiplexer with four address inputs (A_0 to A_3), an active LOW enable input (\bar{E}), sixteen independent inputs/outputs (Y_0 to Y_{15}) and a common input/output (Z).

The device contains sixteen bidirectional analogue switches, each with one side connected to an independent input/output (Y_0 to Y_{15}) and the other side connected to the common input/output (Z).

With \bar{E} LOW, one of the sixteen switches is selected (low impedance ON-state) by A_0 to A_3 . All unselected switches are in the high impedance OFF-state. With \bar{E} HIGH all switches are in the high impedance OFF-state, independent of A_0 to A_3 .

The analogue inputs/outputs (Y_0 to Y_{15} and Z) can swing between V_{DD} as a positive limit and V_{SS} as a negative limit. V_{DD} to V_{SS} may not exceed 15 V.

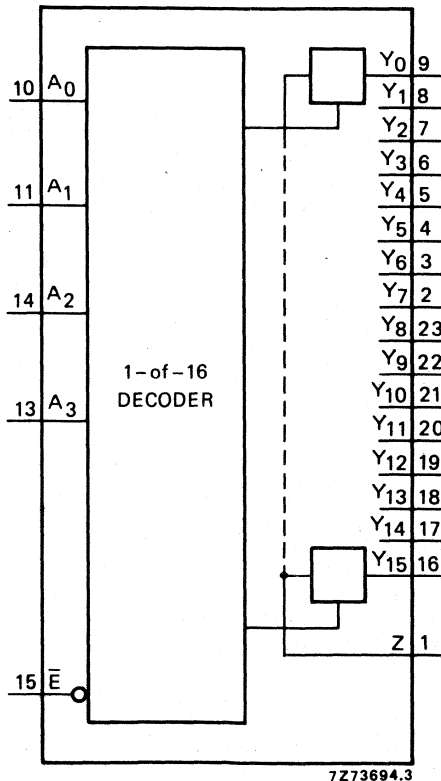


Fig. 1 Functional diagram.

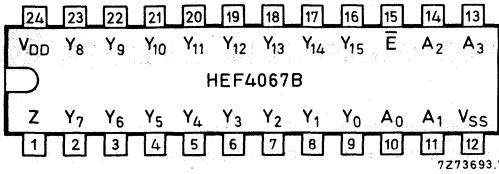
FAMILY DATA

I_{DD} LIMITS category MSI

see Family Specifications

HEF4067B

MSI



HEF4067BP: 24-lead DIL; plastic (SOT-101A).
 HEF4067BD: 24-lead DIL; ceramic (SOT-94).

Fig. 2 Pinning diagram.

PINNING

- Y₀ to Y₁₅ independent inputs/outputs
- A₀ to A₃ address inputs
- E enable input (active LOW)
- Z common input/output

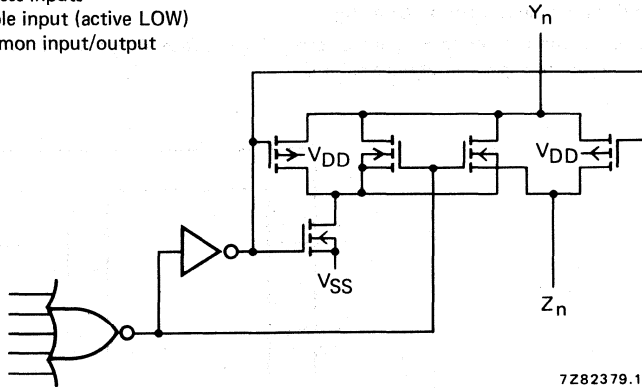


Fig. 3 Schematic diagram (one switch).

7Z82379.1

FUNCTION TABLE

inputs					channel ON
E-bar	A ₃	A ₂	A ₁	A ₀	
L	L	L	L	L	Y ₀ -Z
L	L	L	L	H	Y ₁ -Z
L	L	L	H	L	Y ₂ -Z
L	L	L	H	H	Y ₃ -Z
L	L	H	L	L	Y ₄ -Z
L	L	H	L	H	Y ₅ -Z
L	L	H	H	L	Y ₆ -Z
L	L	H	H	H	Y ₇ -Z
L	H	L	L	L	Y ₈ -Z
L	H	L	L	H	Y ₉ -Z
L	H	L	H	L	Y ₁₀ -Z
L	H	L	H	H	Y ₁₁ -Z
L	H	H	L	L	Y ₁₂ -Z
L	H	H	L	H	Y ₁₃ -Z
L	H	H	H	L	Y ₁₄ -Z
L	H	H	H	H	Y ₁₅ -Z
H	X	X	X	X	none

H = HIGH state (the more positive voltage)
 L = LOW state (the less positive voltage)
 X = state is immaterial

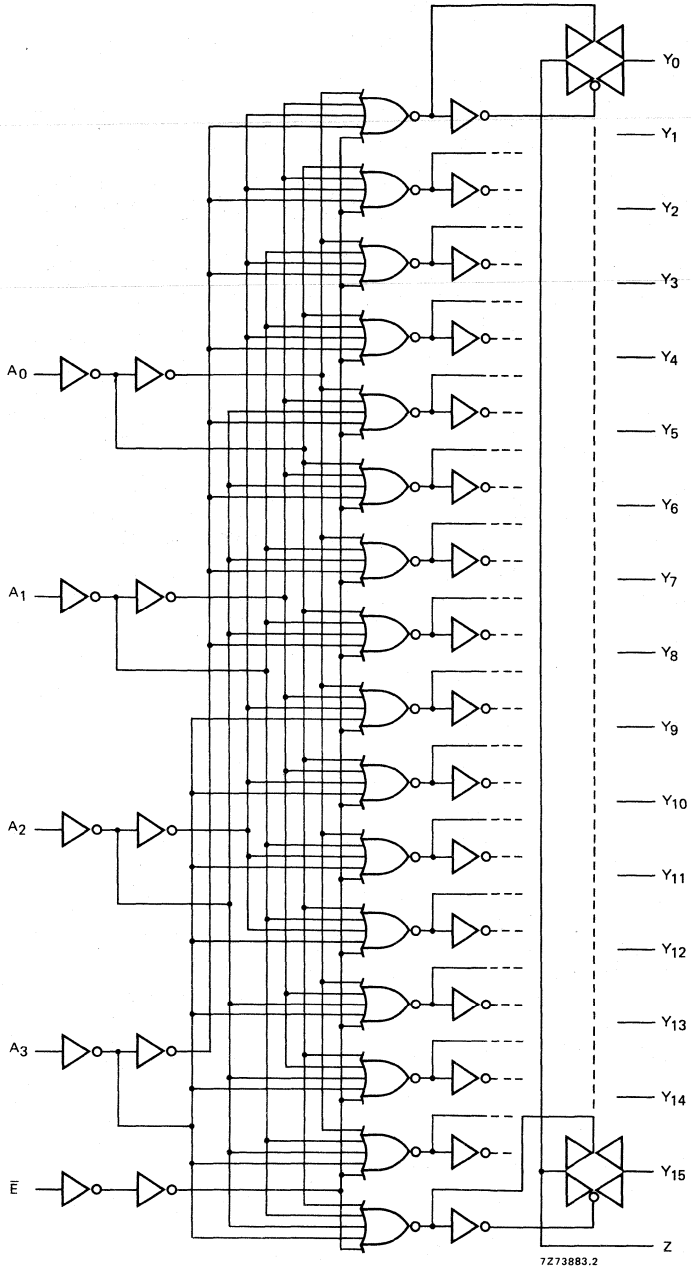


Fig. 4 Logic diagram.

D.C. CHARACTERISTICS

 $T_{amb} = 25\text{ }^{\circ}\text{C}$

	V_{DD} V	symbol	typ.	max.	conditions
ON resistance	5	R_{ON}	350	2500 Ω	} $V_{is} = V_{SS}$ to V_{DD} see Fig. 5
	10		80	245 Ω	
	15		60	175 Ω	
ON resistance	5	R_{ON}	115	340 Ω	} $V_{is} = V_{SS}$ see Fig. 5
	10		50	160 Ω	
	15		40	115 Ω	
ON resistance	5	R_{ON}	120	365 Ω	} $V_{is} = V_{DD}$ see Fig. 5
	10		65	200 Ω	
	15		50	155 Ω	
' Δ ' ON resistance between any two channels	5	ΔR_{ON}	25	— Ω	} $V_{is} = V_{SS}$ to V_{DD} see Fig. 5
	10		10	— Ω	
	15		5	— Ω	
OFF-state leakage current, all channels OFF	5	I_{OZZ}	—	— nA	} \bar{E} at V_{DD}
	10		—	— nA	
	15		—	1000 nA	
OFF-state leakage current, any channel	5	I_{OZY}	—	— nA	} \bar{E} at V_{SS}
	10		—	— nA	
	15		—	200 nA	

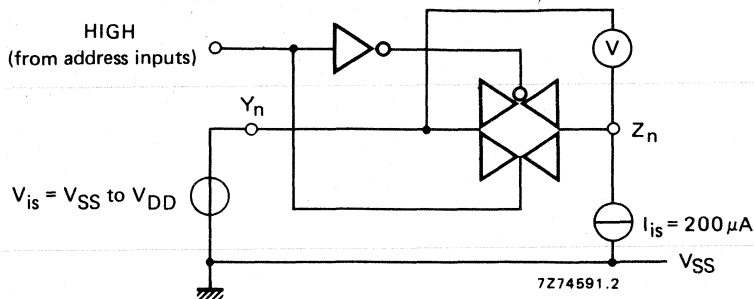


Fig. 5 Test set-up for measuring R_{ON} .

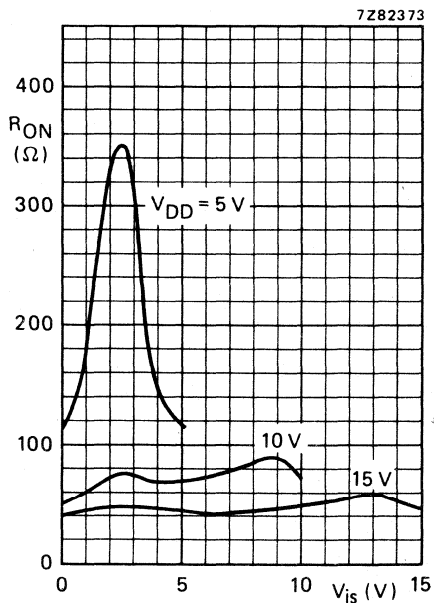


Fig. 6 Typical R_{ON} as a function of input voltage.

$I_{is} = 200 \mu A$
 $V_{SS} = 0 V$

NOTE

To avoid drawing V_{DD} current out of terminal Z, when switch current flows into terminals Y, the voltage drop across the bidirectional switch must not exceed 0,4 V. If the switch current flows into terminal Z, no V_{DD} current will flow out of terminals Y, in this case there is no limit for the voltage drop across the switch, but the voltages at Y and Z may not exceed V_{DD} or V_{SS} .

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ≤ 20 ns

	V _{DD} V	typical formula for P (μW)	where f _i = input freq. (MHz) f _o = output freq. (MHz) C _L = load capacitance (pF) Σ(f _o C _L) = sum of outputs V _{DD} = supply voltage (V)
Dynamic power dissipation per package (P)	5	1 100 f _i + Σ(f _o C _L) × V _{DD} ²	
	10	5 000 f _i + Σ(f _o C _L) × V _{DD} ²	
	15	13 300 f _i + Σ(f _o C _L) × V _{DD} ²	

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ≤ 20 ns

	V _{DD} V	symbol	typ.	max.		
Propagation delays V _{is} → V _{os} HIGH to LOW	5	t _{PHL}	30	60	ns	} note 1
	10		15	25	ns	
	15		10	20	ns	
LOW to HIGH	5	t _{PLH}	25	50	ns	} note 1
	10		10	20	ns	
	15		10	20	ns	
A _n → V _{os} HIGH to LOW	5	t _{PHL}	190	380	ns	} note 2
	10		70	145	ns	
	15		50	100	ns	
LOW to HIGH	5	t _{PLH}	175	345	ns	} note 2
	10		70	140	ns	
	15		50	100	ns	
Output disable times E _n → V _{os} HIGH	5	t _{PHZ}	195	385	ns	} note 3
	10		140	280	ns	
	15		130	260	ns	
LOW	5	t _{PLZ}	215	435	ns	} note 3
	10		180	355	ns	
	15		170	340	ns	
Output enable times E _n → V _{os} HIGH	5	t _{PZH}	155	315	ns	} note 3
	10		70	135	ns	
	15		50	100	ns	
LOW	5	t _{PZL}	170	340	ns	} note 3
	10		70	140	ns	
	15		50	100	ns	

A.C. CHARACTERISTICS

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^\circ\text{C}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	symbol	typ.	max.	
Distortion, sine-wave response	5		0,25	%	} note 4
	10		0,04	%	
	15		0,04	%	
Crosstalk between any two channels	5		—	MHz	} note 5
	10		1	MHz	
	15		—	MHz	
Crosstalk; enable or address input to output	5		—	mV	} note 6
	10		50	mV	
	15		—	mV	
OFF-state feed-through	5		—	MHz	} note 7
	10		1	MHz	
	15		—	MHz	
ON-state frequency response	5		13	MHz	} note 8
	10		40	MHz	
	15		70	MHz	

NOTES

V_{is} is the input voltage at a Y or Z terminal, whichever is assigned as input.

V_{os} is the output voltage at a Y or Z terminal, whichever is assigned as output.

- $R_L = 10\text{ k}\Omega$ to V_{SS} ; $C_L = 50\text{ pF}$ to V_{SS} ; $\bar{E} = V_{SS}$; $V_{is} = V_{DD}$ (square-wave); see Fig. 7.
- $R_L = 10\text{ k}\Omega$; $C_L = 50\text{ pF}$ to V_{SS} ; $\bar{E} = V_{SS}$; $A_n = V_{DD}$ (square-wave); $V_{is} = V_{DD}$ and R_L to V_{SS} for t_{PLH} ; $V_{is} = V_{SS}$ and R_L to V_{DD} for t_{PHL} ; see Fig. 7.
- $R_L = 10\text{ k}\Omega$; $C_L = 50\text{ pF}$ to V_{SS} ; $\bar{E} = V_{DD}$ (square-wave); $V_{is} = V_{DD}$ and R_L to V_{SS} for t_{PHZ} and t_{PZH} ; $V_{is} = V_{SS}$ and R_L to V_{DD} for t_{PLZ} and t_{PZL} ; see Fig. 7.
- $R_L = 10\text{ k}\Omega$; $C_L = 15\text{ pF}$; channel ON; $V_{is} = \frac{1}{2} V_{DD(p-p)}$ (sine-wave, symmetrical about $\frac{1}{2} V_{DD}$); $f_{is} = 1\text{ kHz}$; see Fig. 8.
- $R_L = 1\text{ k}\Omega$; $V_{is} = \frac{1}{2} V_{DD(p-p)}$ (sine-wave, symmetrical about $\frac{1}{2} V_{DD}$); $20 \log \frac{V_{os}}{V_{is}} = -40\text{ dB}$; see Fig. 9.
- $R_L = 10\text{ k}\Omega$ to V_{SS} ; $C_L = 15\text{ pF}$ to V_{SS} ; \bar{E} or $A_n = V_{DD}$ (square-wave); crosstalk is $|V_{os}|$ (peak value); see Fig. 7.
- $R_L = 1\text{ k}\Omega$; $C_L = 5\text{ pF}$; channel OFF; $V_{is} = \frac{1}{2} V_{DD(p-p)}$ (sine-wave, symmetrical about $\frac{1}{2} V_{DD}$); $20 \log \frac{V_{os}}{V_{is}} = -40\text{ dB}$; see Fig. 8.
- $R_L = 1\text{ k}\Omega$; $C_L = 5\text{ pF}$; channel ON; $V_{is} = \frac{1}{2} V_{DD(p-p)}$ (sine-wave, symmetrical about $\frac{1}{2} V_{DD}$); $20 \log \frac{V_{os}}{V_{is}} = -3\text{ dB}$; see Fig. 8.

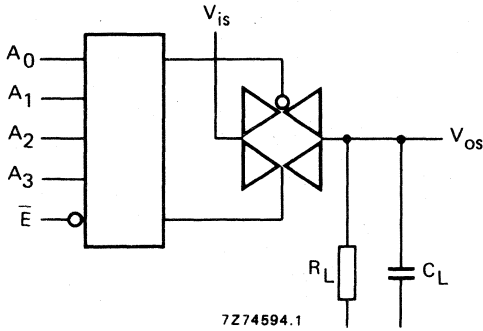


Fig. 7.

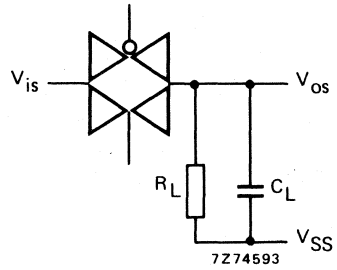


Fig. 8.

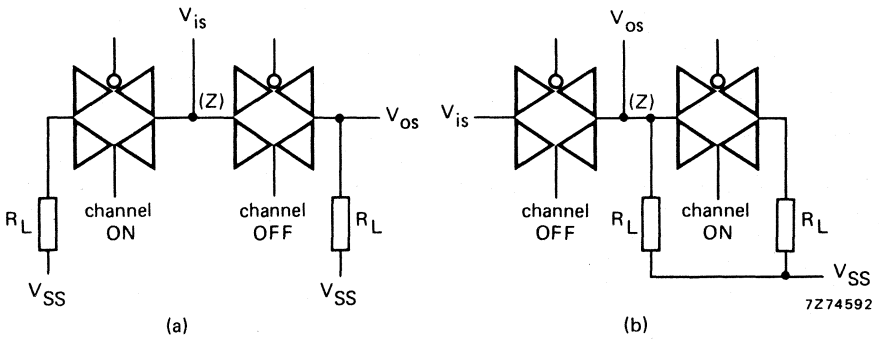


Fig. 9.

APPLICATION INFORMATION

Some examples of applications for the HEF4067B are:

- Analogue multiplexing and demultiplexing.
- Digital multiplexing and demultiplexing.
- Signal gating.

NOTE

If break before make is needed, then it is necessary to use the enable input.

8-INPUT NAND GATE



The HEF4068B provides the 8-input NAND function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

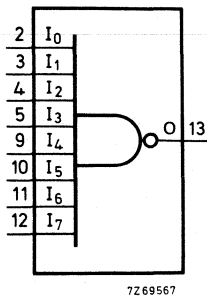


Fig. 1 Functional diagram.

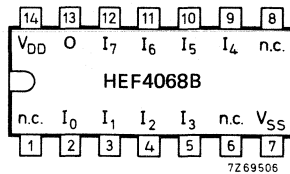


Fig. 2 Pinning diagram.

HEF4068BP: 14-lead DIL: plastic (SOT-27S, T, V).

HEF4068BD: 14-lead DIL: ceramic (SOT-73).

HEF4068BT: 14-lead flat pack; plastic (SO-14; SOT-108A).

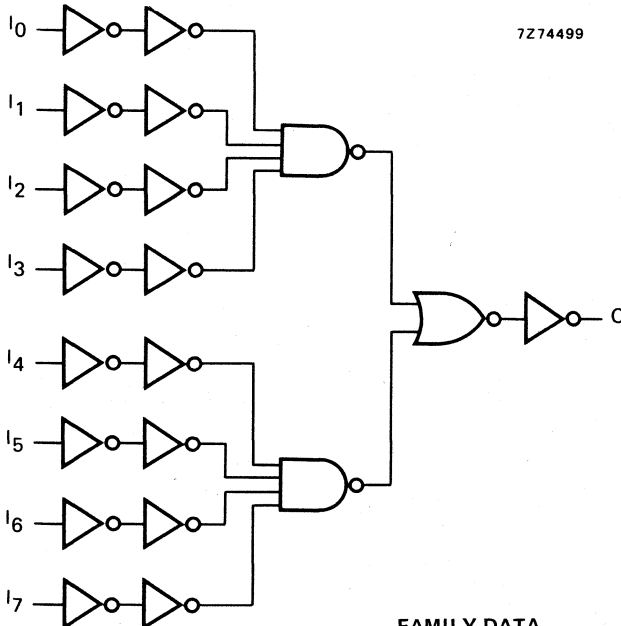


Fig. 3 Logic diagram.

FAMILY DATA

I_{DD} LIMITS category GATES

} see Family Specifications

A.C. CHARACTERISTICS

 $V_{SS} = 0 \text{ V}$; $T_{amb} = 25 \text{ }^\circ\text{C}$; $C_L = 50 \text{ pF}$; input transition times $\leq 20 \text{ ns}$

	V_{DD} V	symbol	typ.	max.		typical extrapolation formula
Propagation delays $I_n \rightarrow 0$ HIGH to LOW	5	t_{PHL}	95	195	ns	$68 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
	10		40	85	ns	$29 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
	15		30	65	ns	$22 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
LOW to HIGH	5	t_{PLH}	80	165	ns	$53 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
	10		35	70	ns	$24 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
	15		30	60	ns	$22 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
Output transition times HIGH to LOW	5	t_{THL}	60	120	ns	$10 \text{ ns} + (1,0 \text{ ns/pF}) C_L$
	10		30	60	ns	$9 \text{ ns} + (0,42 \text{ ns/pF}) C_L$
	15		20	40	ns	$6 \text{ ns} + (0,28 \text{ ns/pF}) C_L$
LOW to HIGH	5	t_{TLH}	60	120	ns	$10 \text{ ns} + (1,0 \text{ ns/pF}) C_L$
	10		30	60	ns	$9 \text{ ns} + (0,42 \text{ ns/pF}) C_L$
	15		20	40	ns	$6 \text{ ns} + (0,28 \text{ ns/pF}) C_L$

	V_{DD} V	typical formula for P (μW)	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
Dynamic power dissipation per package (P)	5	$700 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	10	$2900 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$7200 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

HEX INVERTER



The HEF4069UB is a general purpose hex inverter. Each of the six inverters is a single stage.

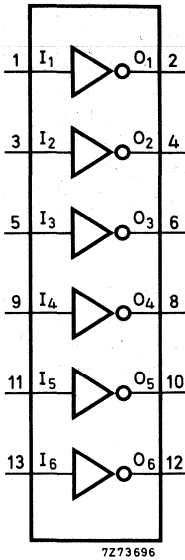


Fig. 1 Functional diagram.

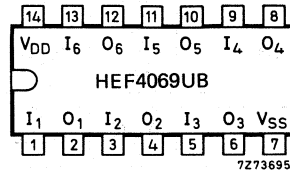


Fig. 2 Pinning diagram.

HEF4069UBP : 14-lead DIL; plastic (SOT-27S, T, V).

HEF4069UBD : 14-lead DIL; ceramic (SOT-73).

HEF4069UBT : 14-lead flat pack; plastic (SO-14; SOT-108A).

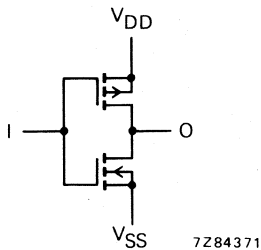


Fig. 3 Schematic diagram (one inverter).

FAMILY DATA

I_{DD} LIMITS category GATES

} see Family Specifications

A.C. CHARACTERISTICS

 $V_{SS} = 0 \text{ V}$; $T_{amb} = 25 \text{ }^\circ\text{C}$; $C_L = 50 \text{ pF}$; input transition times $\leq 20 \text{ ns}$

	V_{DD} V	symbol	typ.	max.	typical extrapolation formula
Propagation delays $I_n \rightarrow O_n$ HIGH to LOW	5	t _{PHL}	45	90 ns	18 ns + (0,55 ns/pF) C _L
	10		20	40 ns	9 ns + (0,23 ns/pF) C _L
	15		15	25 ns	7 ns + (0,16 ns/pF) C _L
LOW to HIGH	5	t _{PLH}	40	80 ns	13 ns + (0,55 ns/pF) C _L
	10		20	40 ns	9 ns + (0,23 ns/pF) C _L
	15		15	30 ns	7 ns + (0,16 ns/pF) C _L
Output transition times HIGH to LOW	5	t _{THL}	60	120 ns	10 ns + (1,0 ns/pF) C _L
	10		30	60 ns	9 ns + (0,42 ns/pF) C _L
	15		20	40 ns	6 ns + (0,28 ns/pF) C _L
LOW to HIGH	5	t _{TLH}	60	120 ns	10 ns + (1,0 ns/pF) C _L
	10		30	60 ns	9 ns + (0,42 ns/pF) C _L
	15		20	40 ns	6 ns + (0,28 ns/pF) C _L
	V_{DD} V	typical formula for P (μW)	where		
Dynamic power dissipation per package (P)	5	$600 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f _i = input freq. (MHz)		
	10		f _o = output freq. (MHz)		
	15		C _L = load capacitance (pF)		
			$\Sigma(f_o C_L)$ = sum of outputs		
			V _{DD} = supply voltage (V)		

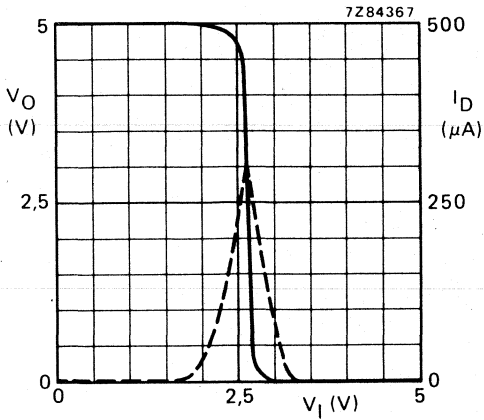


Fig. 4 Typical transfer characteristics;
 — V_O ; - - - I_D (drain current); $I_O = 0$;
 $V_{DD} = 5 \text{ V}$.

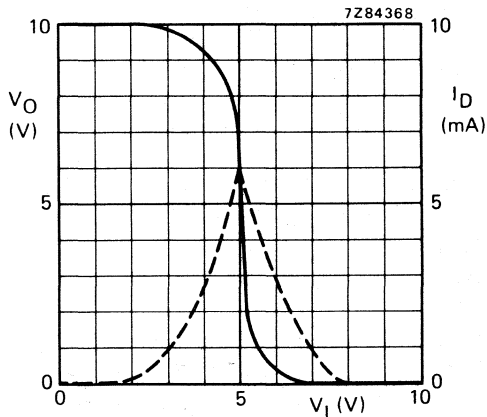


Fig. 5 Typical transfer characteristics;
 — V_O ; - - - I_D (drain current); $I_O = 0$;
 $V_{DD} = 10 \text{ V}$.

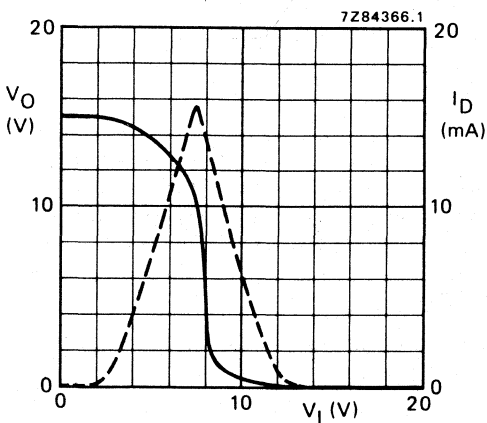
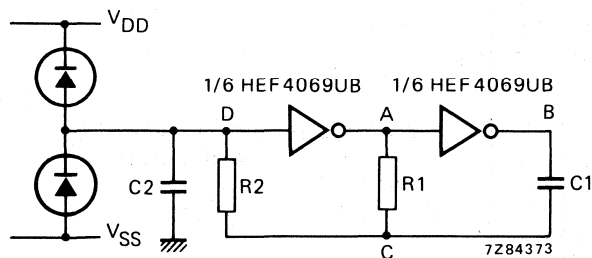


Fig. 6 Typical transfer characteristics;
 — V_O ; - - - I_D (drain current) $I_O = 0$;
 $V_{DD} = 15 \text{ V}$.

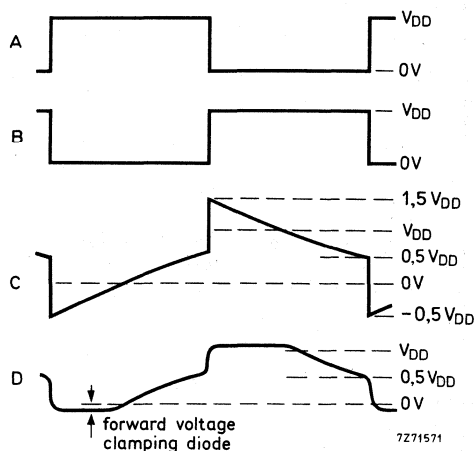
APPLICATION INFORMATION

Some examples of applications for the HEF4069UB are shown below.

In Fig. 7 an astable relaxation oscillator is given. The oscillation frequency is mainly determined by $R1C1$, provided $R1 \ll R2$ and $R2C2 \ll R1C1$.



(a)



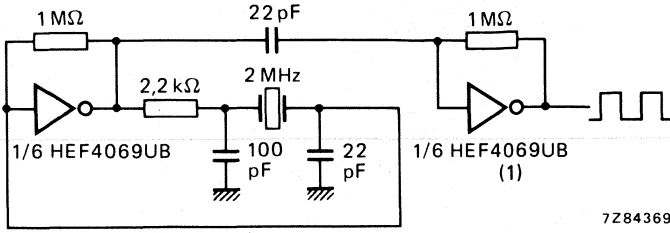
(b)

Fig. 7(a) Astable relaxation oscillator using two HEF4069UB inverters; the diodes may be BAW62; C2 is a parasitic capacitance. (b) Waveforms at the points marked A, B, C and D in the circuit diagram.

The function of R2 is to minimize the influence of the forward voltage across the protection diodes on the frequency; C2 is a stray (parasitic) capacitance. The period T_p is given by $T_p = T_1 + T_2$, in which

$$T_1 = R1C1 \ln \frac{V_{DD} + V_{ST}}{V_{ST}} \quad \text{and} \quad T_2 = R1C1 \ln \frac{2V_{DD} - V_{ST}}{V_{DD} - V_{ST}} \quad \text{where}$$

V_{ST} is the signal threshold level of the inverter. The period is fairly independent of V_{DD} , V_{ST} and temperature. The duty factor, however, is influenced by V_{ST} .



7Z84369

(1) This inverter is added to amplify the oscillator output voltage to a level sufficient to drive other LOCMOS circuits.

Fig. 8 Crystal oscillator for frequencies up to 10 MHz, using two HEF4069UB inverters.

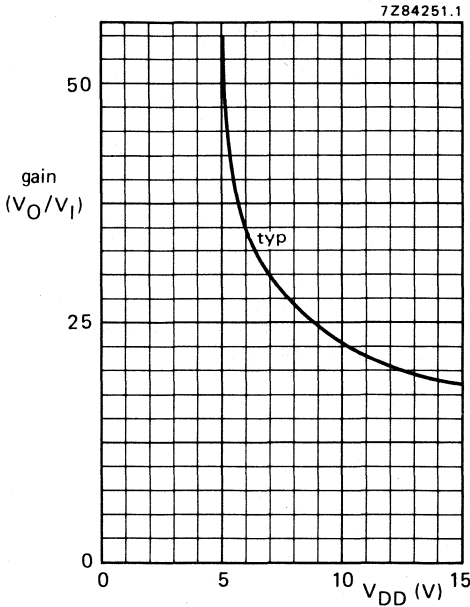


Fig. 9 Voltage gain (V_O/V_I) as a function of supply voltage.

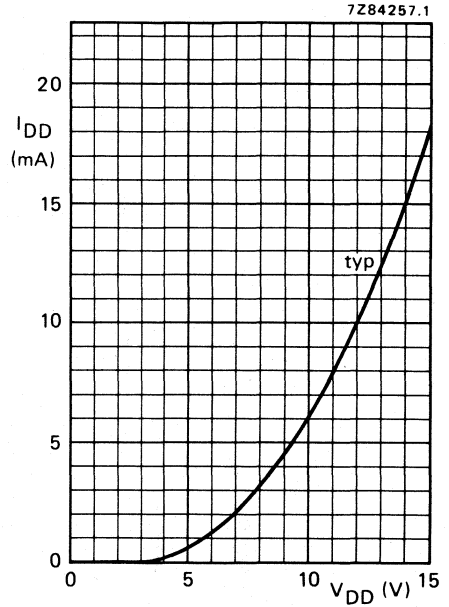
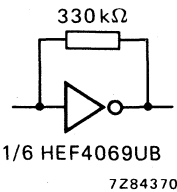


Fig. 10 Supply current as a function of supply voltage.



7Z84370

Fig. 11 Test set-up for measuring graphs of Figs 9 and 10. It is also an example of an analogue amplifier using one HEF4069UB.

APPLICATION INFORMATION (continued)

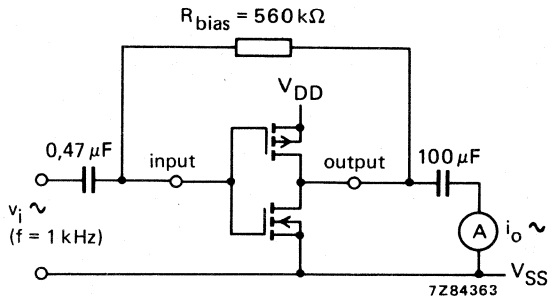


Fig. 12 Test set-up for measuring forward transconductance $g_{fs} = di_o/dv_i$ at v_o is constant (see also graph Fig. 13).

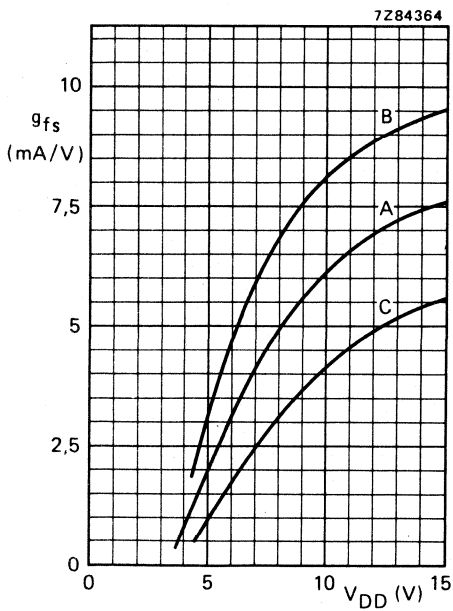


Fig. 13 Typical forward transconductance g_{fs} as a function of the supply voltage at $T_{amb} = 25\text{ }^{\circ}\text{C}$.

Curves in Fig. 13:

- A : average,
- B : average + 2 s,
- C : average - 2 s, in where:
's' is the observed standard deviation.

QUADRUPLE EXCLUSIVE-OR GATE



The HEF4070B provides the positive quadruple exclusive-OR function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

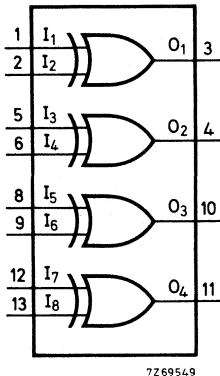


Fig. 1 Functional diagram.

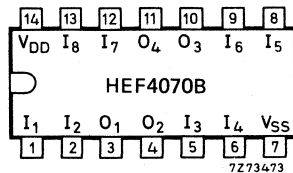


Fig. 2 Pinning diagram.

HEF4070BP: 14-lead DIL; plastic (SOT-27S,T,V).
 HEF4070BD: 14-lead DIL; ceramic (SOT-73).
 HEF4070BT: 14-lead flat pack;
 plastic (SO-14; SOT-108A).

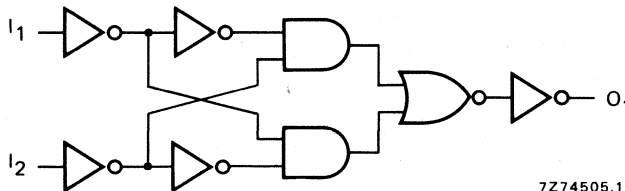


Fig. 3 Logic diagram (one gate).

APPLICATION INFORMATION

Some examples of applications for the HEF4070B are:

- Logical comparators
- Parity checkers and generators

TRUTH TABLE

I ₁	I ₂	O ₁
L	L	L
H	L	H
L	H	H
H	H	L

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

FAMILY DATA

I_{DD} LIMITS category GATES

} see Family Specifications

A.C. CHARACTERISTICS

 $V_{SS} = 0 \text{ V}$; $T_{amb} = 25 \text{ }^\circ\text{C}$; $C_L = 50 \text{ pF}$; input transition times $\leq 20 \text{ ns}$

	V_{DD} V	symbol	typ.	max.		typical extrapolation formula
Propagation delays $I_n \rightarrow O_n$ HIGH to LOW	5	t_{PHL}	85	175	ns	$57 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
	10		35	75	ns	$23 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
	15		30	55	ns	$22 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
LOW to HIGH	5	t_{PLH}	75	150	ns	$47 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
	10		30	65	ns	$19 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
	15		25	50	ns	$17 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
Output transition times HIGH to LOW	5	t_{THL}	60	120	ns	$10 \text{ ns} + (1,0 \text{ ns/pF}) C_L$
	10		30	60	ns	$9 \text{ ns} + (0,42 \text{ ns/pF}) C_L$
	15		20	40	ns	$6 \text{ ns} + (0,28 \text{ ns/pF}) C_L$
LOW to HIGH	5	t_{TLH}	60	120	ns	$10 \text{ ns} + (1,0 \text{ ns/pF}) C_L$
	10		30	60	ns	$9 \text{ ns} + (0,42 \text{ ns/pF}) C_L$
	15		20	40	ns	$6 \text{ ns} + (0,28 \text{ ns/pF}) C_L$

	V_{DD} V	typical formula for P (μW)	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
Dynamic power dissipation per package (P)	5	$1100 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	10	$4900 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$14400 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

QUADRUPLE 2-INPUT OR GATE



The HEF4071B is a positive logic quadruple 2-input OR gate. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

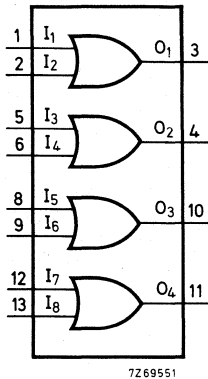


Fig. 1 Functional diagram.

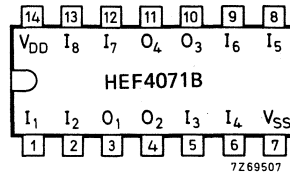
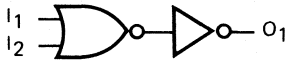


Fig. 2 Pinning diagram.

HEF4071BP: 14-lead DIL; plastic (SOT-27S, T, V).

HEF4071BD: 14-lead DIL; ceramic (SOT-73).

HEF4071BT: 14-lead flat pack; plastic (SO-14; SOT-108A).



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Fig. 3 Logic diagram (one gate).

FAMILY DATA

I_{DD} LIMITS category GATES

} see Family Specifications



A.C. CHARACTERISTICS

 $V_{SS} = 0 \text{ V}; T_{amb} = 25 \text{ }^\circ\text{C}; C_L = 50 \text{ pF};$ input transition times $\leq 20 \text{ ns}$

	V_{DD} V	symbol	typ.	max.		typical extrapolation formula	
Propagation delays $I_n \rightarrow O_n$ HIGH to LOW	5	tPHL	55	115	ns	$28 \text{ ns} + (0,55 \text{ ns/pF}) C_L$	
	10		25	50	ns	$15 \text{ ns} + (0,23 \text{ ns/pF}) C_L$	
	15		20	35	ns	$12 \text{ ns} + (0,16 \text{ ns/pF}) C_L$	
	LOW to HIGH	5	tPLH	45	90	ns	$18 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
		10		20	45	ns	$9 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
		15		15	30	ns	$7 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
Output transition times HIGH to LOW	5	tTHL	60	120	ns	$10 \text{ ns} + (1,0 \text{ ns/pF}) C_L$	
	10		30	60	ns	$9 \text{ ns} + (0,42 \text{ ns/pF}) C_L$	
	15		20	40	ns	$6 \text{ ns} + (0,28 \text{ ns/pF}) C_L$	
	LOW to HIGH	5	tTLH	60	120	ns	$10 \text{ ns} + (1,0 \text{ ns/pF}) C_L$
		10		30	60	ns	$9 \text{ ns} + (0,42 \text{ ns/pF}) C_L$
		15		20	40	ns	$6 \text{ ns} + (0,28 \text{ ns/pF}) C_L$

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$1150 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz)
	10		f_o = output freq. (MHz)
	15		C_L = load capacitance (pF)
			$\Sigma(f_o C_L)$ = sum of outputs
			V_{DD} = supply voltage (V)

DUAL 4-INPUT OR GATE



The HEF4072B provides the positive dual 4-input OR function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

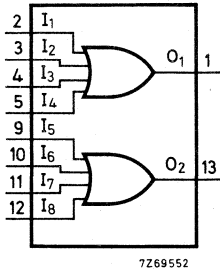


Fig. 1 Functional diagram.

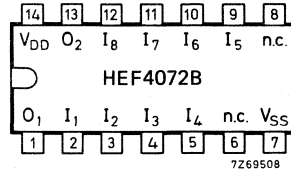


Fig. 2 Pinning diagram.

HEF4072BP: 14-lead DIL; plastic (SOT-27S, T, V).

HEF4072BD: 14-lead DIL; ceramic (SOT-73).

HEF4072BT: 14-lead flat pack; plastic (SO-14; SOT-108A).

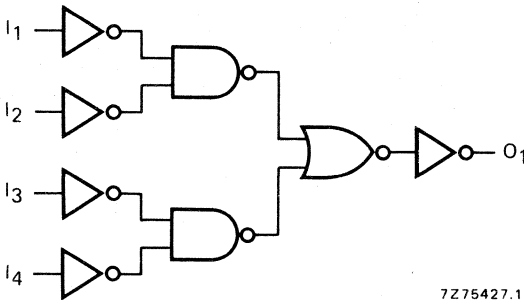


Fig. 3 Logic diagram (one gate).

FAMILY DATA

I_{DD} LIMITS category GATES

} see Family Specifications



A.C. CHARACTERISTICS

 $V_{SS} = 0 \text{ V}$; $T_{amb} = 25 \text{ }^\circ\text{C}$; $C_L = 50 \text{ pF}$; input transition times $\leq 20 \text{ ns}$

	V_{DD} V	symbol	typ.	max.		typical extrapolation formula
Propagation delays $I_n \rightarrow O_n$ HIGH to LOW	5	t _{PHL}	80	155	ns	$53 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
	10		35	70	ns	$24 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
	15		25	55	ns	$17 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
LOW to HIGH	5	t _{PLH}	75	145	ns	$48 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
	10		35	70	ns	$24 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
	15		25	55	ns	$17 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
Output transition times HIGH to LOW	5	t _{THL}	60	120	ns	$10 \text{ ns} + (1,0 \text{ ns/pF}) C_L$
	10		30	60	ns	$9 \text{ ns} + (0,42 \text{ ns/pF}) C_L$
	15		20	40	ns	$6 \text{ ns} + (0,28 \text{ ns/pF}) C_L$
LOW to HIGH	5	t _{TLH}	60	120	ns	$10 \text{ ns} + (1,0 \text{ ns/pF}) C_L$
	10		30	60	ns	$9 \text{ ns} + (0,42 \text{ ns/pF}) C_L$
	15		20	40	ns	$6 \text{ ns} + (0,28 \text{ ns/pF}) C_L$

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$950 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz)
	10	$4500 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_o = output freq. (MHz)
	15	$13\,700 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	C_L = load capacitance (pF)
			$\Sigma(f_o C_L)$ = sum of outputs
			V_{DD} = supply voltage (V)

TRIPLE 3-INPUT AND GATE



The HEF4073B provides the positive triple 3-input AND function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

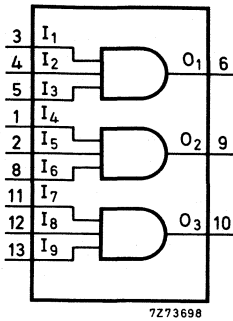


Fig.1 Functional diagram.

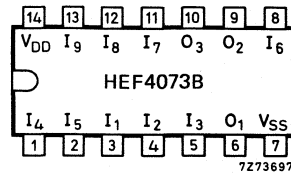


Fig.2 Pinning diagram.

HEF4073BP: 14-lead DIL; plastic (SOT-27 S, T, V).

HEF4073BD: 14-lead DIL; ceramic (SOT-73).

HEF4073BT: 14-lead flat pack; plastic (SO-14; SOT-108A).

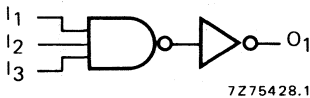


Fig.3 Logic diagram (one gate).

FAMILY DATA

I_{DD} LIMITS category GATES

} see Family Specifications

HEF4073B

gates

A.C. CHARACTERISTICS

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	symbol	typ.	max.		typical extrapolation formula
Propagation delays $I_n \rightarrow O_n$ HIGH to LOW	5	t _{PHL}	55	100	ns	23 ns + (0,55 ns/pF) C _L
	10		25	50	ns	14 ns + (0,23 ns/pF) C _L
	15		20	40	ns	12 ns + (0,16 ns/pF) C _L
LOW to HIGH	5	t _{PLH}	45	90	ns	13 ns + (0,55 ns/pF) C _L
	10		20	40	ns	9 ns + (0,23 ns/pF) C _L
	15		15	30	ns	7 ns + (0,16 ns/pF) C _L
Output transition times HIGH to LOW	5	t _{THL}	60	120	ns	10 ns + (1,0 ns/pF) C _L
	10		30	60	ns	9 ns + (0,42 ns/pF) C _L
	15		20	40	ns	6 ns + (0,28 ns/pF) C _L
LOW to HIGH	5	t _{TLH}	60	120	ns	10 ns + (1,0 ns/pF) C _L
	10		30	60	ns	9 ns + (0,42 ns/pF) C _L
	15		20	40	ns	6 ns + (0,28 ns/pF) C _L

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$600 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz)
	10	$2700 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_o = output freq. (MHz)
	15	$8400 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	C _L = load capacitance (pF)
			$\Sigma(f_o C_L)$ = sum of outputs
			V _{DD} = supply voltage (V)



TRIPLE 3-INPUT OR GATE

The HEF4075B provides the positive triple 3-input OR function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

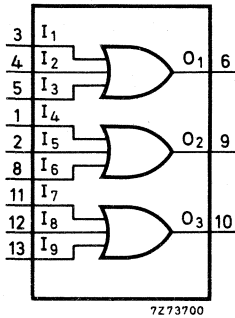


Fig.1 Functional diagram.

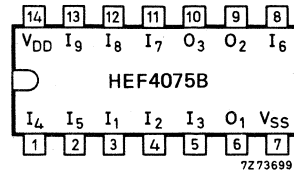


Fig.2 Pinning diagram.

- HEF4075BP : 14-lead DIL; plastic (SOT-27S, T, V).
- HEF4075BD : 14-lead DIL; ceramic (SOT-73).
- HEF4075BT : 14-lead flat pack; plastic (SO-14; SOT-108A).

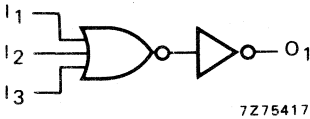


Fig.3 Logic diagram (one gate).

FAMILY DATA

I_{DD} LIMITS category GATES

} see Family Specifications

A.C. CHARACTERISTICS

 $V_{SS} = 0 \text{ V}$; $T_{amb} = 25 \text{ }^\circ\text{C}$; $C_L = 50 \text{ pF}$; input transition times $\leq 20 \text{ ns}$

	V_{DD} V	symbol	typ.	max.		typical extrapolation formula
Propagation delays $I_n \rightarrow O_n$ HIGH to LOW	5	t _{PHL}	65	130	ns	38 ns + (0,55 ns/pF) C _L
	10		30	60	ns	19 ns + (0,23 ns/pF) C _L
	15		20	40	ns	12 ns + (0,16 ns/pF) C _L
LOW to HIGH	5	t _{PLH}	65	130	ns	38 ns + (0,55 ns/pF) C _L
	10		30	60	ns	19 ns + (0,23 ns/pF) C _L
	15		25	50	ns	17 ns + (0,16 ns/pF) C _L
Output transition times HIGH to LOW	5	t _{THL}	60	120	ns	10 ns + (1,0 ns/pF) C _L
	10		30	60	ns	9 ns + (0,42 ns/pF) C _L
	15		20	40	ns	6 ns + (0,28 ns/pF) C _L
LOW to HIGH	5	t _{TLH}	60	120	ns	10 ns + (1,0 ns/pF) C _L
	10		30	60	ns	9 ns + (0,42 ns/pF) C _L
	15		20	40	ns	6 ns + (0,28 ns/pF) C _L

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$750 f_i + \sum(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz)
	10		f_o = output freq. (MHz)
	15		C_L = load capacitance (pF)
			$\sum(f_o C_L)$ = sum of outputs
			V_{DD} = supply voltage (V)

QUADRUPLE D-TYPE REGISTER WITH 3-STATE OUTPUTS



The HEF4076B is a quadruple edge-triggered D-type flip-flop with four data inputs (D_0 to D_3), two active LOW data enable inputs (\overline{ED}_0 and \overline{ED}_1), a common clock input (CP), four 3-state outputs (O_0 to O_3), two active LOW output enable inputs (\overline{EO}_0 and \overline{EO}_1), and an overriding asynchronous master reset input (MR).

Information on D_0 to D_3 is stored in the four flip-flops on the LOW to HIGH transition of CP if both \overline{ED}_0 and \overline{ED}_1 are LOW. A HIGH on either \overline{ED}_0 or \overline{ED}_1 prevents the flip-flops from changing on the LOW to HIGH transition of CP, independent of the information on D_0 to D_3 . When both \overline{EO}_0 and \overline{EO}_1 are LOW, the contents of the four flip-flops are available at O_0 to O_3 . A HIGH on either \overline{EO}_0 or \overline{EO}_1 forces O_0 to O_3 into the high impedance OFF-state. A HIGH on MR resets all four flip-flops, independent of all other input conditions.

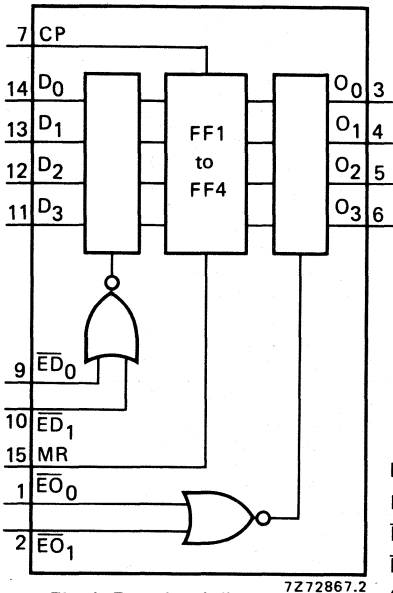
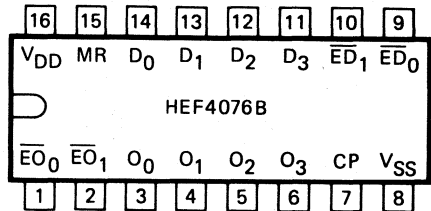


Fig. 1 Functional diagram.

7272867.2



7272868.2

Fig. 2 Pinning diagram.

HEF4076BP: 16-lead DIL; plastic (SOT-38Z).
HEF4076BD: 16-lead DIL; ceramic (SOT-74).
HEF4076BT: 16-lead flat pack; plastic (SO-16; SOT-109A).

PINNING

- D_0 to D_3 data inputs
- \overline{ED}_0 , \overline{ED}_1 data enable inputs (active LOW)
- \overline{EO}_0 , \overline{EO}_1 output enable inputs (active LOW)
- CP clock input (LOW to HIGH, edge-triggered)
- MR master reset input
- O_0 to O_3 data outputs

FAMILY DATA

I_{DD} LIMITS category MSI

} see Family Specifications

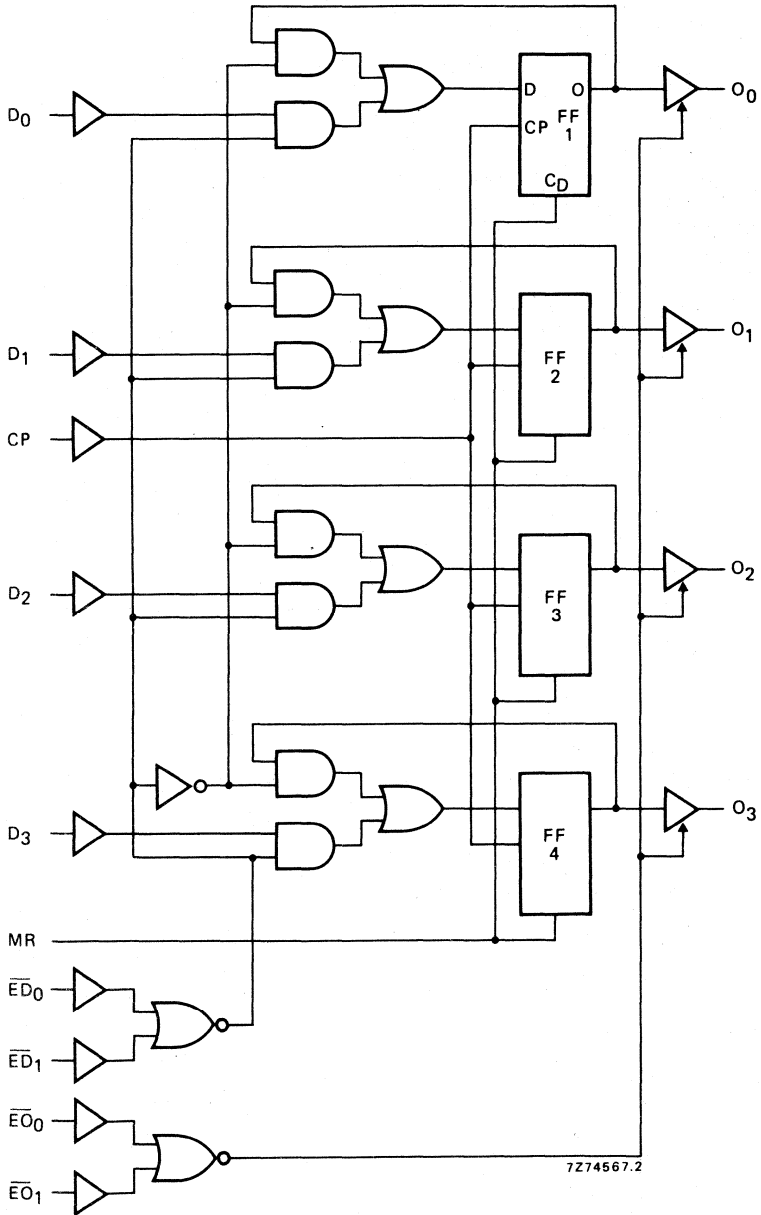


Fig. 3 Logic diagram.

FUNCTION TABLE

inputs					outputs
MR	CP	$\overline{E}D_0$	$\overline{E}D_1$	D_n	O_n
H	X	X	X	X	L
L	\int	H	X	X	no change
L	\int	X	H	X	no change
L	\int	L	L	H	H
L	\int	L	L	L	L
L	\setminus	X	X	X	no change

$\overline{E}O_0 = \overline{E}O_1 = \text{LOW}$

When either $\overline{E}O_0$ or $\overline{E}O_1$ is HIGH, the outputs are disabled (high impedance OFF-state).

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

X = state is immaterial

\int = positive-going transition

\setminus = negative-going transition

A.C. CHARACTERISTICS

$V_{SS} = 0 \text{ V}$; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$; $C_L = 50 \text{ pF}$; input transition times $\leq 20 \text{ ns}$; see also waveforms Fig. 4

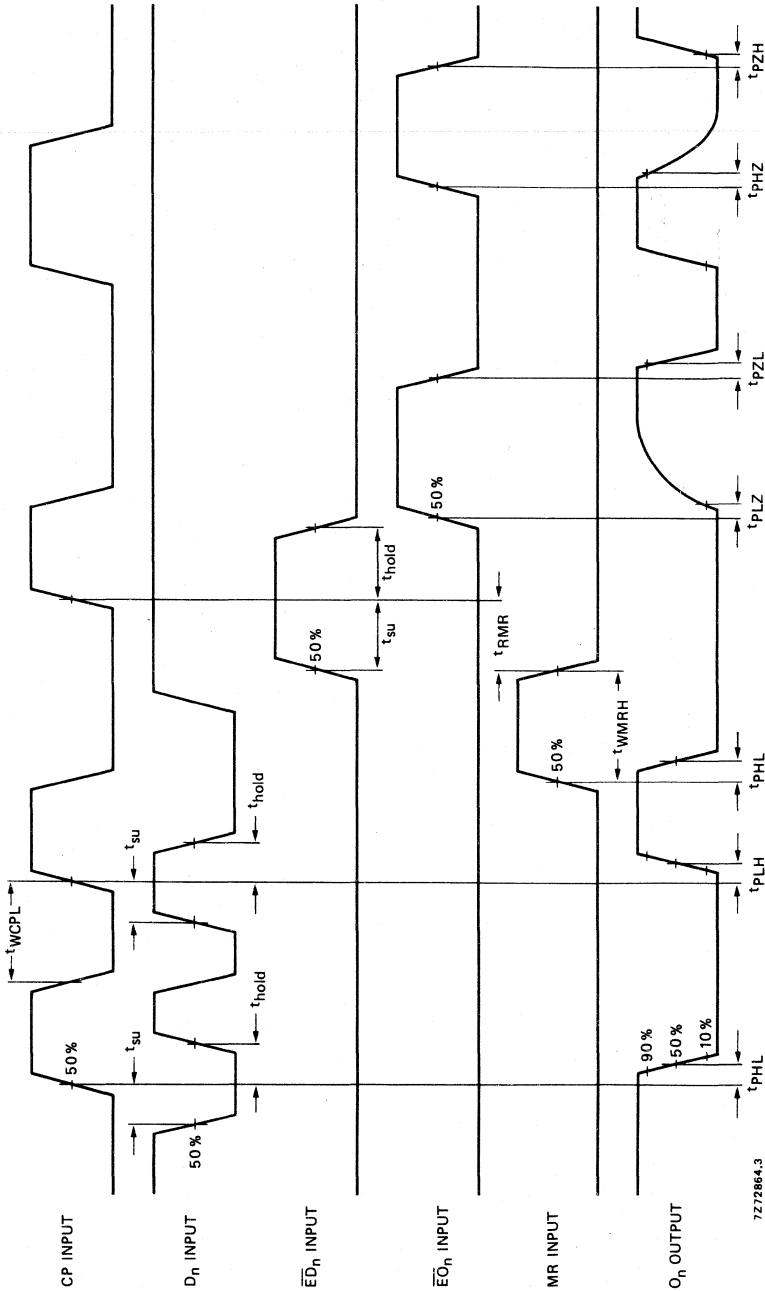
	V_{DD} V	symbol	min.	typ.	max.	typical extrapolation formula	
Propagation delays CP \rightarrow O_n HIGH to LOW	5	tPHL		150	305 ns	$123 \text{ ns} + (0,55 \text{ ns/pF}) C_L$	
	10		60	120 ns	$49 \text{ ns} + (0,23 \text{ ns/pF}) C_L$		
	15		45	85 ns	$37 \text{ ns} + (0,16 \text{ ns/pF}) C_L$		
LOW to HIGH	5	tPLH		160	320 ns	$133 \text{ ns} + (0,55 \text{ ns/pF}) C_L$	
	10		65	130 ns	$54 \text{ ns} + (0,23 \text{ ns/pF}) C_L$		
	15		45	90 ns	$37 \text{ ns} + (0,16 \text{ ns/pF}) C_L$		
MR \rightarrow O_n HIGH to LOW	5	tPHL		95	190 ns	$68 \text{ ns} + (0,55 \text{ ns/pF}) C_L$	
	10		40	85 ns	$29 \text{ ns} + (0,23 \text{ ns/pF}) C_L$		
	15		30	65 ns	$22 \text{ ns} + (0,16 \text{ ns/pF}) C_L$		
Output transition times HIGH to LOW	5	tTHL		60	120 ns	$10 \text{ ns} + (1,0 \text{ ns/pF}) C_L$	
	10		30	60 ns	$9 \text{ ns} + (0,42 \text{ ns/pF}) C_L$		
	15		20	40 ns	$6 \text{ ns} + (0,28 \text{ ns/pF}) C_L$		
LOW to HIGH	5	tTLH		60	120 ns	$10 \text{ ns} + (1,0 \text{ ns/pF}) C_L$	
	10		30	60 ns	$9 \text{ ns} + (0,42 \text{ ns/pF}) C_L$		
	15		20	40 ns	$6 \text{ ns} + (0,28 \text{ ns/pF}) C_L$		
3-state propagation delays							
	Output disable times $\overline{E}O_n \rightarrow O_n$ HIGH	5	tPHZ		50	105 ns	
		10		35	70 ns		
15		30		65 ns			
LOW	5	tPLZ		45	90 ns		
	10		30	65 ns			
	15		30	60 ns			
Output enable times $\overline{E}O_n \rightarrow O_n$ HIGH	5	tPZH		65	130 ns		
	10		30	55 ns			
	15		20	40 ns			
LOW	5	tPZL		60	120 ns		
	10		25	50 ns			
	15		20	35 ns			

A.C. CHARACTERISTICS

 $V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	symbol	min.	typ.	max.	typical extrapolation formula
Set-up times $D_n \rightarrow CP$	5	t_{su}	10	-15	ns	see also waveforms Fig. 4
	10		0	-10	ns	
	15		0	-5	ns	
$\overline{ED}_n \rightarrow CP$	5	t_{su}	0	-50	ns	
	10		0	-20	ns	
	15		0	-15	ns	
Hold times $D_n \rightarrow CP$	5	t_{hold}	55	30	ns	
	10		20	10	ns	
	15		15	10	ns	
$\overline{ED}_n \rightarrow CP$	5	t_{hold}	25	-25	ns	
	10		10	-10	ns	
	15		5	-5	ns	
Minimum clock pulse width; LOW	5	t_{WCPL}	120	60	ns	
	10		45	20	ns	
	15		30	15	ns	
Minimum MR pulse width; HIGH	5	t_{WMRH}	55	25	ns	
	10		30	15	ns	
	15		20	10	ns	
Recovery time for MR	5	t_{RMR}	90	45	ns	
	10		35	15	ns	
	15		20	10	ns	
Maximum clock pulse frequency	5	f_{max}	4	8	MHz	
	10		11	22	MHz	
	15		16	32	MHz	

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$2200 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz)
	10		f_o = output freq. (MHz)
	15		C_L = load capacitance (pF)
			$\Sigma(f_o C_L)$ = sum of outputs
			V_{DD} = supply voltage (V)



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Fig. 4 Waveforms showing propagation delays, output disable/enable times, minimum CP and MR pulse widths, set-up and hold times for D_n to CP and E \overline{D}_n to CP, and recovery time for MR. Set-up and hold times are shown as positive values but may be specified as negative values.

QUADRUPLE EXCLUSIVE-NOR GATE



The HEF4077B provides the exclusive-NOR function. The outputs are fully buffered for best performance.

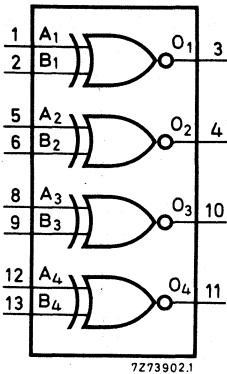


Fig. 1 Functional diagram.

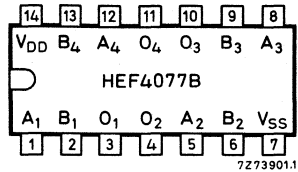


Fig. 2 Pinning diagram.

HEF4077BP: 14-lead DIL; plastic (SOT-27S, T, V).
HEF4077BD: 14-lead DIL; ceramic (SOT-73).
HEF4077BT: 14-lead flat pack; plastic (SO-14; SOT-108A).

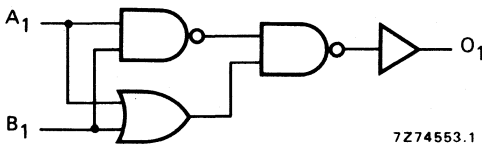


Fig. 3 Logic diagram (one gate).

TRUTH TABLE

A_n	B_n	O_n
L	L	H
L	H	L
H	L	L
H	H	H

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)

FAMILY DATA

I_{DD} LIMITS category GATES

} see Family Specifications

A.C. CHARACTERISTICS

 $V_{SS} = 0 \text{ V}$; $T_{amb} = 25 \text{ }^\circ\text{C}$; $C_L = 50 \text{ pF}$; input transition times $\leq 20 \text{ ns}$

	V_{DD} V	symbol	typ.	max.		typical extrapolation formula
Propagation delays $A_n, B_n \rightarrow O_n$ HIGH to LOW	5	t_{PHL}	75	150	ns	$48 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
	10		35	70	ns	$24 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
	15		30	55	ns	$22 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
LOW to HIGH	5	t_{PLH}	70	145	ns	$43 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
	10		30	60	ns	$19 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
	15		25	50	ns	$17 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
Output transition times HIGH to LOW	5	t_{THL}	60	120	ns	$10 \text{ ns} + (1,0 \text{ ns/pF}) C_L$
	10		30	60	ns	$9 \text{ ns} + (0,42 \text{ ns/pF}) C_L$
	15		20	40	ns	$6 \text{ ns} + (0,28 \text{ ns/pF}) C_L$
LOW to HIGH	5	t_{TLH}	60	120	ns	$10 \text{ ns} + (1,0 \text{ ns/pF}) C_L$
	10		30	60	ns	$9 \text{ ns} + (0,42 \text{ ns/pF}) C_L$
	15		20	40	ns	$6 \text{ ns} + (0,28 \text{ ns/pF}) C_L$

	V_{DD} V	typical formula for P (μW)	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
Dynamic power dissipation per package (P)	5	$850 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	10	$4\,500 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$14\,700 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	



8-INPUT NOR GATE

The HEF4078B provides the positive 8-input NOR function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

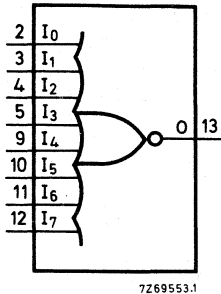


Fig. 1 Functional diagram.

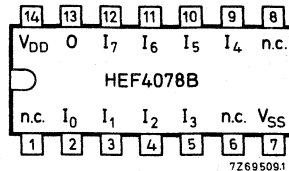


Fig. 2 Pinning diagram.

HEF4078BP: 14-lead DIL; plastic (SOT-27S, T, V).

HEF4078BD: 14-lead DIL; ceramic (SOT-73).

HEF4078BT: 14-lead flat pack; plastic (SO-14; SOT-108A).

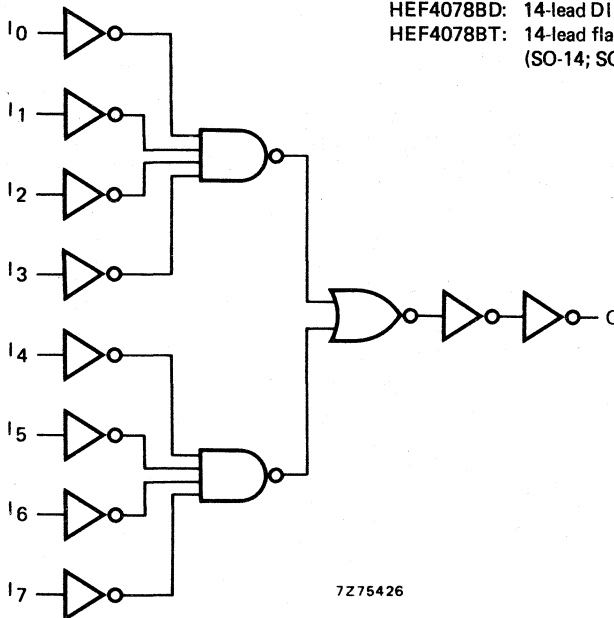


Fig. 3 Logic diagram.

FAMILY DATA

I_{DD} LIMITS category GATES

} see Family Specifications

A.C. CHARACTERISTICS

 $V_{SS} = 0 \text{ V}$; $T_{amb} = 25^\circ \text{C}$; $C_L = 50 \text{ pF}$; input transition times $\leq 20 \text{ ns}$

	V_{DD} V	symbol	typ.	max.		typical extrapolation formula	
Propagation delays $I_n \rightarrow O_n$ HIGH to LOW	5	t _{PHL}	80	160	ns	53 ns + (0,55 ns/pF) C _L	
	10		35	70	ns	24 ns + (0,23 ns/pF) C _L	
	15		25	50	ns	17 ns + (0,16 ns/pF) C _L	
	LOW to HIGH	5	t _{PLH}	80	160	ns	53 ns + (0,55 ns/pF) C _L
		10		35	70	ns	24 ns + (0,23 ns/pF) C _L
		15		25	50	ns	17 ns + (0,16 ns/pF) C _L
Output transition times	HIGH to LOW	t _{THL}	60	120	ns	10 ns + (1,0 ns/pF) C _L	
			10	30	60	ns	9 ns + (0,42 ns/pF) C _L
			15	20	40	ns	6 ns + (0,28 ns/pF) C _L
	LOW to HIGH	t _{TLH}	60	120	ns	10 ns + (1,0 ns/pF) C _L	
			10	30	60	ns	9 ns + (0,42 ns/pF) C _L
			15	20	40	ns	6 ns + (0,28 ns/pF) C _L

	V_{DD} V	typical formula for P (μW)	where f _i = input freq. (MHz) f _o = output freq. (MHz) C _L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V _{DD} = supply voltage (V)
Dynamic power dissipation per package (P)	5	$750 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	10	$2800 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$7500 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

QUADRUPLE 2-INPUT AND GATE



The HEF4081B provides the positive quadruple 2-input AND function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

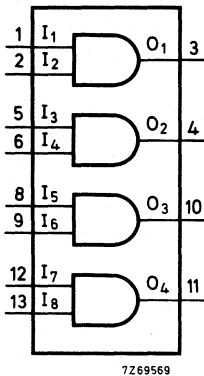


Fig.1 Functional diagram.

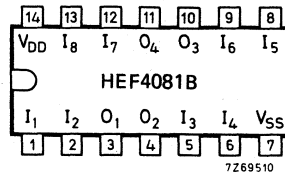


Fig.2 Pinning diagram.

HEF4081BP: 14-lead DIL; plastic (SOT-27S, T, V).

HEF4081BD: 14-lead DIL; ceramic (SOT-73).

HEF4081BT: 14-lead flat pack; plastic (SO-14; SOT-108A).

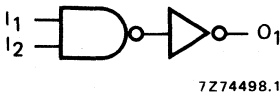


Fig.3 Logic diagram (one gate).

FAMILY DATA

I_{DD} LIMITS category GATES

see Family Specifications

A.C. CHARACTERISTICS

 $V_{SS} = 0 \text{ V}; T_{amb} = 25 \text{ }^\circ\text{C}; C_L = 50 \text{ pF}; \text{input transition times} \leq 20 \text{ ns}$

	V_{DD} V	symbol	typ.	max.		typical extrapolation formula	
Propagation delays $I_n \rightarrow O_n$ HIGH to LOW	5	t _{PHL}	55	110	ns	28 ns + (0,55 ns/pF) C _L	
	10		25	50	ns	14 ns + (0,23 ns/pF) C _L	
	15		20	40	ns	12 ns + (0,16 ns/pF) C _L	
	LOW to HIGH	5	t _{PLH}	45	90	ns	18 ns + (0,55 ns/pF) C _L
		10		20	40	ns	9 ns + (0,23 ns/pF) C _L
		15		15	30	ns	7 ns + (0,16 ns/pF) C _L
Output transition times HIGH to LOW	5	t _{THL}	60	120	ns	10 ns + (1,0 ns/pF) C _L	
	10		30	60	ns	9 ns + (0,42 ns/pF) C _L	
	15		20	40	ns	6 ns + (0,28 ns/pF) C _L	
	LOW to HIGH	5	t _{TLH}	60	120	ns	10 ns + (1,0 ns/pF) C _L
		10		30	60	ns	9 ns + (0,42 ns/pF) C _L
		15		20	40	ns	6 ns + (0,28 ns/pF) C _L

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$800 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz)
	10		f_o = output freq. (MHz)
	15		C_L = load capacitance (pF)
			$\Sigma(f_o C_L)$ = sum of outputs
			V_{DD} = supply voltage (V)

DUAL 4-INPUT AND GATE



The HEF4082B provides the positive dual 4-input AND function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

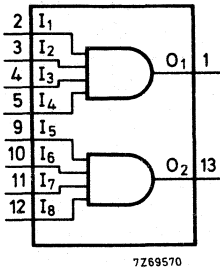


Fig. 1 Functional diagram.

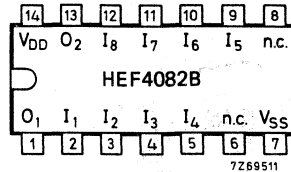


Fig. 2 Pinning diagram.

HEF4082BP: 14-lead DIL; plastic (SOT-27S, T, V).

HEF4082BD: 14-lead DIL; ceramic (SOT-73).

HEF4082BT: 14-lead flat pack; plastic (SO-14; SOT-108A).

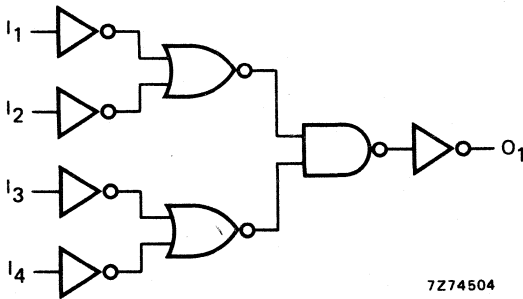


Fig. 3 Logic diagram (one gate).

FAMILY DATA

IDD LIMITS category GATES

see Family Specifications

A.C. CHARACTERISTICS

 $V_{SS} = 0 \text{ V}$; $T_{amb} = 25 \text{ }^\circ\text{C}$; $C_L = 50 \text{ pF}$; input transition times $\leq 20 \text{ ns}$

	V_{DD} V	symbol	typ.	max.		typical extrapolation formula
Propagation delays $I_n \rightarrow O_n$	5	$t_{PHL}; t_{PLH}$	65	125	ns	$38 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
	10		30	60	ns	$19 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
	15		25	45	ns	$17 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
Output transition times HIGH to LOW	5	t_{THL}	60	120	ns	$10 \text{ ns} + (1,0 \text{ ns/pF}) C_L$
	10		30	60	ns	$9 \text{ ns} + (0,42 \text{ ns/pF}) C_L$
	15		20	40	ns	$6 \text{ ns} + (0,28 \text{ ns/pF}) C_L$
LOW to HIGH	5	t_{TLH}	60	120	ns	$10 \text{ ns} + (1,0 \text{ ns/pF}) C_L$
	10		30	60	ns	$9 \text{ ns} + (0,42 \text{ ns/pF}) C_L$
	15		20	40	ns	$6 \text{ ns} + (0,28 \text{ ns/pF}) C_L$

	V_{DD} V	typical formula for P (μW)	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
Dynamic power dissipation per package (P)	5	$1500 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	10	$6700 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$16800 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATE



The HEF4085B is a dual 2-wide 2-input AND-OR-invert gate, each with an additional input (A_4 or B_4) which can be used as either an expander input or an inhibit input. A HIGH on A_4 or B_4 forces the output (O_A or O_B) LOW independent of the other inputs (A_0 to A_3 or B_0 to B_3). The outputs O_A and O_B are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

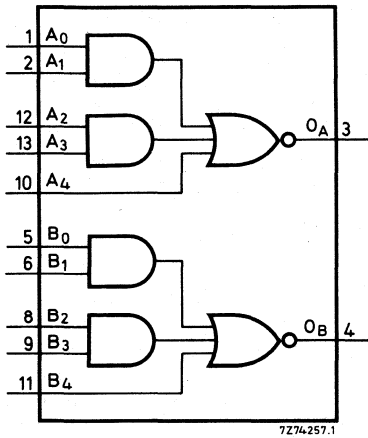


Fig. 1 Functional diagram.

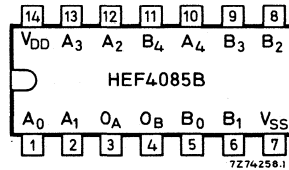


Fig. 2 Pinning diagram.

HEF4085BP: 14-lead DIL; plastic (SOT-27S, T, V).
HEF4085BD: 14-lead DIL; ceramic (SOT-73).
HEF4085BT: 14-lead flat pack; plastic (SO-14; SOT-108A).

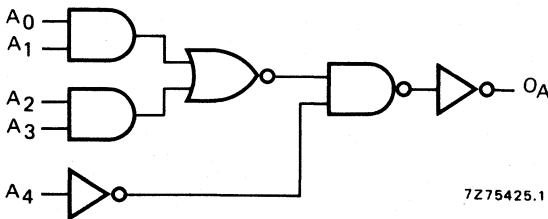


Fig. 3 Logic diagram (one gate).

LOGIC FUNCTION

$$O_A = \overline{A_0 \cdot A_1 + A_2 \cdot A_3 + A_4}$$

$$O_B = \overline{B_0 \cdot B_1 + B_2 \cdot B_3 + B_4}$$

FAMILY DATA

I_{DD} LIMITS category GATES

} see Family Specifications

A.C. CHARACTERISTICS

 $V_{SS} = 0 \text{ V}; T_{amb} = 25 \text{ }^\circ\text{C}; C_L = 50 \text{ pF}; \text{input transition times} \leq 20 \text{ ns}$

	V_{DD} V	symbol	typ.	max.		typical extrapolation formula
Propagation delays $A_n, B_n \rightarrow O_n$ HIGH to LOW	5	tPHL	75	155	ns	$48 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
	10		30	60	ns	$19 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
	15		20	40	ns	$12 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
LOW to HIGH	5	tPLH	65	135	ns	$38 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
	10		30	55	ns	$19 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
	15		20	40	ns	$12 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
Output transition times HIGH to LOW	5	tTHL	60	120	ns	$10 \text{ ns} + (1,0 \text{ ns/pF}) C_L$
	10		30	60	ns	$9 \text{ ns} + (0,42 \text{ ns/pF}) C_L$
	15		20	40	ns	$6 \text{ ns} + (0,28 \text{ ns/pF}) C_L$
LOW to HIGH	5	tTLH	60	120	ns	$10 \text{ ns} + (1,0 \text{ ns/pF}) C_L$
	10		30	60	ns	$9 \text{ ns} + (0,42 \text{ ns/pF}) C_L$
	15		20	40	ns	$6 \text{ ns} + (0,28 \text{ ns/pF}) C_L$

	V_{DD} V	typical formula for P (μW)	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
Dynamic power dissipation per package (P)	5	$750 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	10	$3200 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$9200 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

4-WIDE 2-INPUT AND-OR-INVERT GATE



The HEF4086B is a 4-wide 2-input AND-OR-invert (AOI) gate with two additional inputs (I_8 and \bar{I}_9) which can be used as either expander or inhibit inputs by connecting them to any standard LOCMOS output. A HIGH on I_8 or a LOW on \bar{I}_9 forces the output (O) LOW independent of the other eight inputs (I_0 to I_7). The output (O) is fully buffered for highest noise immunity and pattern insensitivity of output impedance.

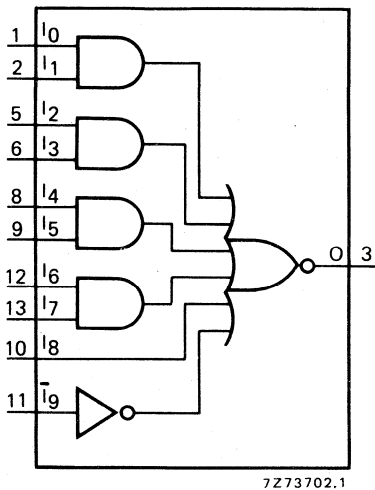


Fig. 1 Functional diagram.

PINNING

I_0 to I_8 gate inputs
 \bar{I}_9 gate input (active LOW)
 O output (active LOW)

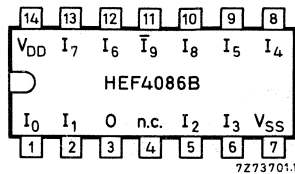


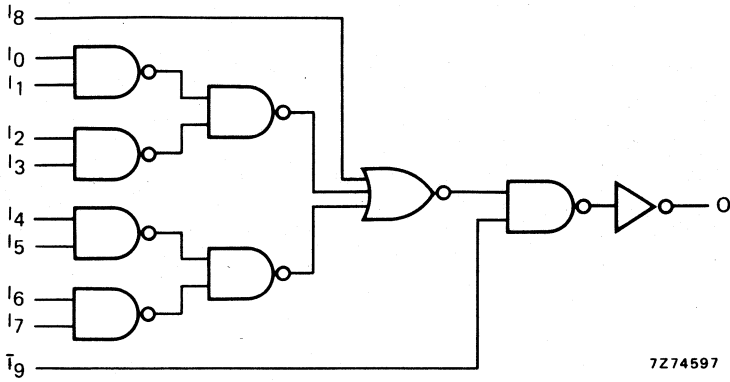
Fig. 2 Pinning diagram.

HEF4086BP: 14-lead DIL; plastic (SOT-27S, T, V).
 HEF4086BD: 14-lead DIL; ceramic (SOT-73).
 HEF4086BT: 14-lead flat pack; plastic
 (SO-14; SOT-108A).

FAMILY DATA

I_{DD} LIMITS category GATES

} see Family Specifications



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Fig. 3 Logic diagram.

LOGIC EQUATION

$$O = I_0 \cdot I_1 + I_2 \cdot I_3 + I_4 \cdot I_5 + I_6 \cdot I_7 + I_8 + I_9$$

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V _{DD} V	symbol	typ.	max.		typical extrapolation formula
Propagation delays I ₀ to I ₇ → 0 HIGH to LOW	5	t _{PHL}	90	180	ns	63 ns + (0,55 ns/pF) C _L
	10		30	65	ns	19 ns + (0,23 ns/pF) C _L
	15		20	40	ns	12 ns + (0,16 ns/pF) C _L
LOW to HIGH	5	t _{PLH}	80	155	ns	53 ns + (0,55 ns/pF) C _L
	10		30	60	ns	19 ns + (0,23 ns/pF) C _L
	15		20	40	ns	12 ns + (0,16 ns/pF) C _L
I ₈ → 0 HIGH to LOW	5	t _{PHL}	70	140	ns	43 ns + (0,55 ns/pF) C _L
	10		25	55	ns	14 ns + (0,23 ns/pF) C _L
	15		20	40	ns	12 ns + (0,16 ns/pF) C _L
LOW to HIGH	5	t _{PLH}	55	115	ns	28 ns + (0,55 ns/pF) C _L
	10		20	40	ns	9 ns + (0,23 ns/pF) C _L
	15		15	25	ns	7 ns + (0,16 ns/pF) C _L
I ₉ → 0 HIGH to LOW	5	t _{PHL}	55	105	ns	28 ns + (0,55 ns/pF) C _L
	10		20	45	ns	9 ns + (0,23 ns/pF) C _L
	15		15	30	ns	7 ns + (0,16 ns/pF) C _L
LOW to HIGH	5	t _{PLH}	45	90	ns	18 ns + (0,55 ns/pF) C _L
	10		15	35	ns	4 ns + (0,23 ns/pF) C _L
	15		10	25	ns	2 ns + (0,16 ns/pF) C _L
Output transition times HIGH to LOW	5	t _{THL}	60	120	ns	10 ns + (1,0 ns/pF) C _L
	10		30	60	ns	9 ns + (0,42 ns/pF) C _L
	15		20	40	ns	6 ns + (0,28 ns/pF) C _L
LOW to HIGH	5	t _{TLH}	60	120	ns	10 ns + (1,0 ns/pF) C _L
	10		30	60	ns	9 ns + (0,42 ns/pF) C _L
	15		20	40	ns	6 ns + (0,28 ns/pF) C _L

	V _{DD} V	typical formula for P (μW)	where f _i = input freq. (MHz) f _o = output freq. (MHz) C _L = load capacitance (pF) Σ(f _o C _L) = sum of outputs V _{DD} = supply voltage (V)
Dynamic power dissipation per package (P)	5	525 f _i + Σ(f _o C _L) × V _{DD} ²	
	10	2600 f _i + Σ(f _o C _L) × V _{DD} ²	
	15	7300 f _i + Σ(f _o C _L) × V _{DD} ²	

APPLICATION INFORMATION

Figure 4 shows two HEF4086B ICs connected to obtain an 8-wide 2-input AOI function. The output (O_A) of the first IC is fed directly into the \bar{T}_B gate input of the second IC. Similarly, any NAND gate output can be fed directly into the \bar{T}_g gate input to obtain a 5-wide AOI function. In addition, any AND gate output can be fed directly into the I_g gate input with the same result.

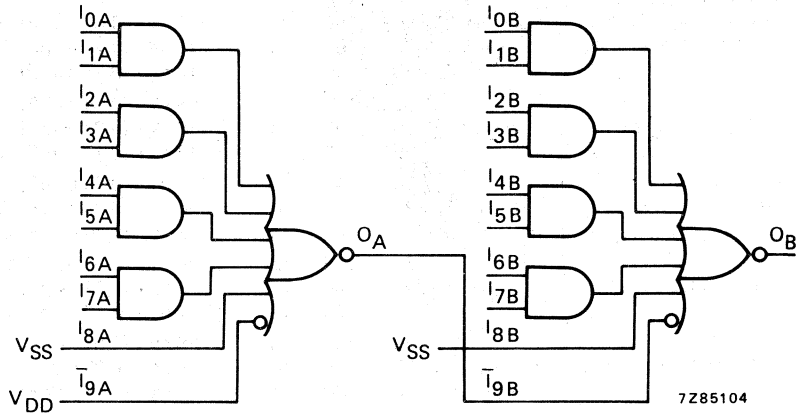


Fig. 4 Two HEF4086B ICs connected as an 8-wide 2-input AOI gate.

Logic equation for Fig. 4:

$$O_B = I_{0A} \cdot I_{1A} + I_{2A} \cdot I_{3A} + I_{4A} \cdot I_{5A} + I_{6A} \cdot I_{7A} + I_{0B} \cdot I_{1B} + I_{2B} \cdot I_{3B} + I_{4B} \cdot I_{5B} + I_{6B} \cdot I_{7B}$$

QUADRUPLE 2-INPUT NAND SCHMITT TRIGGER



The HEF4093B consists of four Schmitt-trigger circuits. Each circuit functions as a two-input NAND gate with Schmitt-trigger action on both inputs. The gate switches at different points for positive and negative-going signals. The difference between the positive voltage (V_{IH}) and the negative voltage (V_{IL}) is defined as hysteresis voltage (V_H).

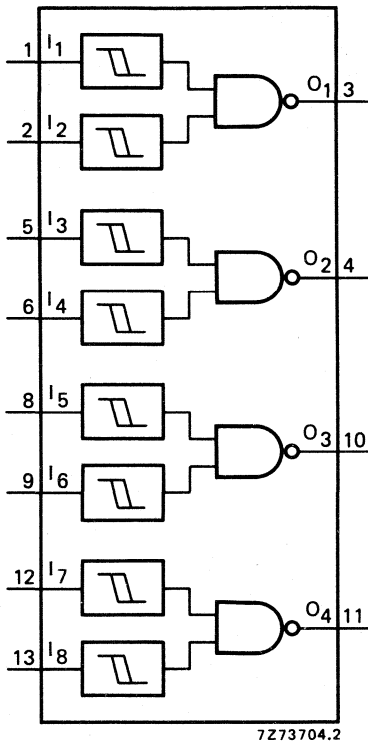


Fig. 1 Functional diagram.

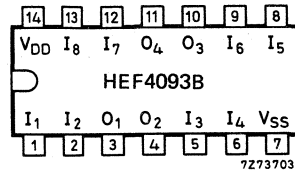


Fig. 2 Pinning diagram.

HEF4093BP: 14-lead DIL; plastic (SOT-27S, T, V).
HEF4093BD: 14-lead DIL; ceramic (SOT-73).
HEF4093BT: 14-lead flat pack; plastic (SO-14; SOT-108A).

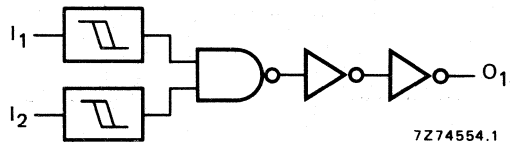


Fig. 3 Logic diagram (one gate).

FAMILY DATA

I_{DD} LIMITS category GATES

} see Family Specifications

D.C. CHARACTERISTICS

$V_{SS} = 0 \text{ V}; T_{amb} = 25 \text{ }^\circ\text{C}$

	V_{DD} V	symbol	min.	typ.	max.	
Hysteresis voltage	5	V_H	0,4	0,7		V
	10		0,6	1,0		V
	15		0,7	1,3		V
Switching levels positive-going input voltage	5	V_{IH}		2,9	3,5	V
	10			5,2	7	V
	15			7,3	11	V
negative-going input voltage	5	V_{IL}	1,5	2,2		V
	10		3	4,2		V
	15		4	6,0		V

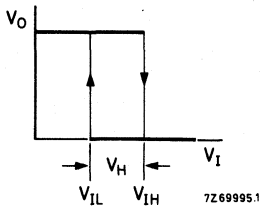


Fig. 4 Transfer characteristic.

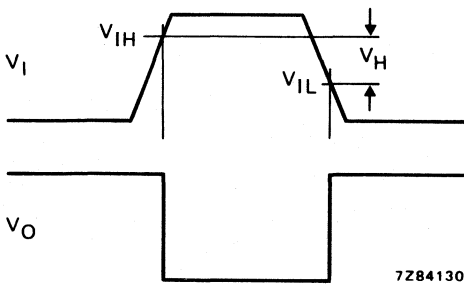


Fig. 5 Waveforms showing definition of V_{IH} , V_{IL} and V_H ; where V_{IL} and V_{IH} are between limits of 30% and 70%.

A.C. CHARACTERISTICS

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^\circ\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	symbol	typ.	max.		typical extrapolation formula
Propagation delays $I_n \rightarrow O_n$ HIGH to LOW	5	t_{PHL}	90	185	ns	$63\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10		40	80	ns	$29\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15		30	60	ns	$22\text{ ns} + (0,16\text{ ns/pF}) C_L$
LOW to HIGH	5	t_{PLH}	85	170	ns	$58\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10		40	80	ns	$29\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15		30	60	ns	$22\text{ ns} + (0,16\text{ ns/pF}) C_L$
Output transition times HIGH to LOW	5	t_{THL}	60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$
	10		30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$
	15		20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$
LOW to HIGH	5	t_{TLH}	60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$
	10		30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$
	15		20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$1300 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz)
	10		f_o = output freq. (MHz)
	15		C_L = load capacitance (pF)
			$\Sigma(f_o C_L)$ = sum of outputs
			V_{DD} = supply voltage (V)

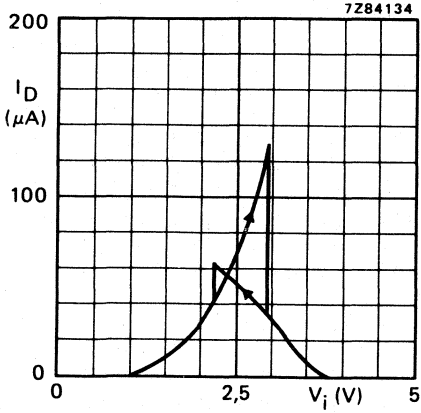


Fig. 6 Typical drain current as a function of input voltage; $V_{DD} = 5$ V; $T_{amb} = 25$ °C.

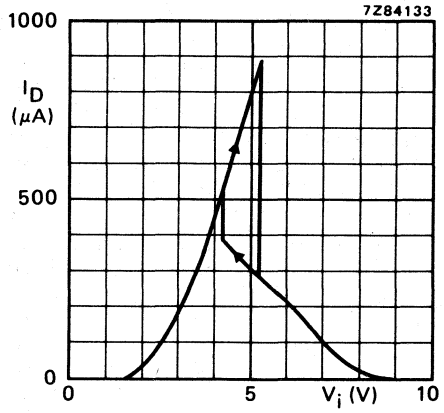


Fig. 7 Typical drain current as a function of input voltage; $V_{DD} = 10$ V; $T_{amb} = 25$ °C.

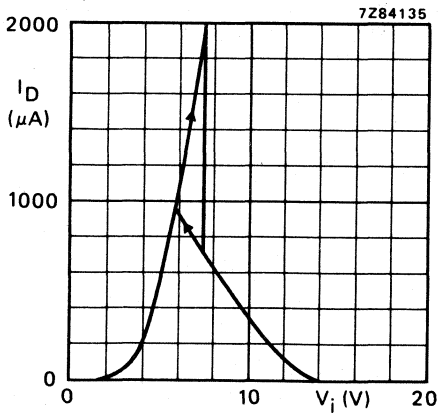


Fig. 8 Typical drain current as a function of input voltage; $V_{DD} = 15$ V; $T_{amb} = 25$ °C.

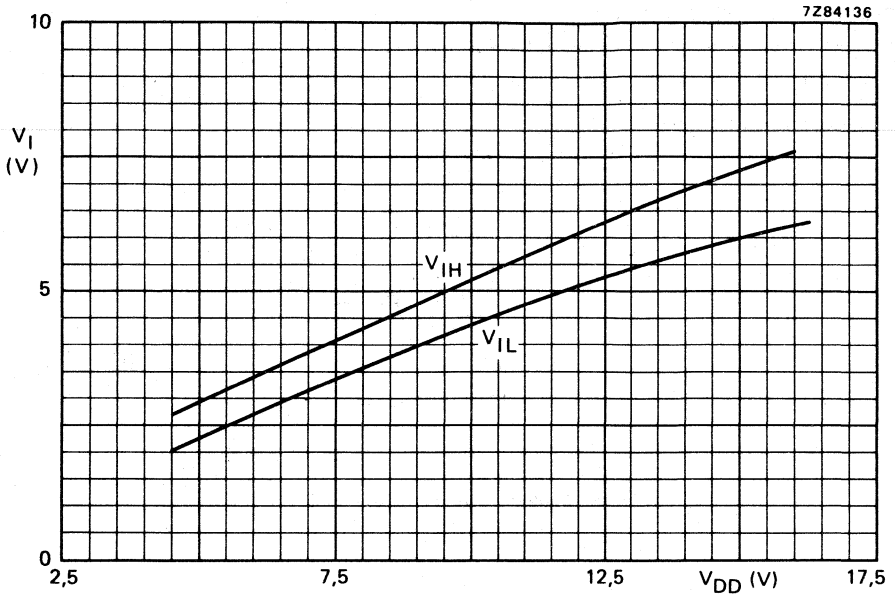


Fig. 9 Typical switching levels as a function of supply voltage V_{DD} ; $T_{amb} = 25\text{ }^\circ\text{C}$.

APPLICATION INFORMATION

Some examples of applications for the HEF4093B are:

- Wave and pulse shapers
- Astable multivibrators
- Monostable multivibrators.

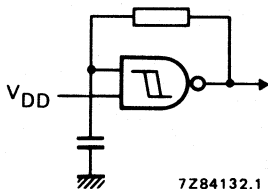


Fig. 10 The HEF4093B used as a astable multivibrator.

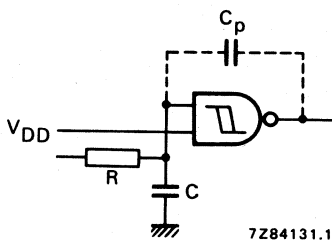


Fig. 11 Schmitt trigger driven via a high impedance ($R > 1 \text{ k}\Omega$).

If a Schmitt trigger is driven via a high impedance ($R > 1 \text{ k}\Omega$) then it is necessary to incorporate a capacitor C of such value that: $\frac{C}{C_p} > \frac{V_{DD}-V_{SS}}{V_H}$, otherwise oscillation can occur on the edges of a pulse.

C_p is the external parasitic capacitance between inputs and output; the value depends on the circuit board layout.

Note

The two inputs may be connected together, but this will result in a larger through-current at the moment of switching.

8-STAGE SHIFT-AND-STORE BUS REGISTER



The HEF4094B is an 8-stage serial shift register having a storage latch associated with each stage for strobing data from the serial input to parallel buffered 3-state outputs O_0 to O_7 . The parallel outputs may be connected directly to common bus lines. Data is shifted on positive-going clock transitions. The data in each shift register stage is transferred to the storage register when the strobe (STR) input is HIGH. Data in the storage register appears at the outputs whenever the output enable (EO) signal is HIGH.

Two serial outputs (O_s and O_s') are available for cascading a number of HEF4094B devices. Data is available at O_s on positive-going clock edges to allow high-speed operation in cascaded systems in which the clock rise time is fast. The same serial information is available at O_s' on the next negative-going clock edge and provides cascading HEF4094B devices when the clock rise time is slow.

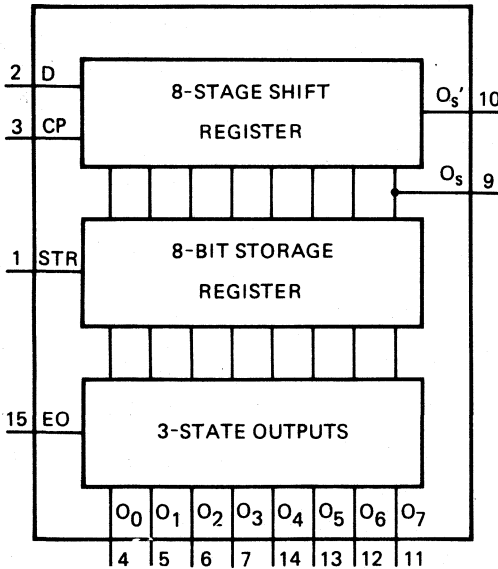


Fig. 1 Functional diagram.

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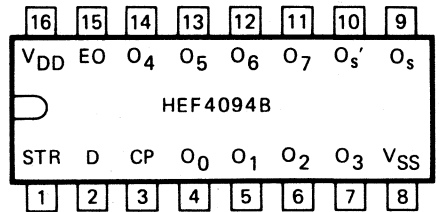


Fig. 2 Pinning diagram.

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HEF4094BP: 16-lead DIL; plastic (SOT-38Z).
HEF4094BD: 16-lead DIL; ceramic (SOT-74).
HEF4094BT: 16-lead flat pack; plastic (SO-16; SOT-109A).

PINNING

D	data input	EO	output enable input
CP	clock input	O_s, O_s'	serial outputs
STR	strobe input	O_0 to O_7	parallel outputs

FAMILY DATA

I_{DD} LIMITS category MSI } see Family Specifications

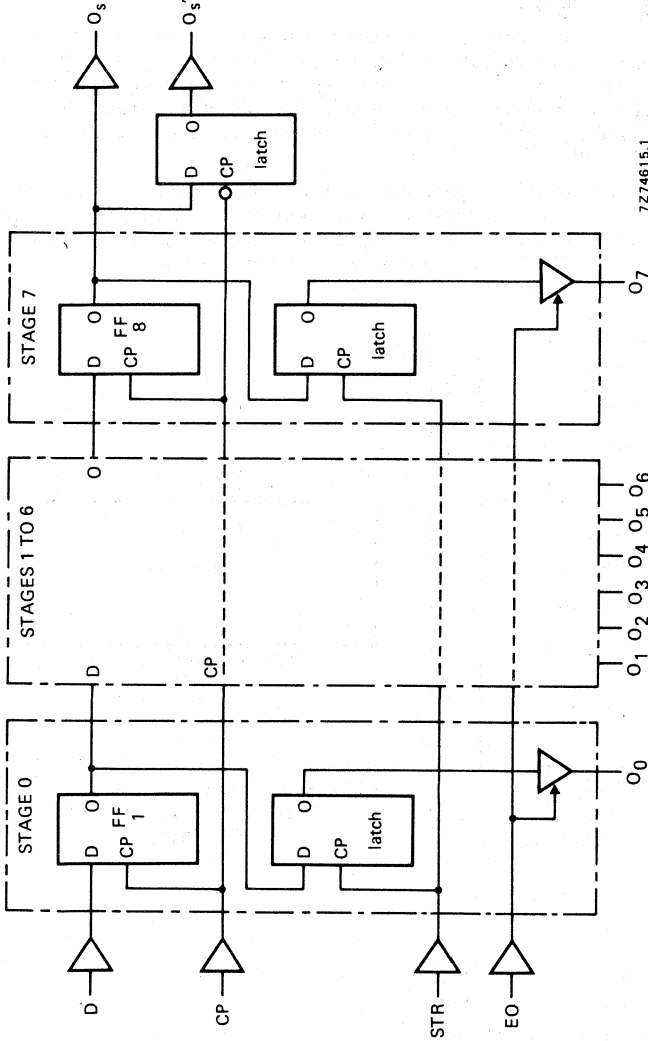


Fig. 3a Logic diagram.

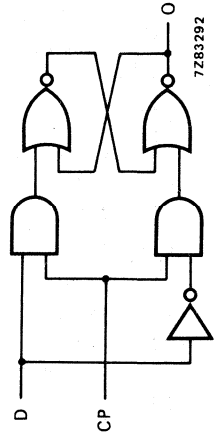


Fig. 3b One D-latch.

FUNCTION TABLE

inputs				parallel outputs		serial outputs	
CP	EO	STR	D	O ₀	O _n	O _s	O' _s
∕	L	X	X	Z	Z	O ₆	nc
∖	L	X	X	Z	Z	nc	O ₇
∕	H	L	X	nc	nc	O ₆	nc
∕	H	H	L	L	O _{n-1}	O ₆	nc
∕	H	H	H	H	O _{n-1}	O ₆	nc
∖	H	H	H	nc	nc	nc	O ₇

- H = HIGH state (the more positive voltage)
- L = LOW state (the less positive voltage)
- X = state is immaterial
- ∕ = positive-going transition
- ∖ = negative-going transition
- Z = high impedance off state
- nc = no change
- O₆ = the information in the seventh shift register stage

At the positive clock edge the information in the 7th register stage is transferred to the 8th register stage and the O_s output.

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ≤ 20 ns

	V _{DD} V	typical formula for P (μW)	where f _i = input freq. (MHz) f _o = output freq. (MHz) C _L = load capacitance (pF) Σ(f _o C _L) = sum of outputs V _{DD} = supply voltage (V)
Dynamic power dissipation per package (P)	5	2100 f _i + Σ(f _o C _L) × V _{DD} ²	
	10	9700 f _i + Σ(f _o C _L) × V _{DD} ²	
	15	26 000 f _i + Σ(f _o C _L) × V _{DD} ²	

A.C. CHARACTERISTICS

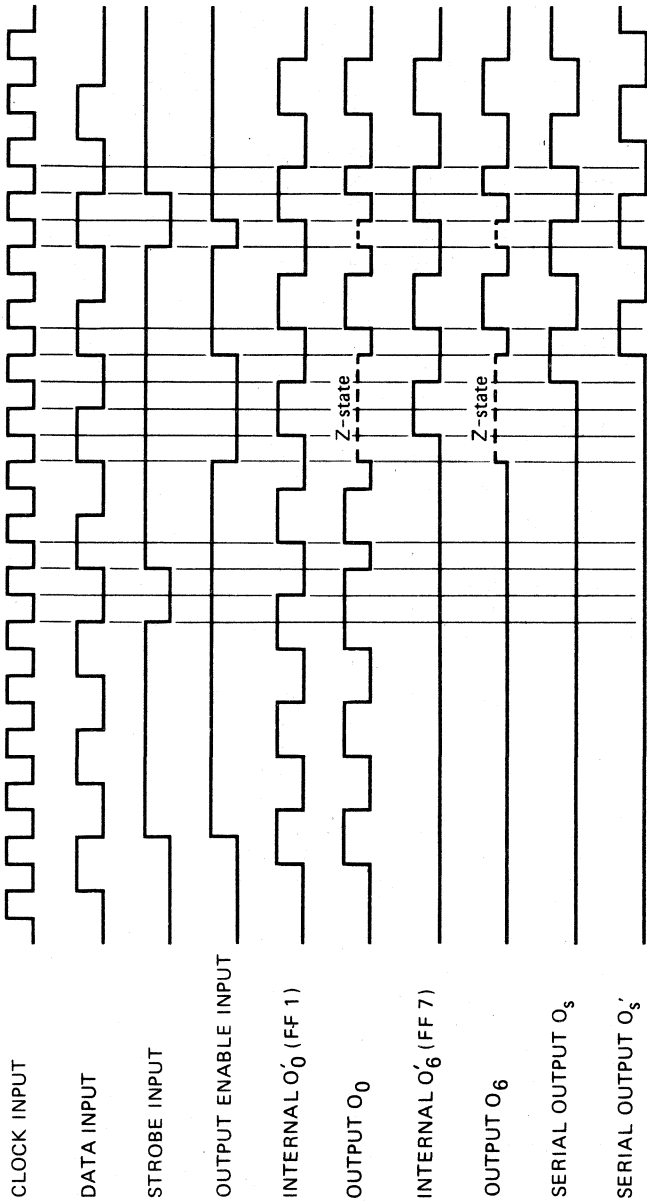
 $V_{SS} = 0 \text{ V}$; $T_{amb} = 25 \text{ }^\circ\text{C}$; $C_L = 50 \text{ pF}$; input transition times $\leq 20 \text{ ns}$

	V_{DD} V	symbol	typ.	max.		typical extrapolation formula
Propagation delays						
CP \rightarrow O_s	5		135	270	ns	$108 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
HIGH to LOW	10	tPHL	65	130	ns	$54 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
	15		50	100	ns	$42 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
	5		105	210	ns	$78 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
LOW to HIGH	10	tPLH	50	100	ns	$39 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
	15		40	80	ns	$32 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
	5		105	210	ns	$78 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
CP \rightarrow O'_s	5		105	210	ns	$78 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
HIGH to LOW	10	tPHL	50	100	ns	$39 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
	15		40	80	ns	$32 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
	5		105	210	ns	$78 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
LOW to HIGH	10	tPLH	50	100	ns	$39 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
	15		40	80	ns	$32 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
	5		105	210	ns	$78 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
CP \rightarrow O_n	5		165	330	ns	$138 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
HIGH to LOW	10	tPHL	75	150	ns	$64 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
	15		55	110	ns	$47 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
	5		150	300	ns	$123 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
LOW to HIGH	10	tPLH	70	140	ns	$59 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
	15		55	110	ns	$47 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
	5		100	200	ns	$73 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
STR \rightarrow O_n	5		110	220	ns	$83 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
HIGH to LOW	10	tPHL	50	100	ns	$39 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
	15		35	70	ns	$27 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
	5		100	200	ns	$73 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
LOW to HIGH	10	tPLH	45	90	ns	$34 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
	15		35	70	ns	$27 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
	5		100	200	ns	$73 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
Output transition times						
HIGH to LOW	5		60	120	ns	$10 \text{ ns} + (1,0 \text{ ns/pF}) C_L$
	10	tTHL	30	60	ns	$9 \text{ ns} + (0,42 \text{ ns/pF}) C_L$
	15		20	40	ns	$6 \text{ ns} + (0,28 \text{ ns/pF}) C_L$
	5		60	120	ns	$10 \text{ ns} + (1,0 \text{ ns/pF}) C_L$
LOW to HIGH	10	tTLH	30	60	ns	$9 \text{ ns} + (0,42 \text{ ns/pF}) C_L$
	15		20	40	ns	$6 \text{ ns} + (0,28 \text{ ns/pF}) C_L$
	5		60	120	ns	$10 \text{ ns} + (1,0 \text{ ns/pF}) C_L$

A.C. CHARACTERISTICS

 $V_{SS} = 0 \text{ V}$; $T_{amb} = 25 \text{ }^\circ\text{C}$; $C_L = 50 \text{ pF}$; input transition times $\leq 20 \text{ ns}$

	V_{DD} V	symbol	min.	typ.	max.
3-state propagation delays					
Output enable times	5			40	80 ns
EO \rightarrow O_n	10	t_{PZH}		25	50 ns
HIGH	15			20	40 ns
	5			40	80 ns
LOW	10	t_{PZL}		25	50 ns
	15			20	40 ns
Output disable times	5			75	150 ns
EO \rightarrow O_n	10	t_{PHZ}		40	80 ns
HIGH	15			30	60 ns
	5			80	160 ns
LOW	10	t_{PLZ}		40	80 ns
	15			30	60 ns
Minimum clock pulse width	5		60	30	ns
LOW	10	t_{WCPL}	30	15	ns
	15		24	12	ns
Minimum strobe pulse width	5		40	20	ns
HIGH	10	t_{WSTRH}	30	15	ns
	15		24	12	ns
Set-up times	5		60	30	ns
D \rightarrow CP	10	t_{su}	20	10	ns
	15		15	5	ns
Hold times	5		5	-15	ns
D \rightarrow CP	10	t_{hold}	20	5	ns
	15		20	5	ns
Maximum clock pulse frequency	5		5	10	MHz
	10	f_{max}	11	22	MHz
	15		14	28	MHz



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Fig. 4 Timing diagram.

APPLICATION INFORMATION

Some examples of applications for the HEF4094B are:

- Serial-to-parallel data conversion
- Remote control holding register

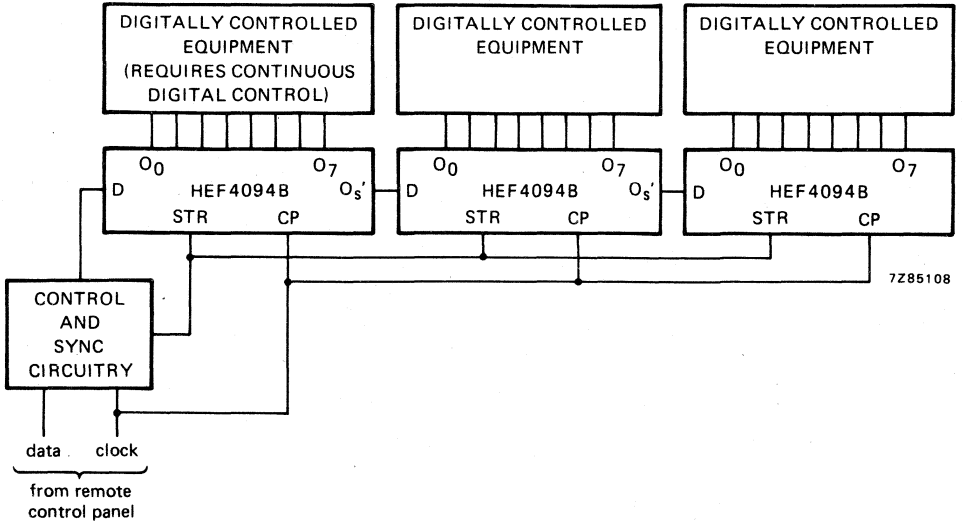


Fig. 5 Remote control holding register.

QUADRUPLE LOW TO HIGH VOLTAGE TRANSLATOR WITH 3-STATE OUTPUTS

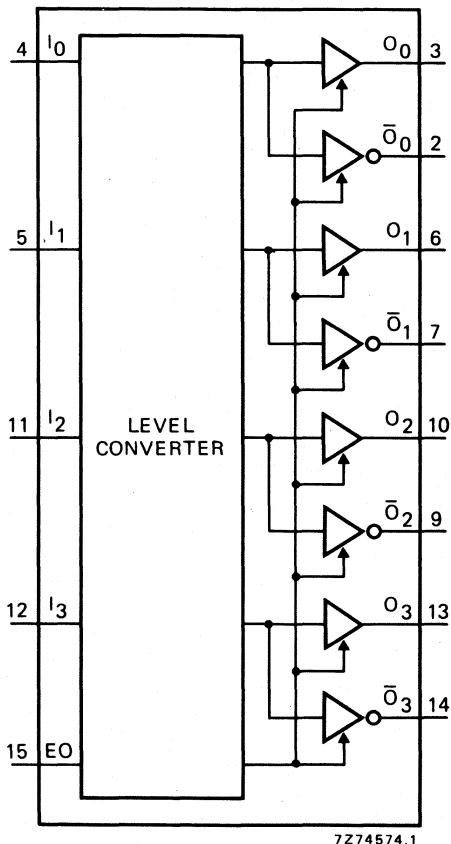


The HEF4104B quadruple low voltage to high voltage translator with 3-state outputs provides the capability of interfacing low voltage circuits to high voltage circuits, such as low voltage LOC MOS and TTL to high voltage LOC MOS. It has four data inputs (I_0 to I_3), an active HIGH output enable input (EO), four data outputs (O_0 to O_3) and their complements (\bar{O}_0 to \bar{O}_3).

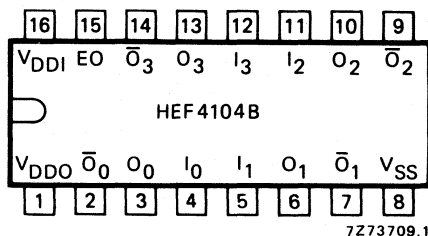
With EO HIGH, O_0 to O_3 and \bar{O}_0 to \bar{O}_3 are in the low impedance ON-state, either HIGH or LOW as determined by I_0 to I_3 ; with EO LOW, O_0 to O_3 and \bar{O}_0 to \bar{O}_3 are in the high impedance OFF-state.

The device uses a common negative supply (V_{SS}) and separate positive supplies for inputs (V_{DDI}) and outputs (V_{DDO}). V_{DDI} must always be less than or equal to V_{DDO} , even during power turn-on and turn-off. For the permissible operating range of V_{DDI} and V_{DDO} see graph Fig. 4.

Each input protection circuit is terminated between V_{DDO} and V_{SS} . This allows the input signals to be driven from any potential between V_{DDO} and V_{SS} , without regard to current limiting. When driving from potentials greater than V_{DDO} or less than V_{SS} , the current at each input must be limited to 10 mA.



7274574.1



7273709.1

Fig. 2 Pinning diagram.

- HEF4104BP: 16-lead DIL; plastic (SOT-38Z).
- HEF4104BD: 16-lead DIL; ceramic (SOT-74).
- HEF4104BT: 16-lead flat pack; plastic (SO-16; SOT-109A).

PINNING

- I_0 to I_3 data inputs
- EO output enable input
- O_0 to O_3 data outputs
- \bar{O}_0 to \bar{O}_3 complementary data outputs

Fig. 1 Functional diagram.

FAMILY DATA

I_{DD} LIMITS category MSI

} see Family Specifications

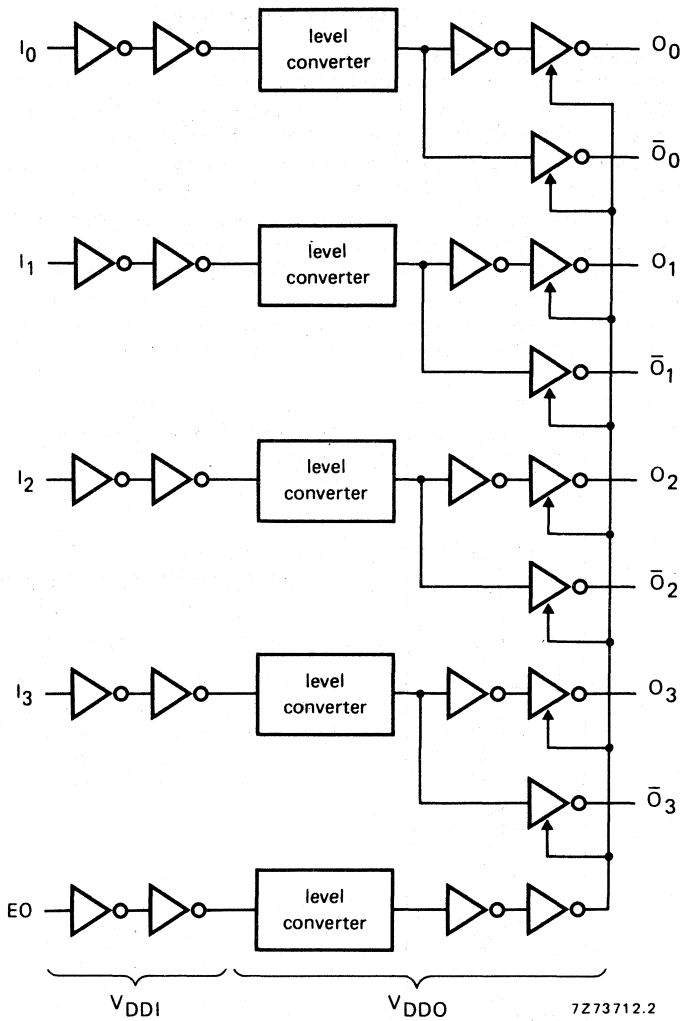


Fig. 3 Logic diagram.

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V _{DD} V	symbol	typ.	max.		typical extrapolation formula
Propagation delays I _n → O _n , \overline{O}_n HIGH to LOW	5	t _{PHL}	170	340	ns	143 ns + (0,55 ns/pF) C _L
	10		80	160	ns	69 ns + (0,23 ns/pF) C _L
	15		65	135	ns	57 ns + (0,16 ns/pF) C _L
LOW to HIGH	5	t _{PLH}	170	340	ns	143 ns + (0,55 ns/pF) C _L
	10		80	160	ns	69 ns + (0,23 ns/pF) C _L
	15		70	140	ns	62 ns + (0,16 ns/pF) C _L
Output transition times HIGH to LOW	5	t _{THL}	60	120	ns	10 ns + (1,0 ns/pF) C _L
	10		30	60	ns	9 ns + (0,42 ns/pF) C _L
	15		20	40	ns	6 ns + (0,28 ns/pF) C _L
LOW to HIGH	5	t _{TLH}	60	120	ns	10 ns + (1,0 ns/pF) C _L
	10		30	60	ns	9 ns + (0,42 ns/pF) C _L
	15		20	40	ns	6 ns + (0,28 ns/pF) C _L
3-state propagation delays						
Output disable times EO → O _n , \overline{O}_n HIGH	5	t _{PHZ}	70	135	ns	
	10		55	110	ns	
	15		60	120	ns	
LOW	5	t _{PLZ}	70	135	ns	
	10		55	105	ns	
	15		55	110	ns	
Output enable times EO → O _n , \overline{O}_n HIGH	5	t _{PZH}	195	395	ns	
	10		95	195	ns	
	15		80	165	ns	
LOW	5	t _{PZL}	195	395	ns	
	10		95	190	ns	
	15		80	160	ns	

	V _{DD} V	typical formula for P (μW)	where f _i = input freq. (MHz) f _o = output freq. (MHz) C _L = load capacitance (pF) Σ(f _o C _L) = sum of outputs V _{DD} = supply voltage (V)
Dynamic power dissipation per package (P)	5	3 000 f _i + Σ(f _o C _L) × V _{DD} ²	
	10	12 200 f _i + Σ(f _o C _L) × V _{DD} ²	
	15	31 000 f _i + Σ(f _o C _L) × V _{DD} ²	

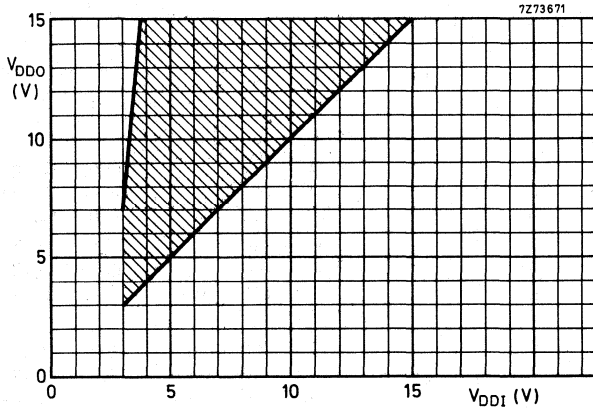


Fig. 4 V_{DD0} as a function of V_{DD1} ; the shaded area shows the permissible operating range.

STROBED HEX INVERTER/BUFFER



The HEF4502B consists of six inverter/buffers with 3-state outputs. When the output enable input (\overline{EO}) is HIGH all six outputs (O_1 to O_6) are in the high impedance OFF-state. When the enable input (\overline{E}) is HIGH all six outputs are switched to LOW. The outputs have a 2-TTL load drive capability.

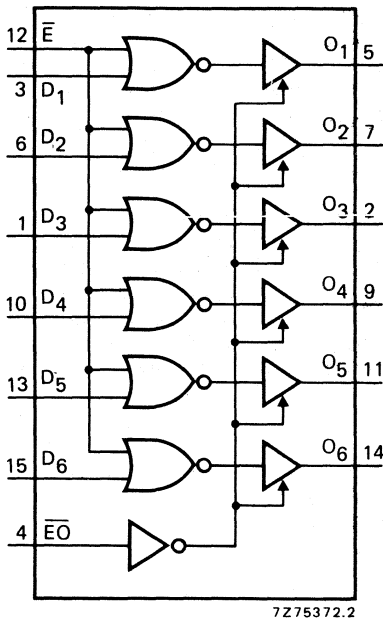


Fig. 1 Functional diagram.

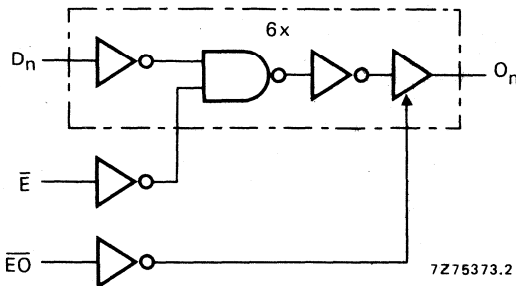


Fig. 3 Logic diagram.

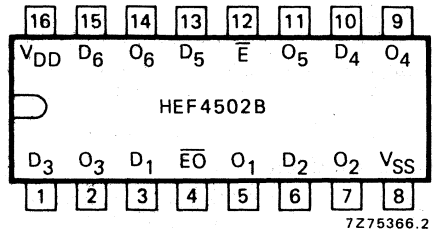


Fig. 2 Pinning diagram.

HEF4502BP : 16-lead DIL; plastic (SOT-38Z).
 HEF4502BD : 16-lead DIL; ceramic (SOT-74).
 HEF4502BT : 16-lead flat-pack; plastic (SO-16; SOT-109A).

PINNING

D_1 to D_6 data inputs
 \overline{E} enable input
 \overline{EO} output enable input
 O_1 to O_6 3-state outputs

TRUTH TABLE

inputs			output
D_n	\overline{E}	\overline{EO}	O_n
L	L	L	H
H	L	L	L
X	H	L	L
X	X	H	Z

H = HIGH state (the more pos. voltage)
 L = LOW state (the less pos. voltage)
 X = state is immaterial
 Z = high impedance off state

FAMILY DATA

I_{DD} LIMITS category BUFFERS

see Family Specifications

D.C. CHARACTERISTICS

V_{SS} = 0 V

	V _{DD} V	V _{OH} V	V _{OL} V	symbol	T _{amb} (°C)						
					-40		+ 25		+ 85		mA
					min.	max.	min.	max.	min.	max.	
Output current HIGH	5	4,6		-I _{OH}	1,2		1,0		0,8		
	10	9,5			3,8		3,2		2,5		
	15	13,5			12,0		10,0		8,0		
Output current HIGH	5	2,5		-I _{OH}	3,8		3,2		2,5		
Output current LOW	4,75		0,4	I _{OL}	3,5		2,9		2,3		
	10		0,5		12,0		10,0		8,0		
	15		1,5		24,0		20,0		16,0		

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ≤ 20 ns

	V _{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	5 000 f _i + Σ(f _o C _L) × V _{DD} ²	f _i = output freq. (MHz)
	10	25 000 f _i + Σ(f _o C _L) × V _{DD} ²	f _o = output freq. (MHz)
	15	85 000 f _i + Σ(f _o C _L) × V _{DD} ²	C _L = load capacitance (pF)
			Σ(f _o C _L) = sum of outputs
			V _{DD} = supply voltage (V)

A.C. CHARACTERISTICS

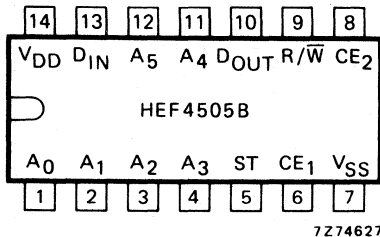
 $V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	symbol	typ.	max.	typical extrapolation formula
Propagation delays					
$D_n, \bar{E} \rightarrow O_n$	5		85	170 ns	$77\text{ ns} + (0,17\text{ ns/pF}) C_L$
HIGH to LOW	10	tPHL	40	80 ns	$37\text{ ns} + (0,06\text{ ns/pF}) C_L$
	15		35	70 ns	$33\text{ ns} + (0,04\text{ ns/pF}) C_L$
LOW to HIGH	5		80	160 ns	$66\text{ ns} + (0,28\text{ ns/pF}) C_L$
	10	tPLH	35	70 ns	$28\text{ ns} + (0,13\text{ ns/pF}) C_L$
	15		30	60 ns	$25\text{ ns} + (0,10\text{ ns/pF}) C_L$
Output transition times					
HIGH to LOW	5		25	50 ns	$10\text{ ns} + (0,30\text{ ns/pF}) C_L$
	10	tTHL	12	24 ns	$7\text{ ns} + (0,11\text{ ns/pF}) C_L$
	15		8	15 ns	$5\text{ ns} + (0,07\text{ ns/pF}) C_L$
LOW to HIGH	5		30	60 ns	$5\text{ ns} + (0,50\text{ ns/pF}) C_L$
	10	tTLH	15	30 ns	$3\text{ ns} + (0,24\text{ ns/pF}) C_L$
	15		12	24 ns	$3\text{ ns} + (0,18\text{ ns/pF}) C_L$
3-state propagation delays					
Output disable times					
$\bar{E}O \rightarrow O_n$	5		60	160 ns	
HIGH	10	tPHZ	55	140 ns	
	15		55	140 ns	
LOW	5		50	100 ns	
	10	tPLZ	35	70 ns	
	15		30	60 ns	
Output enable times					
$\bar{E}O \rightarrow O_n$	5		60	120 ns	
HIGH	10	tPZH	35	70 ns	
	15		30	60 ns	
LOW	5		55	110 ns	
	10	tPZL	25	50 ns	
	15		20	40 ns	

64-BIT, 1-BIT PER WORD RANDOM ACCESS READ/WRITE MEMORY



The HEF4505B is a 64-bit, 1-bit per word, fully decoded and completely static, random access memory. The memory is strobed for reading or writing only when the strobe input (ST), chip enable inputs (CE₁ and CE₂) are HIGH simultaneously. The output data is available at the data output (D_{OUT}) only when the memory is strobed, the read/write input (R/W) is HIGH and after the read access time has passed. Note that the three-state output is initially disabled and always goes to the LOW state before data is valid. The output is disabled in the high-impedance OFF-state, when the memory is not strobed or R/W is LOW. R/W may remain HIGH during a read cycle or LOW during a write cycle. The output data has the same polarity as the input data.



HEF4505BP: 14-lead DIL; plastic (SOT-27S, T, V).
HEF4505BD: 14-lead DIL; ceramic (SOT-73).

Fig. 1 Pinning diagram.

PINNING

A ₀ to A ₅	address inputs
CE ₁ , CE ₂	chip enable inputs
R/W	read/write input
ST	strobe input
D _{IN}	data input
D _{OUT}	data output

FUNCTION TABLE

ST, CE ₁ , CE ₂	R/W	D _{OUT}	mode
L	L	Z	disabled
H	L	Z	write
L	H	Z	disabled
H	H	equal to memory data	read

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

Z = high-impedance OFF-state

FAMILY DATA

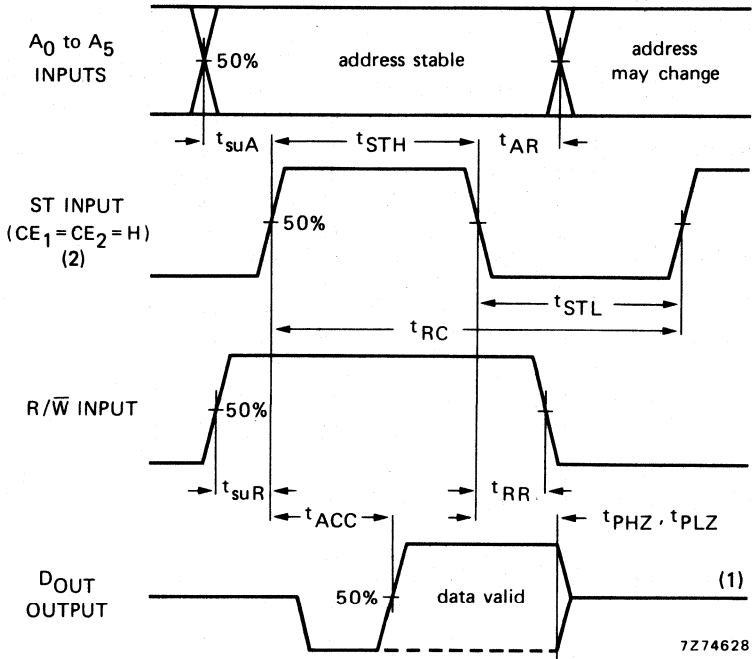
I_{DD} LIMITS category LSI

} see Family Specifications

A.C. CHARACTERISTICS

 $V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

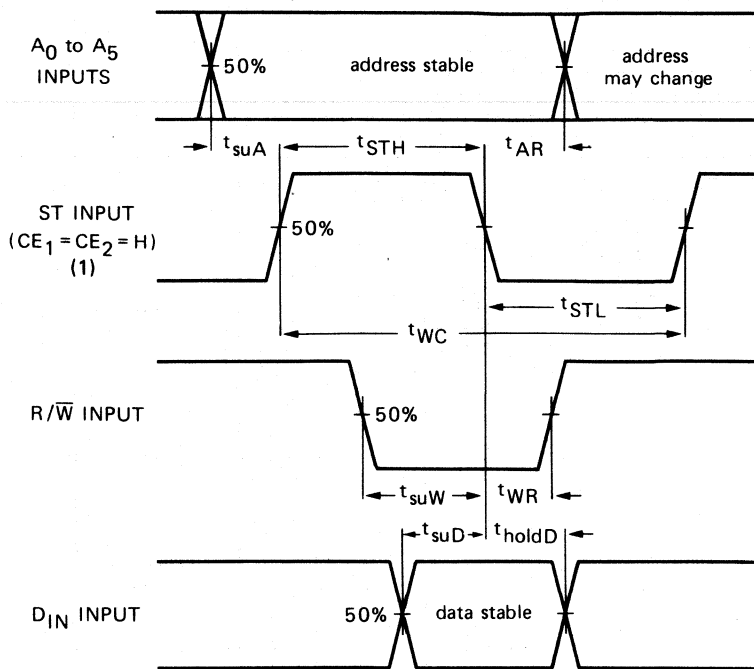
	V_{DD} V	symbol	min.	typ.	max.	typical extrapolation formula	
Minimum strobe pulse width; LOW	5	t_{STL}	75	35	ns		
	10		45	22	ns		
	15		30	15	ns		
Read cycle time	5	t_{RC}		350	700		ns
	10		250	500	ns		
	15		210	420	ns		
Write cycle time	5	t_{WC}		220	440		ns
	10		125	250	ns		
	15		75	150	ns		
Read access time	5	t_{ACC}		330	660		ns
	10		135	270	ns		
	15		100	200	ns		
Address recovery time	5	t_{AR}	80	40	ns		$303\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10		40	20	ns		$124\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15		25	10	ns		$92\text{ ns} + (0,16\text{ ns/pF}) C_L$
Read recovery time	5	t_{RR}	180	90	ns		
	10		120	60	ns		
	15		90	45	ns		
Write recovery time	5	t_{WR}	75	35	ns		
	10		45	25	ns		
	15		40	20	ns		
3-state propagation delays							
Output disable times	5	t_{PHZ} ,		105	210	ns	
	10	t_{PLZ}		60	125	ns	
	15			55	115	ns	
Set-up times $A_n \rightarrow ST$	5	t_{suA}	-20	-40	ns		
	10		-10	-20	ns		
	15		-5	-10	ns		
$R/\bar{W} \rightarrow ST$	5	t_{suR}	-30	-60	ns		
	10		-15	-30	ns		
	15		-5	-10	ns		
$D_{IN} \rightarrow ST$	5	t_{suD}	160	80	ns		
	10		75	35	ns		
	15		45	20	ns		
$R/\bar{W} \rightarrow ST$	5	t_{suW}	240	120	ns		
	10		100	50	ns		
	15		75	35	ns		
Hold time $D_{IN} \rightarrow ST$	5	t_{holdD}	-20	-40	ns		
	10		5	-10	ns		
	15		10	0	ns		



(1) Output in high impedance OFF-state.

(2) $t_{STHmin} = t_{RCmax} - t_{STLmin}$

Fig. 3 Read cycle timing diagram.

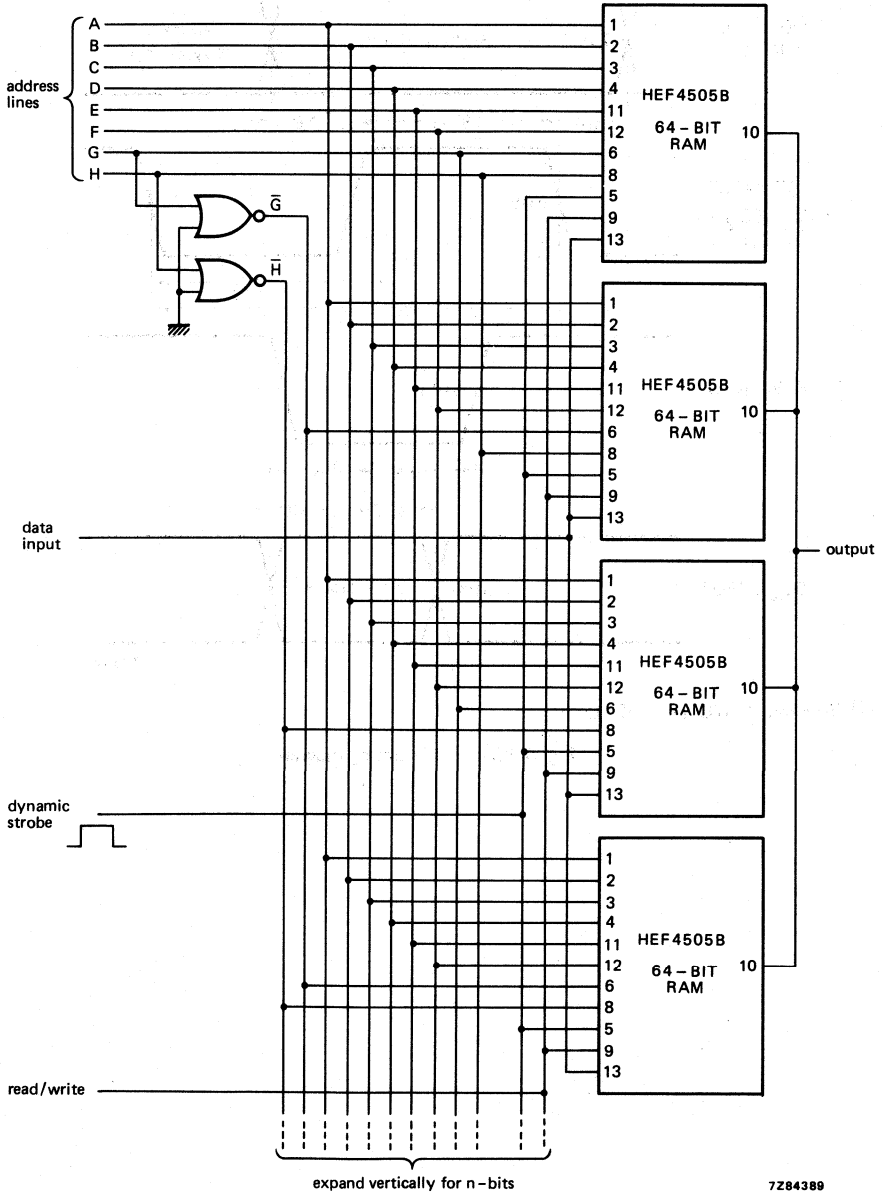


7274629

(1) $t_{STHmin} = t_{WCmax} - t_{STLmin}$

Fig. 4 Write cycle timing diagram.

APPLICATION INFORMATION



7284389

Fig. 5 256-word by n-bit static read/write memory using HEF4505B ICs.

Figure 5 shows a 256-word by n-bit static RAM system. The outputs of the four HEF4505B circuits are tied together to form 256 words by 1-bit. Additional bits are attained by paralleling the inputs in groups of four. Memories of larger words can be attained by decoding the most significant bits of the address and AND-ing them with the strobe input.

Fan-in and fan-out of the memory are limited only by speed requirements. The extremely low input and output leakage currents keep the output voltage levels from changing significantly as more outputs are tied together. With the output levels independent of fan-out, most of the power supply range is available as logic swing, regardless of the number of units wired together. As a result, high noise immunity is maintained under all conditions.

The memory system shown in Fig. 5 can be interfaced directly with other ICs of the LOCMOS HE family. No external components are required.

Non-volatile information storage is allowed due to very low power dissipation when the memory is powered by a small standby battery. Figure 6 shows an optional standby power supply circuit for making a LOCMOS memory 'non-volatile'. When the usual power fails, a battery is used to sustain operation or maintain stored information. While normal power supply voltage is present, the battery is trickle-charged through a resistor (R) which sets the charging rate. In Fig. 6 the sustaining voltage is V_B , and +V is the ordinary voltage from a power supply. V_{DD} is connected to the power supply pin of the memory. Low-leakage diodes are recommended to conserve battery power.

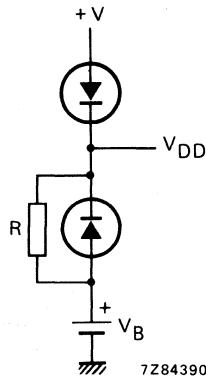


Fig. 6 Standby battery circuit.



DUAL 4-BIT LATCH

The HEF4508B is a dual 4-bit latch, which consists of two identical independent 4-bit latches with separate strobe (ST), master reset (MR), output-enable input (\overline{EO}) and 3-state outputs (O).

With the ST input in the HIGH state, the data on the D inputs appear at the corresponding outputs provided \overline{EO} is LOW. Changing the ST input to the LOW state locks the data into the latch. A HIGH on the reset line forces the outputs to a LOW level regardless of the state of the ST input. The 3-state outputs are controlled by the output-enable input. A HIGH on \overline{EO} causes the outputs to assume a high impedance OFF-state regardless of other input conditions. This allows the outputs to interface directly with bus orientated systems. When \overline{EO} is LOW the contents of the latches are available at the outputs.

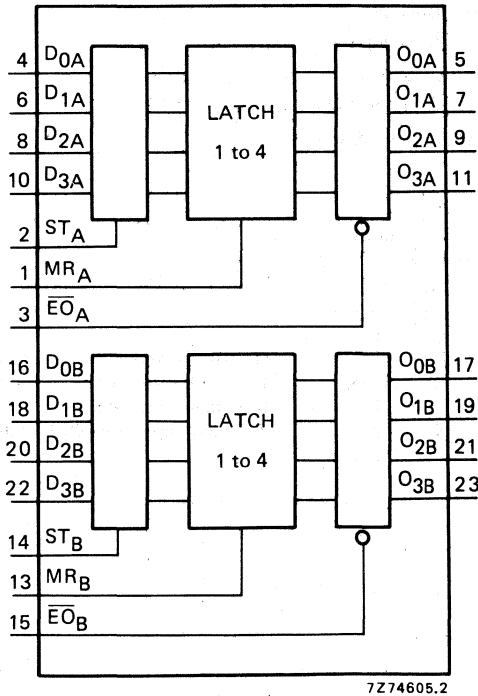
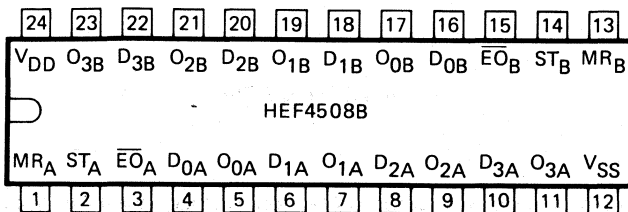


Fig. 1 Functional diagram.

FAMILY DATA

I_{DD} LIMITS category MSI

} see Family Specifications



7274604.2

Fig. 2 Pinning diagram.

HEF4508BP: 24-lead DIL; plastic (SOT-101A).

HEF4508BD: 24-lead DIL; ceramic (SOT-94).

PINNING

- D_{0A} to D_{3A}, D₀₃ to D_{3B} data inputs
- ST_A, ST_B strobe inputs
- MR_A, MR_B master reset inputs
- $\overline{E}O_A$, $\overline{E}O_B$ output enable inputs
- O_{0A} to O_{3A}, O_{0B} to O_{3B} 3-state outputs

FUNCTION TABLE

inputs				output
MR	ST	$\overline{E}O$	D _n	O _n
L	H	L	H	H
L	H	L	L	L
L	L	L	X	latched
H	X	L	X	L
X	X	H	X	Z

H = HIGH state (the more positive voltage)
 L = LOW state (the less positive voltage)
 X = state is immaterial
 Z = high impedance OFF state

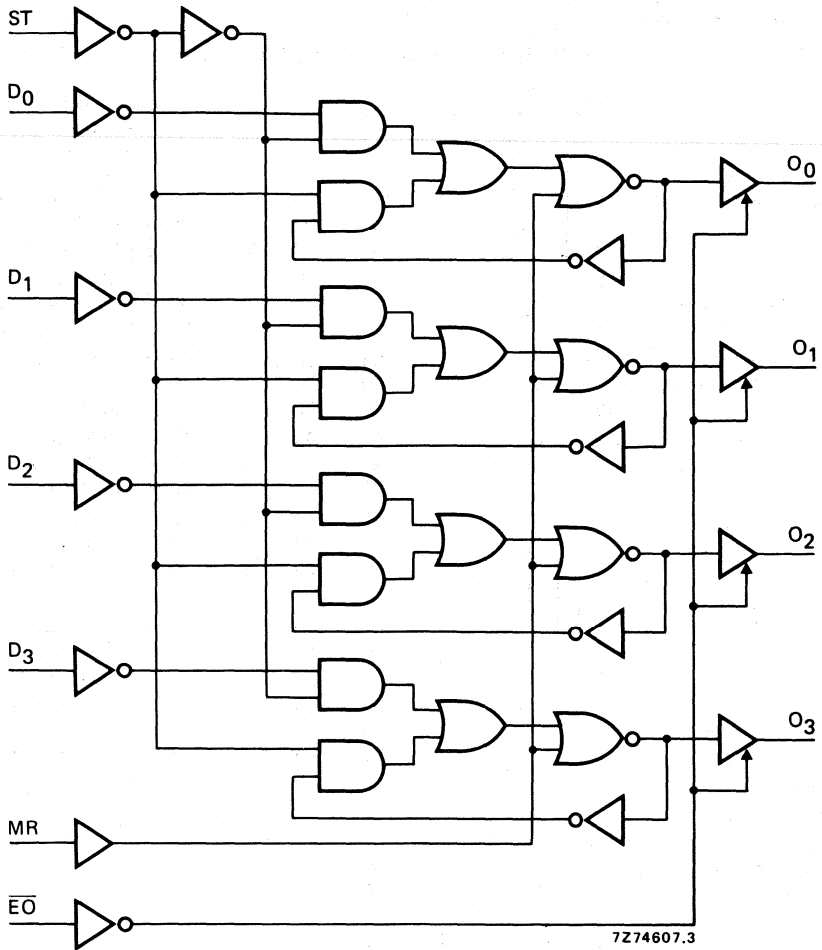


Fig. 3 Logic diagram (one 4-bit latch).



A.C. CHARACTERISTICS

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^\circ\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$; see also waveforms Fig. 4.

	V_{DD} V	symbol	min.	typ.	max.	typical extrapolation formula	
Propagation delays							
ST \rightarrow O_n HIGH to LOW	5			115	230	ns	$88\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10	tPHL		50	100	ns	$39\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			35	70	ns	$27\text{ ns} + (0,16\text{ ns/pF}) C_L$
5				115	230	ns	$88\text{ ns} + (0,55\text{ ns/pF}) C_L$
LOW to HIGH	10	tPLH		50	100	ns	$39\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			35	70	ns	$27\text{ ns} + (0,16\text{ ns/pF}) C_L$
	5				95	190	ns
$D_n \rightarrow O_n$ HIGH to LOW	10	tPHL		40	80	ns	$29\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			30	60	ns	$22\text{ ns} + (0,16\text{ ns/pF}) C_L$
	5				95	190	ns
LOW to HIGH	10	tPLH		40	80	ns	$29\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			30	60	ns	$22\text{ ns} + (0,16\text{ ns/pF}) C_L$
	5				100	200	ns
MR $\rightarrow O_n$ HIGH to LOW	10	tPHL		40	80	ns	$29\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			30	60	ns	$22\text{ ns} + (0,16\text{ ns/pF}) C_L$
	Output transition times						
HIGH to LOW	5			60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$
	10	tTHL		30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$
	15			20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$
5				60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$
LOW to HIGH	10	tTLH		30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$
	15			20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$
	3-state propagation delays						
Output enable times							
$\overline{E}O \rightarrow O_n$ HIGH	5			45	90	ns	
	10	tPZH		20	40	ns	
	15			18	36	ns	
5				45	90	ns	
LOW	10	tPZL		20	40	ns	
	15			18	36	ns	
	Output disable times						
$\overline{E}O \rightarrow O_n$ HIGH	5			35	70	ns	
	10	tPHZ		20	40	ns	
	15			18	36	ns	
5				45	90	ns	
LOW	10	tPLZ		20	40	ns	
	15			18	36	ns	

A.C. CHARACTERISTICS

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	symbol	min.	typ.	max.	
Minimum ST pulse width; HIGH	5	t_{WSTH}	50	25	ns	} see also waveforms Fig. 4
	10		30	15	ns	
	15		20	10	ns	
Minimum MR pulse width; HIGH	5	t_{WMRH}	40	20	ns	
	10		24	12	ns	
	15		20	10	ns	
Recovery time for MR	5	t_{RMR}	20	0	ns	
	10		20	0	ns	
	15		15	0	ns	
Set-up times $D_n \rightarrow ST$	5	t_{su}	35	10	ns	
	10		25	5	ns	
	15		20	0	ns	
Hold times $D_n \rightarrow ST$	5	t_{hold}	20	0	ns	
	10		20	0	ns	
	15		15	0	ns	

	V_{DD} V	typical formula for P (μW)	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
Dynamic power dissipation per package (P)	5	$2\,000 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	10		
	15		

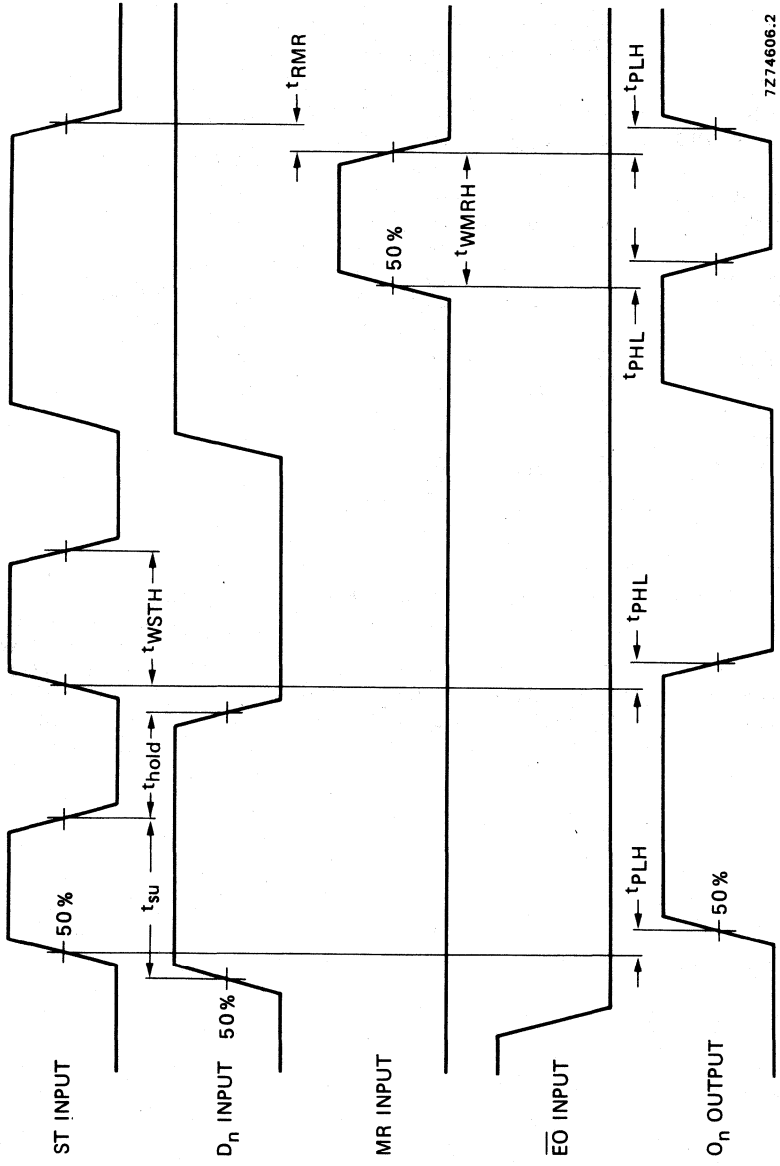


Fig. 4 Waveforms showing minimum ST and MR pulse widths, set-up and hold times for D_n to ST, recovery time for MR and propagation delays from ST to O_n, D_n to O_n and MR to O_n.

APPLICATION INFORMATION

Some examples of application for the HEF4508B are:

- Buffer storage
- Holding registers
- Data storage and multiplexing

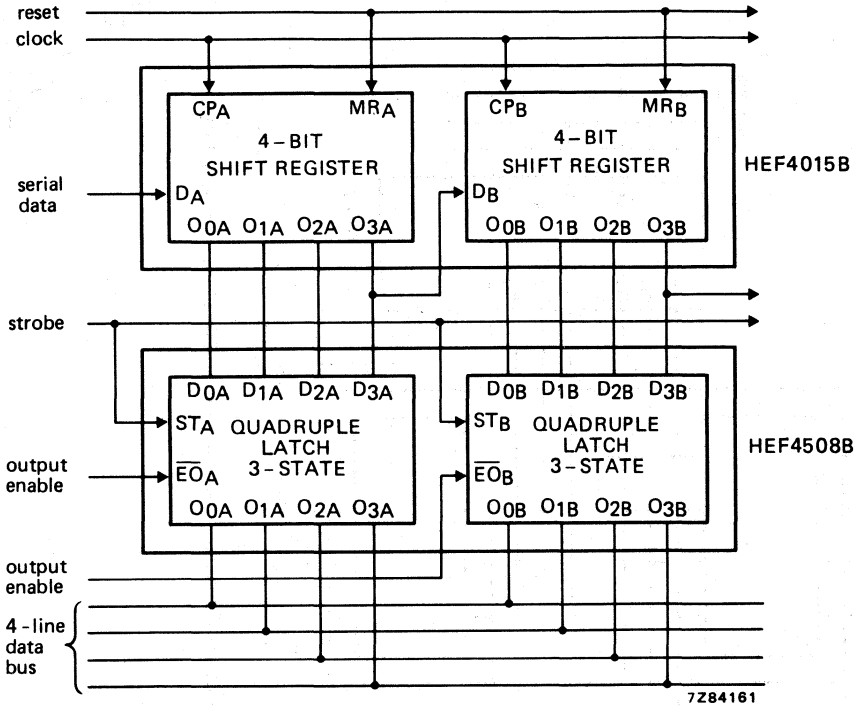


Fig. 5 Example of a bus register using HEF4508B and HEF4015B.

APPLICATION INFORMATION (continued)

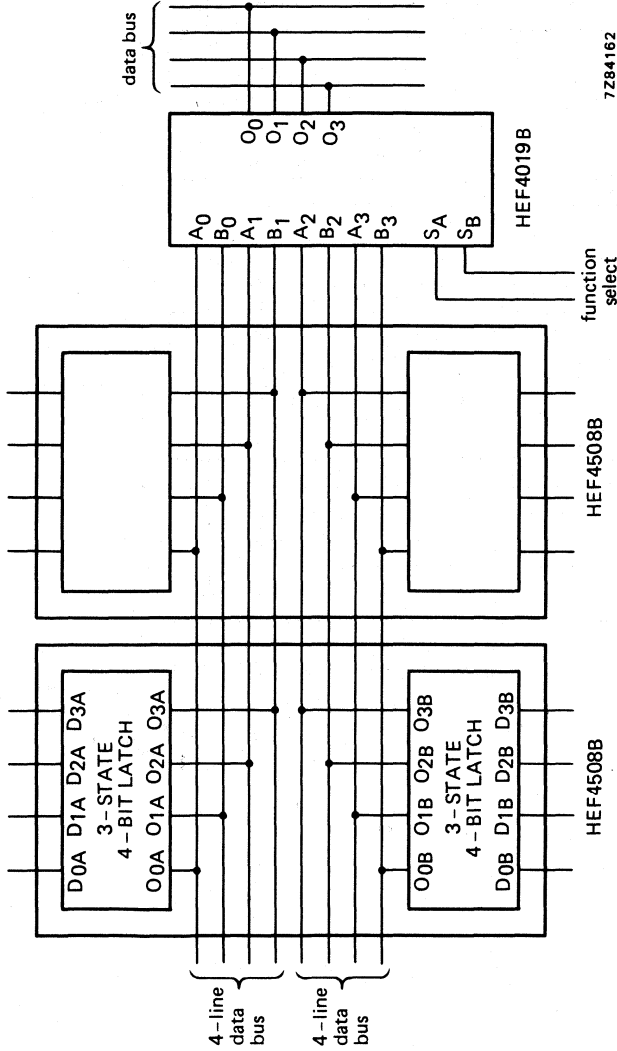


Fig. 6 Example of a dual multiplexed bus register with function select using two HEF4508B and one HEF4019B.

FUNCTION SELECT

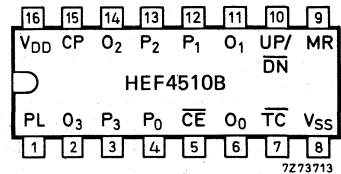
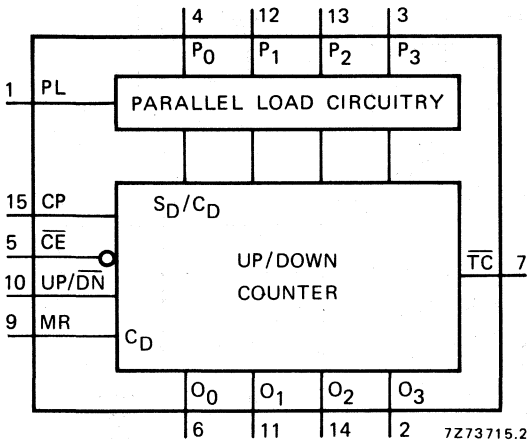
SA	SB	function
L	L	inhibit (all L)
H	L	select A bus
L	H	select B bus
H	H	A ₁ + B ₁



BCD UP/DOWN COUNTER

The HEF4510B is an edge-triggered synchronous up/down BCD counter with a clock input (CP), an up/down count control input (UP/ $\overline{\text{DN}}$), an active LOW count enable input ($\overline{\text{CE}}$), an asynchronous active HIGH parallel load input (PL), four parallel inputs (P_0 to P_3), four parallel outputs (O_0 to O_3), an active LOW terminal count output ($\overline{\text{TC}}$), and an overriding asynchronous master reset input (MR).

Information on P_0 to P_3 is loaded into the counter while PL is HIGH, independent of all other input conditions except the MR input, which must be LOW. With PL LOW, the counter changes on the LOW to HIGH transition of CP if $\overline{\text{CE}}$ is LOW. UP/ $\overline{\text{DN}}$ determines the direction of the count, HIGH for counting up, LOW for counting down. When counting up, $\overline{\text{TC}}$ is LOW when O_0 and O_3 are HIGH and $\overline{\text{CE}}$ is LOW. When counting down, $\overline{\text{TC}}$ is LOW when O_0 to O_3 and $\overline{\text{CE}}$ are LOW. A HIGH on MR resets the counter (O_0 to $O_3 = \text{LOW}$) independent of all other input conditions.



- HEF4510BP: 16-lead DIL; plastic (SOT-38Z).
- HEF4510BD: 16-lead DIL; ceramic (SOT-74).
- HEF4510BT: 16-lead flat pack; plastic (SO-16; SOT-109A).

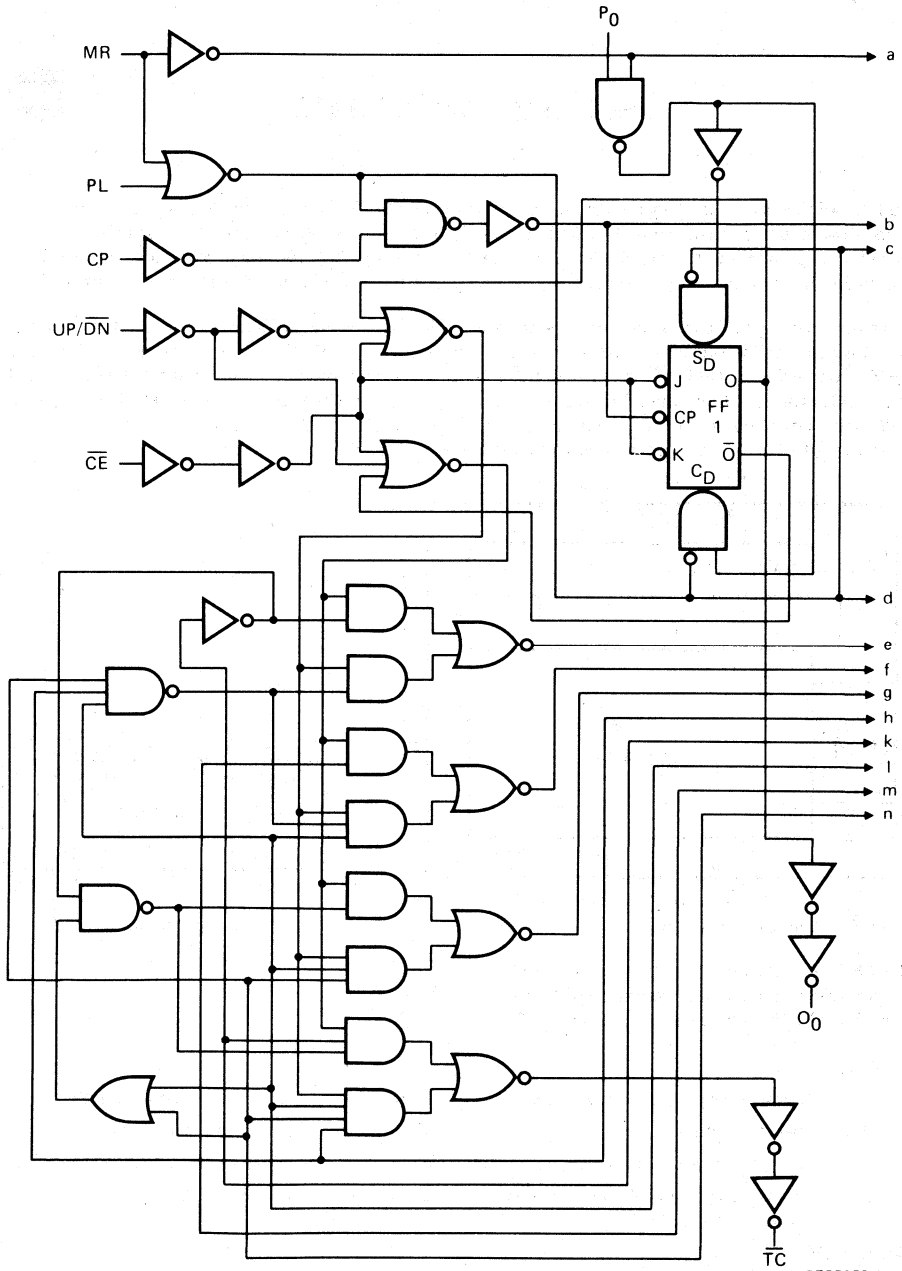
PINNING

PL	parallel load input (active HIGH)	UP/ $\overline{\text{DN}}$	up/down count control input
P_0 to P_3	parallel inputs	MR	master reset input
$\overline{\text{CE}}$	count enable input (active LOW)	$\overline{\text{TC}}$	terminal count output (active LOW)
CP	clock pulse input (LOW to HIGH, edge triggered)	O_0 to O_3	parallel outputs

FAMILY DATA

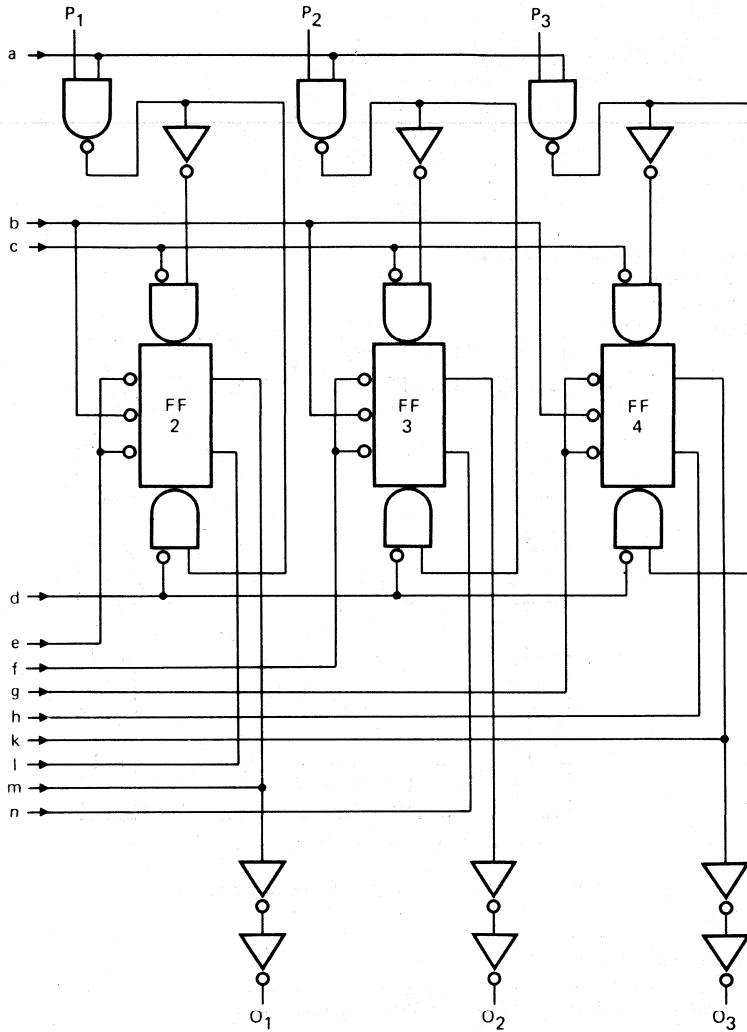
I_{DD} LIMITS category MSI

see Family Specifications



7275079.1

Fig. 3a Logic diagram (continued in Fig. 3b).



7275080.1

Fig. 3b Logic diagram (continued from Fig. 3a).

FUNCTION TABLE

MR	PL	UP/DN	CE	CP	mode
L	H	X	X	X	parallel load
L	L	X	H	X	no change
L	L	L	L	/	count down
L	L	H	L	/	count up
H	X	X	X	X	reset

H = HIGH state (the more positive voltage)
 L = LOW state (the less positive voltage)
 X = state is immaterial
 / = positive-going transition

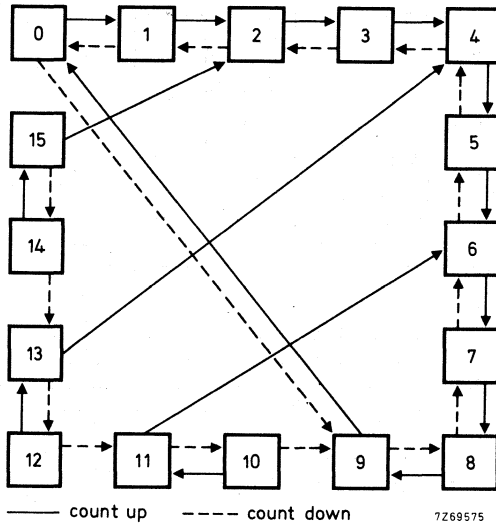


Fig. 4 State diagram.

Logic equation for terminal count:

$$TC = \overline{CE} \cdot \{ (UP/DN) \cdot O_0 \cdot O_3 + (UP/DN) \cdot \overline{O_0} \cdot \overline{O_1} \cdot \overline{O_2} \cdot O_3 \}$$

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ≤ 20 ns

	V _{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	1000 f _i + Σ(f _o C _L) × V _{DD} ²	f _i = input freq. (MHz)
	10	4500 f _i + Σ(f _o C _L) × V _{DD} ²	f _o = output freq. (MHz)
	15	11 200 f _i + Σ(f _o C _L) × V _{DD} ²	C _L = load capacitance (pF)
			Σ(f _o C _L) = sum of outputs
			V _{DD} = supply voltage (V)

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V _{DD} V	symbol	min.	typ.	max.	typical extrapolation formula
Propagation delays CP → O _n HIGH to LOW	5	t _{PHL}		145	290 ns	118 ns + (0,55 ns/pF) C _L
	10		60	120 ns	49 ns + (0,23 ns/pF) C _L	
	15		45	90 ns	37 ns + (0,16 ns/pF) C _L	
LOW to HIGH	5	t _{PLH}		155	310 ns	128 ns + (0,55 ns/pF) C _L
	10		65	130 ns	54 ns + (0,23 ns/pF) C _L	
	15		45	90 ns	37 ns + (0,16 ns/pF) C _L	
CP → \overline{TC} HIGH to LOW	5	t _{PHL}		260	525 ns	233 ns + (0,55 ns/pF) C _L
	10		105	210 ns	94 ns + (0,23 ns/pF) C _L	
	15		75	150 ns	67 ns + (0,16 ns/pF) C _L	
LOW to HIGH	5	t _{PLH}		180	360 ns	153 ns + (0,55 ns/pF) C _L
	10		75	150 ns	64 ns + (0,23 ns/pF) C _L	
	15		55	115 ns	47 ns + (0,16 ns/pF) C _L	
PL → O _n HIGH to LOW	5	t _{PHL}		125	255 ns	98 ns + (0,55 ns/pF) C _L
	10		55	110 ns	44 ns + (0,23 ns/pF) C _L	
	15		40	85 ns	32 ns + (0,16 ns/pF) C _L	
LOW to HIGH	5	t _{PLH}		170	340 ns	143 ns + (0,55 ns/pF) C _L
	10		70	140 ns	59 ns + (0,23 ns/pF) C _L	
	15		50	105 ns	42 ns + (0,16 ns/pF) C _L	
PL → \overline{TC} HIGH to LOW	5	t _{PHL}		250	500 ns	223 ns + (0,55 ns/pF) C _L
	10		110	220 ns	99 ns + (0,23 ns/pF) C _L	
	15		80	160 ns	72 ns + (0,16 ns/pF) C _L	
LOW to HIGH	5	t _{PLH}		250	500 ns	223 ns + (0,55 ns/pF) C _L
	10		110	220 ns	99 ns + (0,23 ns/pF) C _L	
	15		80	160 ns	72 ns + (0,16 ns/pF) C _L	
\overline{CE} → \overline{TC} HIGH to LOW	5	t _{PHL}		165	330 ns	138 ns + (0,55 ns/pF) C _L
	10		65	135 ns	54 ns + (0,23 ns/pF) C _L	
	15		50	100 ns	42 ns + (0,16 ns/pF) C _L	
LOW to HIGH	5	t _{PLH}		145	290 ns	118 ns + (0,55 ns/pF) C _L
	10		60	125 ns	49 ns + (0,23 ns/pF) C _L	
	15		45	95 ns	37 ns + (0,16 ns/pF) C _L	
MR → O _n , \overline{TC} HIGH to LOW	5	t _{PHL}		205	405 ns	178 ns + (0,55 ns/pF) C _L
	10		65	130 ns	54 ns + (0,23 ns/pF) C _L	
	15		45	85 ns	37 ns + (0,16 ns/pF) C _L	
MR → \overline{TC} LOW to HIGH	5	t _{PLH}		225	450 ns	198 ns + (0,55 ns/pF) C _L
	10		75	150 ns	64 ns + (0,23 ns/pF) C _L	
	15		50	100 ns	42 ns + (0,16 ns/pF) C _L	

A.C. CHARACTERISTICS

 $V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	symbol	min.	typ.	max.	typical extrapolation formula
Output transition times HIGH to LOW	5	t_{THL}		60	120 ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$
	10			30	60 ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$
	15			20	40 ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$
LOW to HIGH	5	t_{TLH}		60	120 ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$
	10			30	60 ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$
	15			20	40 ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$
Minimum clock pulse width; LOW	5	t_{WCPL}	95	45	ns	
	10		35	20	ns	
	15		25	15	ns	
Minimum PL pulse width; HIGH	5	t_{WPLH}	105	55	ns	
	10		45	25	ns	
	15		35	15	ns	
Minimum MR pulse width; HIGH	5	t_{WMRH}	120	60	ns	
	10		50	25	ns	
	15		40	20	ns	
Recovery time for MR	5	t_{RMR}	130	65	ns	
	10		45	20	ns	
	15		30	15	ns	
Recovery time for PL	5	t_{RPL}	150	75	ns	
	10		50	25	ns	
	15		30	15	ns	
Set-up times $P_n \rightarrow PL$	5	t_{su}	100	50	ns	see also waveforms Figs 5 and 6
	10		50	25	ns	
	15		40	20	ns	
$UP/\overline{DN} \rightarrow CP$	5	t_{su}	250	125	ns	
	10		100	50	ns	
	15		75	35	ns	
$\overline{CE} \rightarrow PL$	5	t_{su}	120	60	ns	
	10		40	20	ns	
	15		25	10	ns	
Hold times $P_n \rightarrow PL$	5	t_{hold}	10	-40	ns	
	10		5	-20	ns	
	15		0	-20	ns	
$UP/\overline{DN} \rightarrow CP$	5	t_{hold}	35	-90	ns	
	10		15	-35	ns	
	15		15	-25	ns	
$\overline{CE} \rightarrow CP$	5	t_{hold}	20	-40	ns	
	10		5	-15	ns	
	15		5	-10	ns	
Maximum clock pulse frequency	5	f_{max}	5	10	MHz	
	10		12	24	MHz	
	15		17	34	MHz	

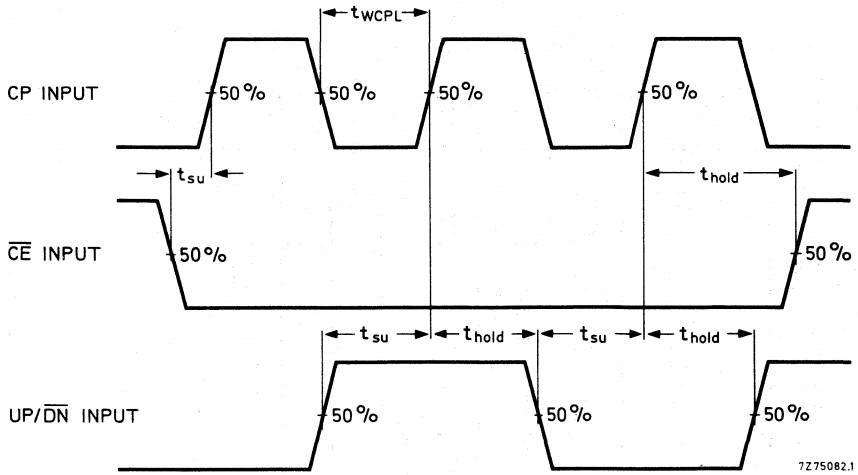


Fig. 5 Waveforms showing minimum pulse width for CP, set-up and hold times for \overline{CE} to CP and UP/ \overline{DN} to CP.

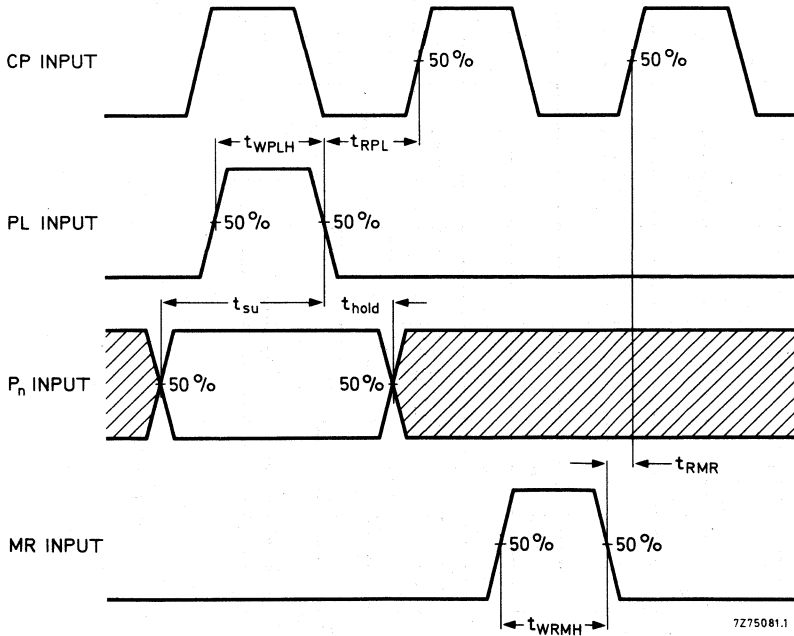


Fig. 6 Waveforms showing minimum pulse width for PL and MR, recovery time for PL and MR and set-up and hold times for P_n to PL.

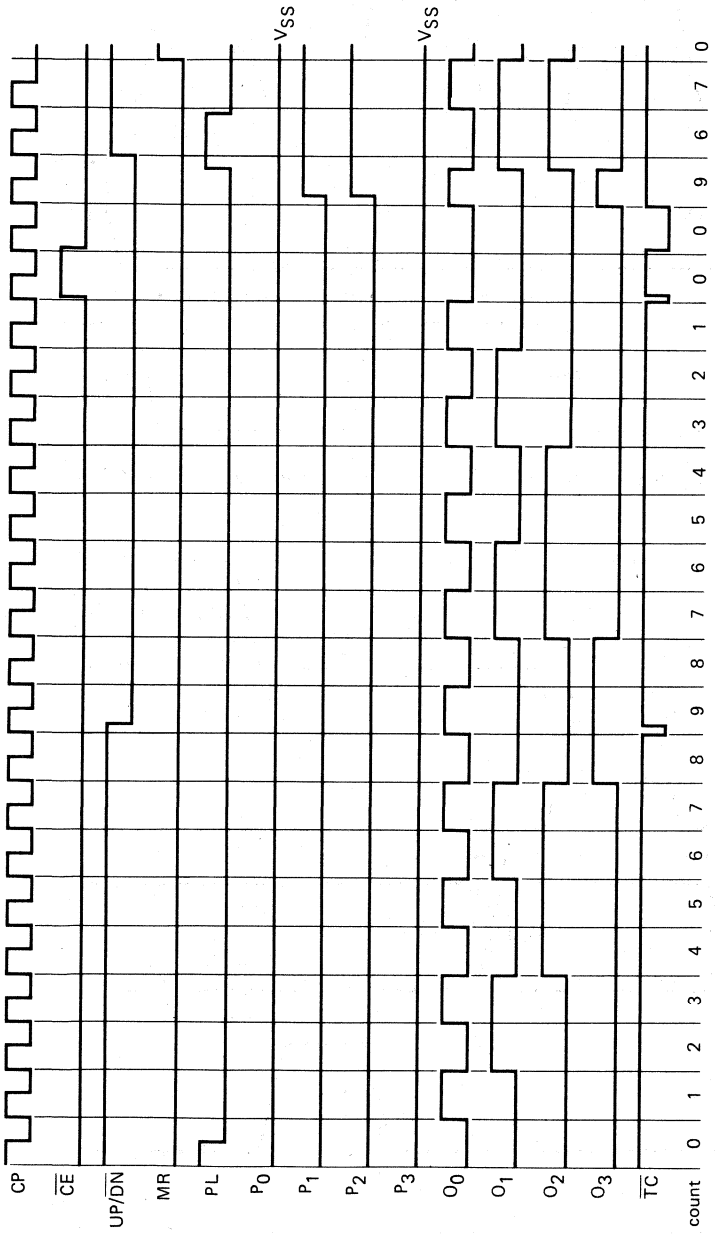


Fig. 7 Timing diagram.

APPLICATION INFORMATION

Some examples of applications for the HEF4510B are:

- Up/down difference counting
- Synchronous frequency dividers

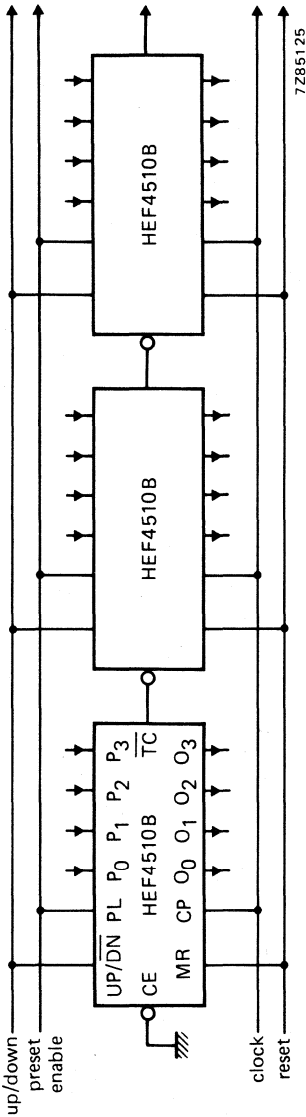


Fig. 8 Example of parallel clocking when cascading HEF4510B ICs.

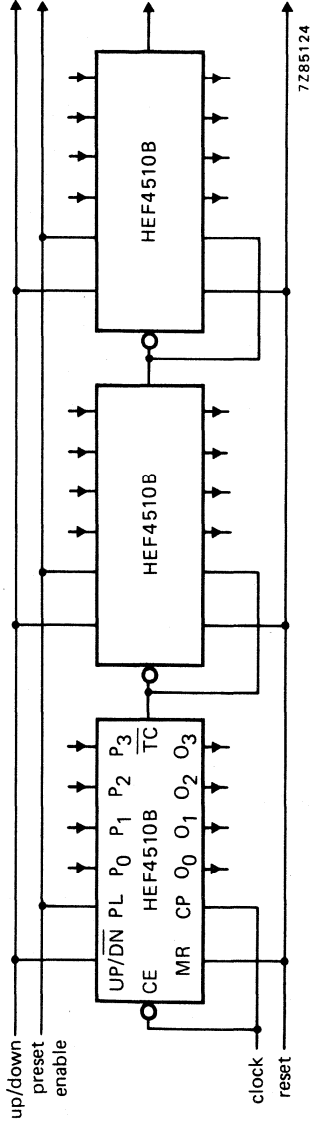


Fig. 9 Example of ripple clocking when cascading HEF4510B ICs. Ripple clocking mode: the up/down control can be changed at any count; the only restriction on changing the up/down control is that the clock input to the first counting stage must be HIGH.

BCD TO 7-SEGMENT LATCH/DECODER/DRIVER



The HEF4511B is a BCD to 7-segment latch/decoder/driver with four address inputs (D_A to D_D), an active LOW latch enable input (\overline{EL}), an active LOW ripple blanking input (\overline{BI}), an active LOW lamp test input (\overline{LT}), and seven active HIGH n-p-n bipolar transistor segment outputs (O_a to O_g).

When \overline{EL} is LOW, the state of the segment outputs (O_a to O_g) is determined by the data on D_A to D_D . When \overline{EL} goes HIGH, the last data present on D_A to D_D are stored in the latches and the segment outputs remain stable. When \overline{LT} is LOW, all the segment outputs are HIGH independent of all other input conditions. With \overline{LT} HIGH, a LOW on \overline{BI} forces all segment outputs LOW. The inputs \overline{LT} and \overline{BI} do not affect the latch circuit.

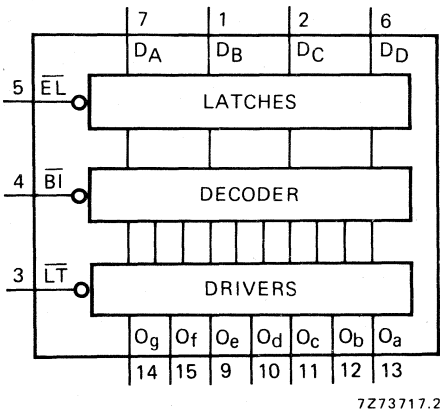


Fig. 1 Functional diagram.

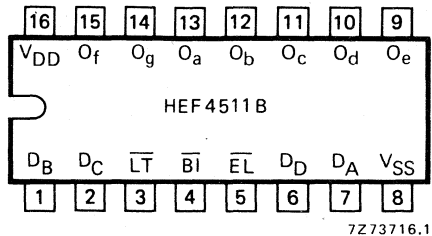


Fig. 2 Pinning diagram.

HEF4511BP: 16-lead DIL; plastic (SOT-38Z).
HEF4511BD: 16-lead DIL; ceramic (SOT-74).
HEF4511BT: 16-lead flat pack; plastic (SO-16; SOT-109A).

PINNING

- D_A to D_D address (data) inputs
- \overline{EL} latch enable input (active LOW)
- \overline{BI} ripple blanking input (active LOW)
- \overline{LT} lamp test input (active LOW)
- O_a to O_g segment outputs

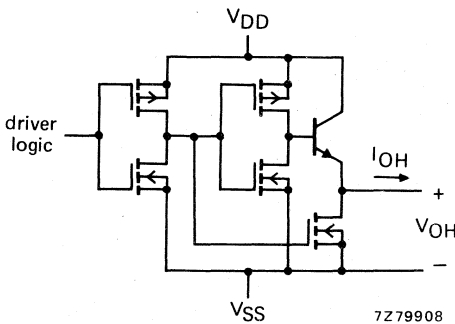


Fig. 3 Schematic diagram of output stage.

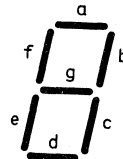
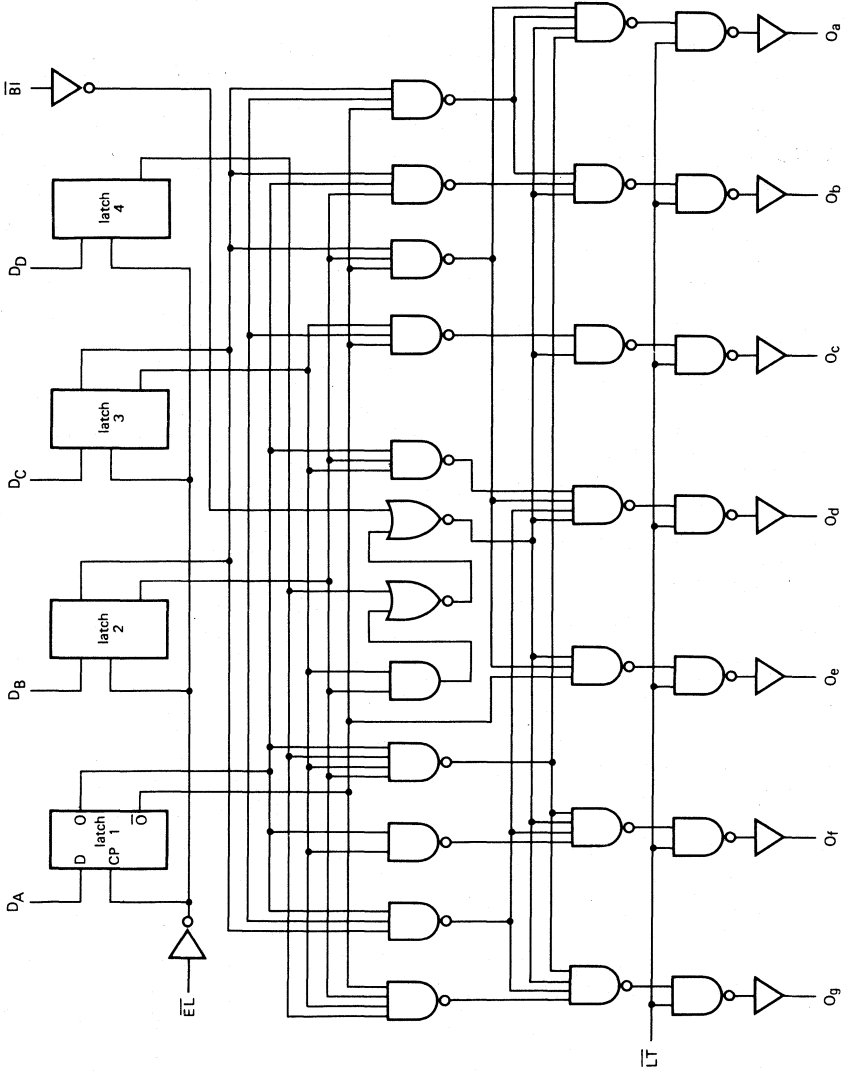


Fig. 4 Segment designation.

FAMILY DATA

I_{DD} LIMITS category MSI

} see Family Specifications



7274585.1

Fig. 5 Logic diagram; for one latch see Fig. 6.

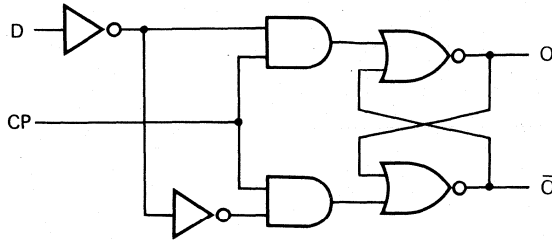


Fig. 6 Logic diagram (one latch); see also Fig. 5. 7Z79901

FUNCTION TABLE

inputs				outputs										display
\overline{EL}	\overline{BI}	\overline{LT}	D_D	D_C	D_B	D_A	O_a	O_b	O_c	O_d	O_e	O_f	O_g	
X	X	L	X	X	X	X	H	H	H	H	H	H	H	8
X	L	H	X	X	X	X	L	L	L	L	L	L	L	blank
L	H	H	L	L	L	L	H	H	H	H	H	H	L	0
L	H	H	L	L	L	H	L	H	H	L	L	L	L	1
L	H	H	L	L	H	L	H	H	L	H	H	L	H	2
L	H	H	L	L	H	H	H	H	H	H	L	L	H	3
L	H	H	L	H	L	L	L	H	H	L	L	H	H	4
L	H	H	L	H	L	H	H	L	H	H	L	H	H	5
L	H	H	L	H	H	L	L	L	H	H	H	H	H	6
L	H	H	L	H	H	H	H	H	H	L	L	L	L	7
L	H	H	H	L	L	L	H	H	H	H	H	H	H	8
L	H	H	H	L	L	H	H	H	L	L	L	H	H	9
L	H	H	H	L	H	L	L	L	L	L	L	L	L	blank
L	H	H	H	L	H	H	L	L	L	L	L	L	L	blank
L	H	H	H	H	L	L	L	L	L	L	L	L	L	blank
L	H	H	H	H	H	L	L	L	L	L	L	L	L	blank
L	H	H	H	H	H	H	L	L	L	L	L	L	L	blank
H	H	H	X	X	X	X	L	L	L	L	L	L	L	*

H = HIGH state (the more positive voltage)
 L = LOW state (the less positive voltage)
 X = state is immaterial

* Depends upon the BCD code applied during the LOW to HIGH transition of \overline{EL} .

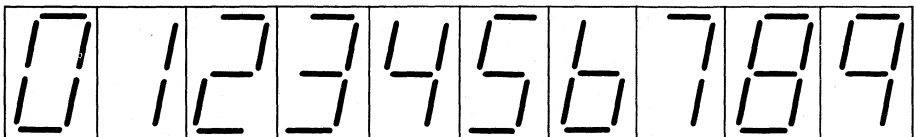


Fig. 7 Display.

7Z72856

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134).

Output (source) current HIGH

$-I_{OH}$ max. 25 mA

For other RATINGS see Family Specifications.

Note

A destructive high current mode may occur if V_I and V_O are not constrained to the range $V_{SS} \leq V_I$ or $V_O \leq V_{DD}$.

D.C. CHARACTERISTICS

$V_{SS} = 0$ V

	V_{DD} V	I_{OH} mA	symbol	T_{amb} ($^{\circ}C$)					
				-40		+25		+85	
				min.	max.	min.	typ.	min.	max.
Output voltage HIGH	5	0	V_{OH}	4,10		4,10	4,40	4,10	
	10	0		9,10		9,10	9,40	9,10	
	15	0		14,10		14,10	14,40	14,10	
Output voltage HIGH	5	5	V_{OH}				4,30		
	10	5					9,30		
	15	5					14,30		
Output voltage HIGH	5	10	V_{OH}	3,60		3,60	4,25	3,30	
	10	10		8,75		8,75	9,25	8,45	
	15	10		13,75		13,75	14,25	13,45	
Output voltage HIGH	5	15	V_{OH}				4,20		
	10	15					9,20		
	15	15					14,20		
Output voltage HIGH	5	20	V_{OH}	2,80		2,80	4,20	2,50	
	10	20		8,10		8,10	9,20	7,80	
	15	20		13,10		13,10	14,20	12,80	
Output voltage HIGH	5	25	V_{OH}				4,15		
	10	25					9,20		
	15	25					14,20		

A.C. CHARACTERISTICS

$V_{SS} = 0$ V; $T_{amb} = 25$ $^{\circ}C$; input transition times ≤ 20 ns

	V_{DD} V	typical formula for P (μW)	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
Dynamic power dissipation per package (P)	5	$2\,000 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	10	$9\,100 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$31\,000 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

A.C. CHARACTERISTICS

 $V_{SS} = 0 \text{ V}$; $T_{amb} = 25 \text{ }^\circ\text{C}$; $C_L = 50 \text{ pF}$; input transition times $\leq 20 \text{ ns}$

	V_{DD} V	symbol	min.	typ.	max.	typical extrapolation formula
Propagation delays						
$D_n \rightarrow O_n$	5		155	310	ns	$128 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
HIGH to LOW	10	t_{PHL}	60	120	ns	$49 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
	15		40	80	ns	$32 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
LOW to HIGH	5		135	270	ns	$108 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
	10	t_{PLH}	55	110	ns	$44 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
	15		40	80	ns	$32 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
$\overline{E_L} \rightarrow O_n$	5		160	320	ns	$133 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
HIGH to LOW	10	t_{PHL}	60	120	ns	$49 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
	15		45	90	ns	$37 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
LOW to HIGH	5		160	320	ns	$133 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
	10	t_{PLH}	60	120	ns	$49 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
	15		45	90	ns	$37 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
$\overline{B_I} \rightarrow O_n$	5		120	240	ns	$93 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
HIGH to LOW	10	t_{PHL}	50	100	ns	$39 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
	15		35	70	ns	$27 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
LOW to HIGH	5		105	210	ns	$78 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
	10	t_{PLH}	40	80	ns	$29 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
	15		30	60	ns	$22 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
$\overline{L_T} \rightarrow O_n$	5		65	130	ns	$38 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
HIGH to LOW	10	t_{PHL}	25	50	ns	$14 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
	15		20	40	ns	$12 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
LOW to HIGH	5		50	100	ns	$23 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
	10	t_{PLH}	25	50	ns	$14 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
	15		20	40	ns	$12 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
Output transition times	5		60	120	ns	$10 \text{ ns} + (1,0 \text{ ns/pF}) C_L$
HIGH to LOW	10	t_{THL}	30	60	ns	$9 \text{ ns} + (0,42 \text{ ns/pF}) C_L$
	15		20	40	ns	$6 \text{ ns} + (0,28 \text{ ns/pF}) C_L$
LOW to HIGH	5		18	36	ns	$13 \text{ ns} + (0,1 \text{ ns/pF}) C_L$
	10	t_{TLH}	11	22	ns	$8 \text{ ns} + (0,06 \text{ ns/pF}) C_L$
	15		9	18	ns	$6 \text{ ns} + (0,06 \text{ ns/pF}) C_L$
Minimum $\overline{E_L}$ pulse width; LOW	5		50	25	ns	
	10	t_{WELL}	20	10	ns	
	15		16	8	ns	
Set-up time	5		30	15	ns	
$D_n \rightarrow \overline{E_L}$	10	t_{su}	10	5	ns	see also waveforms Fig. 8
	15		10	5	ns	
Hold time	5		25	10	ns	
$D_n \rightarrow \overline{E_L}$	10	t_{hold}	10	5	ns	
	15		10	5	ns	

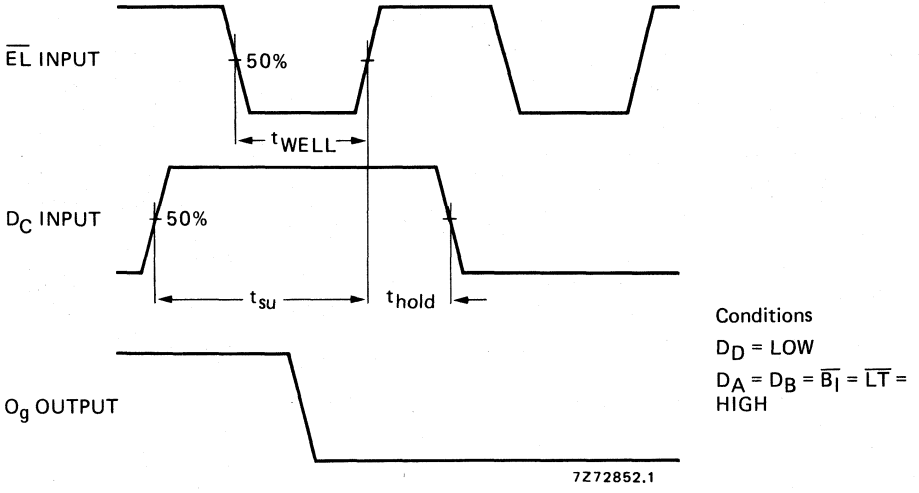


Fig. 8 Waveforms showing minimum \overline{EL} pulse width, set-up and hold time for D_C to \overline{EL} .

APPLICATION INFORMATION

Some examples of applications for the HEF4511B are:

- Driving LED displays.
- Driving incandescent displays.
- Driving fluorescent displays.
- Driving LCD displays.
- Driving gas discharge displays.

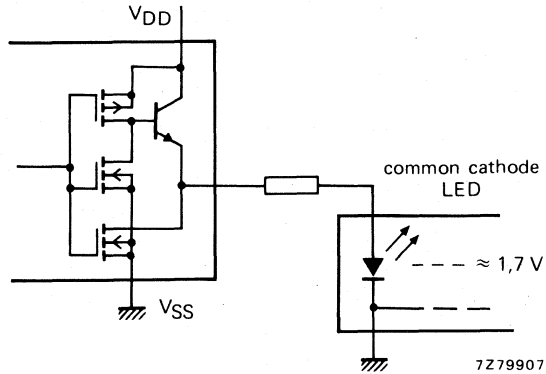


Fig. 9 Connection to common cathode LED display readout.

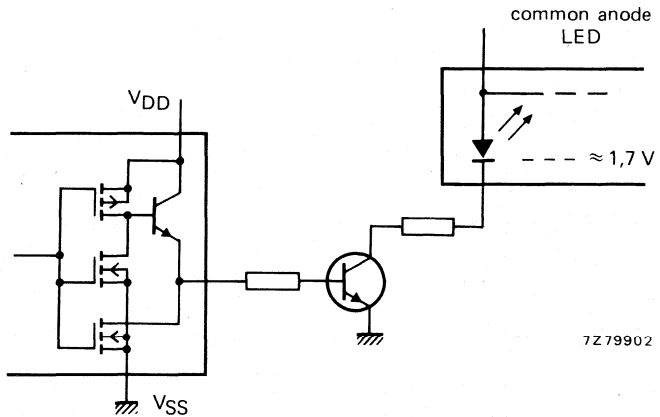


Fig. 10 Connection to common anode LED display readout.

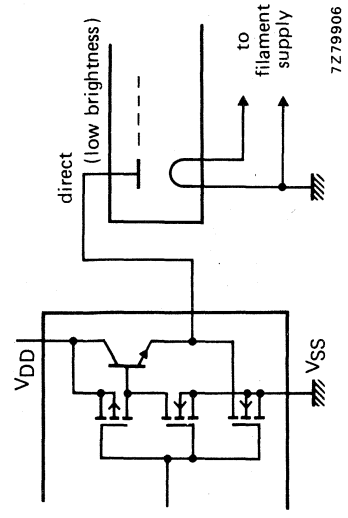
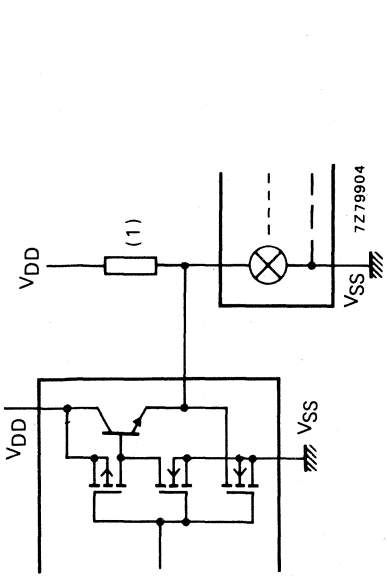


Fig. 12 Connection to fluorescent display readout.



(1) A filament pre-warm resistor is recommended to reduce filament thermal shock and increase the effective cold resistance of the filament.
Fig. 11 Connection to incandescent display readout.

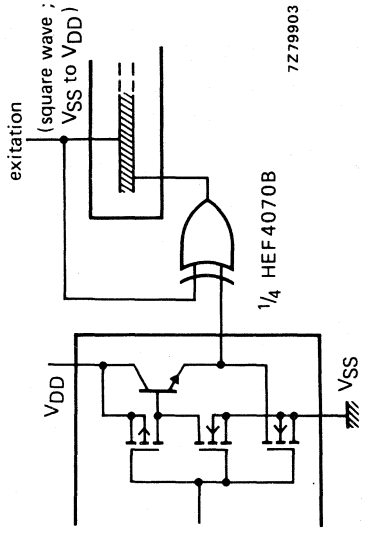


Fig. 14 Connection to liquid crystal (LCD) display readout.
Direct d.c. drive of LCDs not recommended for life of LCD readouts.

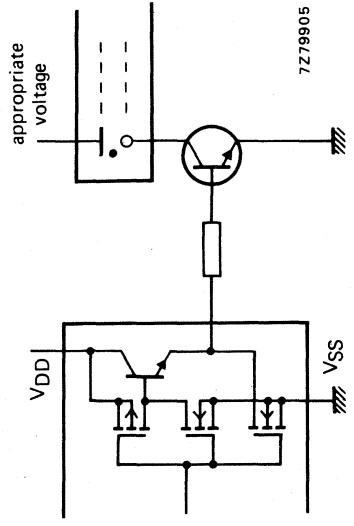


Fig. 13 Connection to gas discharge display readout.

8-INPUT MULTIPLEXER WITH 3-STATE OUTPUT



The HEF4512B is an 8-input multiplexer with 8 binary inputs (I_0 to I_7), an enable input (\bar{E}) and an output enable input (\bar{EO}). One of eight binary inputs is selected by select inputs S_0 , S_1 and S_2 , and is routed to the output O . A HIGH on \bar{EO} causes O to assume a high impedance OFF-state, regardless of other input conditions. This allows the output to interface directly with bus oriented systems (3-state). When the active LOW enable (\bar{E}) is HIGH, it forces the output LOW provided \bar{EO} is LOW. By proper manipulation of the inputs, the device can provide any logic functions of four variables. It cannot be used to multiplex analogue signals.

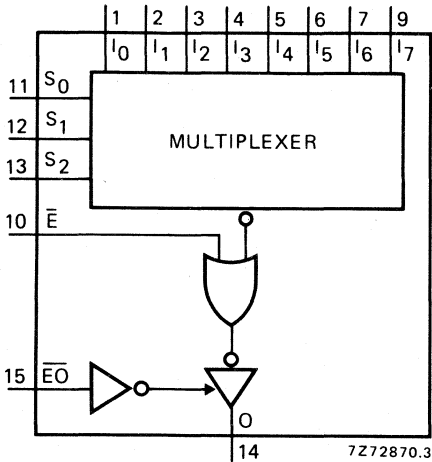


Fig. 1 Functional diagram.

PINNING

- S_0, S_1, S_2 select inputs
- \bar{EO} output enable (active LOW)
- \bar{E} enable (active LOW)
- I_0 to I_7 multiplexer inputs
- O multiplexer output

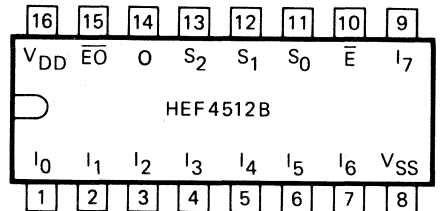


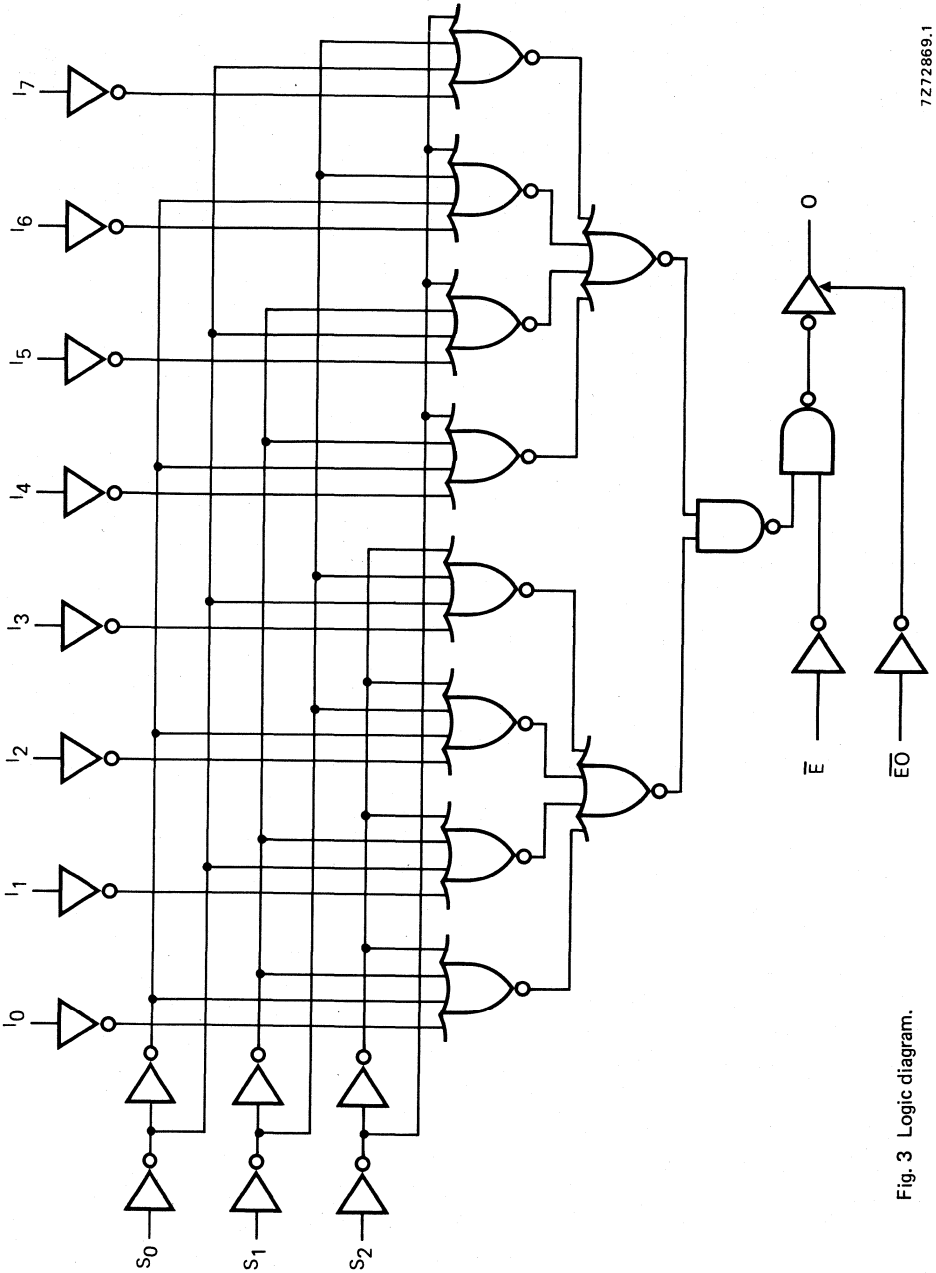
Fig. 2 Pinning diagram.

- HEF4512BP : 16-lead DIL; plastic (SOT-38Z).
- HEF4512BD : 16-lead DIL; ceramic (SOT-74).
- HEF4512BT : 16-lead flat pack; plastic (SO-16; SOT-109A).

FAMILY DATA

I_{DD} LIMITS category MSI

see Family Specifications



7272869.1

Fig. 3 Logic diagram.

TRUTH TABLE

		inputs											output
\overline{EO}	\overline{E}	S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	O
L	H	X	X	X	X	X	X	X	X	X	X	X	L
L	L	L	L	L	L	X	X	X	X	X	X	X	L
L	L	L	L	L	H	X	X	X	X	X	X	X	H
L	L	L	L	H	X	L	X	X	X	X	X	X	L
L	L	L	L	H	X	H	X	X	X	X	X	X	H
L	L	L	H	L	X	X	L	X	X	X	X	X	L
L	L	L	H	L	X	X	H	X	X	X	X	X	H
L	L	L	H	H	X	X	X	L	X	X	X	X	L
L	L	L	H	H	X	X	X	H	X	X	X	X	H
L	L	H	L	L	X	X	X	X	L	X	X	X	L
L	L	H	L	L	X	X	X	X	H	X	X	X	H
L	L	H	L	H	X	X	X	X	X	L	X	X	L
L	L	H	L	H	X	X	X	X	X	H	X	X	H
L	L	H	H	L	X	X	X	X	X	X	L	X	L
L	L	H	H	L	X	X	X	X	X	X	H	X	H
L	L	H	H	H	X	X	X	X	X	X	X	L	L
L	L	H	H	H	X	X	X	X	X	X	X	H	H
H	X	X	X	X	X	X	X	X	X	X	X	X	Z

- H = HIGH state (the more positive voltage)
- L = LOW state (the less positive voltage)
- X = state is immaterial
- Z = high impedance OFF-state

A.C. CHARACTERISTICS

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^\circ\text{C}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	typical formula for P (μW)	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
Dynamic power dissipation per package (P)	5 10 15	$500 f_i + \Sigma(f_o C_L) \times V_{DD}^2$ $2100 f_i + \Sigma(f_o C_L) \times V_{DD}^2$ $5800 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

A.C. CHARACTERISTICS

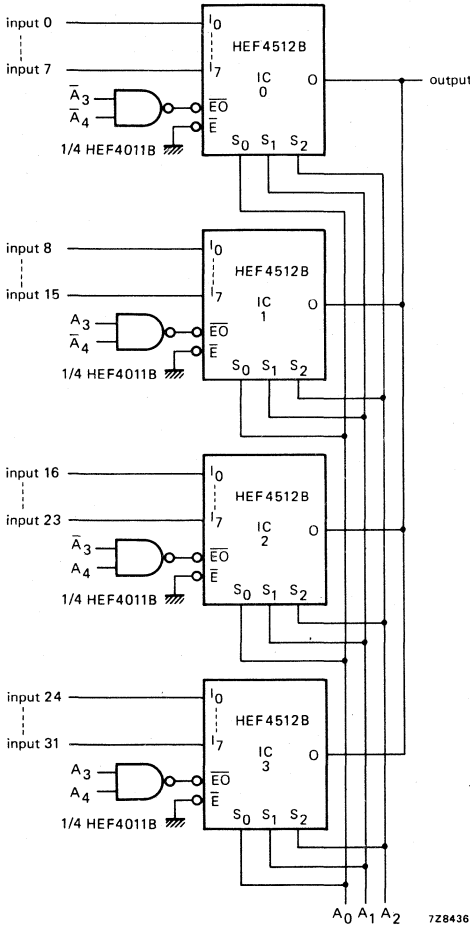
 $V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	symbol	typ.	max.		typical extrapolation formula	
Propagation delays $I_n \rightarrow 0$ HIGH to LOW	5	tPHL	100	200	ns	$73\text{ ns} + (0,55\text{ ns/pF}) C_L$	
	10		40	80	ns	$29\text{ ns} + (0,23\text{ ns/pF}) C_L$	
	15		30	60	ns	$22\text{ ns} + (0,16\text{ ns/pF}) C_L$	
LOW to HIGH	5	tPLH	100	200	ns	$73\text{ ns} + (0,55\text{ ns/pF}) C_L$	
	10		40	80	ns	$29\text{ ns} + (0,23\text{ ns/pF}) C_L$	
	15		30	60	ns	$22\text{ ns} + (0,16\text{ ns/pF}) C_L$	
$S_n \rightarrow 0$ HIGH to LOW	5	tPHL	140	280	ns	$113\text{ ns} + (0,55\text{ ns/pF}) C_L$	
	10		55	110	ns	$44\text{ ns} + (0,23\text{ ns/pF}) C_L$	
	15		40	80	ns	$32\text{ ns} + (0,16\text{ ns/pF}) C_L$	
LOW to HIGH	5	tPLH	150	300	ns	$123\text{ ns} + (0,55\text{ ns/pF}) C_L$	
	10		60	120	ns	$49\text{ ns} + (0,23\text{ ns/pF}) C_L$	
	15		40	80	ns	$32\text{ ns} + (0,16\text{ ns/pF}) C_L$	
$\bar{E} \rightarrow 0$ HIGH to LOW	5	tPHL	60	120	ns	$33\text{ ns} + (0,55\text{ ns/pF}) C_L$	
	10		25	50	ns	$14\text{ ns} + (0,23\text{ ns/pF}) C_L$	
	15		20	40	ns	$12\text{ ns} + (0,16\text{ ns/pF}) C_L$	
LOW to HIGH	5	tPLH	55	110	ns	$28\text{ ns} + (0,55\text{ ns/pF}) C_L$	
	10		25	50	ns	$14\text{ ns} + (0,23\text{ ns/pF}) C_L$	
	15		20	40	ns	$12\text{ ns} + (0,16\text{ ns/pF}) C_L$	
Output transition times HIGH to LOW	5	tTHL	60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$	
	10		30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$	
	15		20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$	
LOW to HIGH	5	tTLH	60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$	
	10		30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$	
	15		20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$	
3-state propagation delays							
	Output disable times $\bar{E}O \rightarrow 0$ HIGH	5	tPHZ	35	70	ns	
		10		20	40	ns	
15		15		30	ns		
LOW	5	tPLZ	35	70	ns		
	10		15	30	ns		
	15		10	20	ns		
Output enable times $\bar{E}O \rightarrow 0$ HIGH	5	tPZH	35	70	ns		
	10		15	30	ns		
	15		10	20	ns		
LOW	5	tPZL	35	70	ns		
	10		20	40	ns		
	15		15	30	ns		

APPLICATION INFORMATION

Some examples of applications for the HEF4512B are:

- Signal gating
- Digital multiplexing
- Number sequence generation



TRUTH TABLE for Fig. 4

A ₄	A ₃	A ₂	A ₁	A ₀	input conn. to output
L	L	L	L	L	0
L	L	L	L	H	1
L	L	L	H	L	2
L	L	L	H	H	3
L	L	H	L	L	4
L	L	H	L	H	5
L	L	H	H	L	6
L	L	H	H	H	7
L	H	L	L	L	8
L	H	L	L	H	9
L	H	L	H	L	10
L	H	L	H	H	11
L	H	H	L	L	12
L	H	H	L	H	13
L	H	H	H	L	14
L	H	H	H	H	15
H	L	L	L	L	16
H	L	L	L	H	17
H	L	L	H	L	18
H	L	L	H	H	19
H	L	H	L	L	20
H	L	H	L	H	21
H	L	H	H	L	22
H	L	H	H	H	23
H	H	L	L	L	24
H	H	L	L	H	25
H	H	L	H	L	26
H	H	L	H	H	27
H	H	H	L	L	28
H	H	H	L	H	29
H	H	H	H	L	30
H	H	H	H	H	31

Fig. 4 32-input multiplexer using 4 x HEF4512B and 1 x HEF4011B. The input is selected by 5-bit address (A₄ to A₀) and presented at the output.

1-OF-16 DECODER/DEMULTIPLEXER WITH INPUT LATCHES



The HEF4514B is a 1-of-16 decoder/demultiplexer, having four binary weighted address inputs (A_0 to A_3), a latch enable input (EL), and an active LOW enable input (\bar{E}). The 16 outputs (O_0 to O_{15}) are mutually exclusive active HIGH. When EL is HIGH, the selected output is determined by the data on A_n . When EL goes LOW, the last data present at A_n are stored in the latches and the outputs remain stable. When \bar{E} is LOW, the selected output, determined by the contents of the latch, is HIGH. At \bar{E} HIGH, all outputs are LOW. The enable input (\bar{E}) does not affect the state of the latch. When the HEF4514B is used as a demultiplexer, \bar{E} is the data input and A_0 to A_3 are the address inputs.

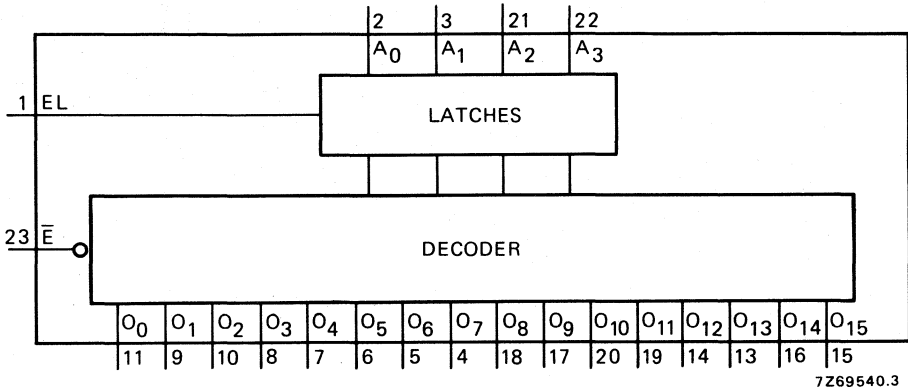


Fig. 1 Functional diagram.

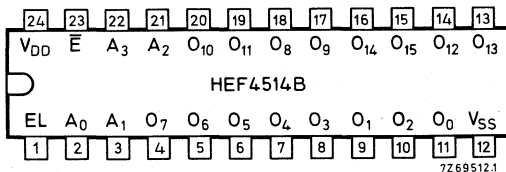


Fig. 2 Pinning diagram.

PINNING

A_0 to A_3	address inputs
\bar{E}	enable input (active LOW)
EL	latch enable input
O_0 to O_{15}	outputs (active HIGH)

HEF4514BP : 24-lead DIL; plastic (SOT-101A).

HEF4514BD : 24-lead DIL; ceramic (SOT-94).

APPLICATION INFORMATION

Some examples of applications for the HEF4514B are:

- Digital multiplexing.
- Address decoding.
- Hexadecimal/BCD decoding.

FAMILY DATA

I_{DD} LIMITS category MSI

} see Family Specifications

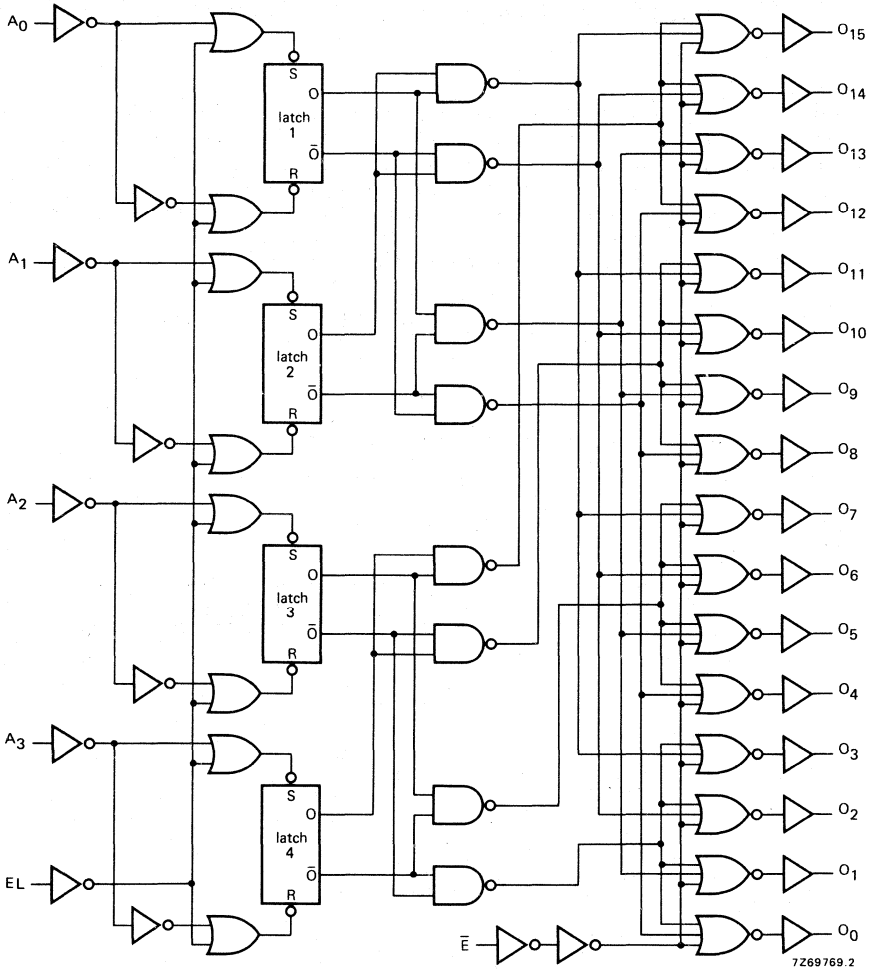


Fig. 3 Logic diagram.

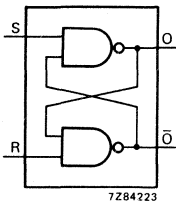


Fig. 4 Logic diagram (one latch).

TRUTH TABLE

inputs					outputs																
\bar{E}	A ₀	A ₁	A ₂	A ₃	O ₀	O ₁	O ₂	O ₃	O ₄	O ₅	O ₆	O ₇	O ₈	O ₉	O ₁₀	O ₁₁	O ₁₂	O ₁₃	O ₁₄	O ₁₅	
H	X	X	X	X	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	H	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	L	H	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	H	H	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L
L	L	L	H	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L
L	H	L	H	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L
L	L	H	H	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L
L	H	H	H	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L
L	L	L	L	H	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L
L	H	L	L	H	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L
L	L	H	L	H	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L
L	H	H	L	H	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L
L	L	L	H	H	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L
L	L	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L
L	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L

EL = HIGH

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

X = state is immaterial

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

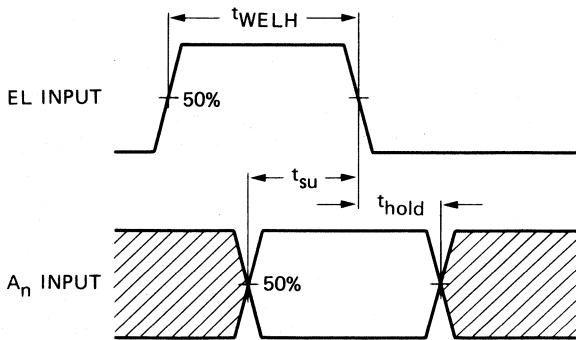
	V _{DD} V	symbol	typ.	max.		typical extrapolation formula
Propagation delays A _n , EL → O _n HIGH to LOW	5	t _{PHL}	260	520	ns	233 ns + (0,55 ns/pF) C _L
	10		95	190	ns	84 ns + (0,23 ns/pF) C _L
	15		65	130	ns	57 ns + (0,16 ns/pF) C _L
LOW to HIGH	5	t _{PLH}	270	550	ns	243 ns + (0,55 ns/pF) C _L
	10		95	190	ns	84 ns + (0,23 ns/pF) C _L
	15		65	130	ns	57 ns + (0,16 ns/pF) C _L
\bar{E} → O _n HIGH to LOW	5	t _{PHL}	175	350	ns	148 ns + (0,55 ns/pF) C _L
	10		65	130	ns	54 ns + (0,23 ns/pF) C _L
	15		45	90	ns	37 ns + (0,16 ns/pF) C _L
LOW to HIGH	5	t _{PLH}	200	400	ns	173 ns + (0,55 ns/pF) C _L
	10		70	140	ns	59 ns + (0,23 ns/pF) C _L
	15		50	100	ns	42 ns + (0,16 ns/pF) C _L

A.C. CHARACTERISTICS

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^\circ\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	symbol	min.	typ.	max.	typical extrapolation formula	
Output transition times HIGH to LOW	5	t_{THL}		90	180	ns	$40\text{ ns} + (1,0\text{ ns/pF}) C_L$
	10		35	65	ns	$14\text{ ns} + (0,42\text{ ns/pF}) C_L$	
	15		25	50	ns	$11\text{ ns} + (0,28\text{ ns/pF}) C_L$	
LOW to HIGH	5	t_{TLH}		85	170	ns	$35\text{ ns} + (1,0\text{ ns/pF}) C_L$
	10		35	70	ns	$14\text{ ns} + (0,42\text{ ns/pF}) C_L$	
	15		25	50	ns	$11\text{ ns} + (0,28\text{ ns/pF}) C_L$	
Set-up time $A_n \rightarrow EL$	5	t_{su}	120	60		ns	} see also waveforms Fig. 5
	10		40	20		ns	
	15		30	15		ns	
Hold time $A_n \rightarrow EL$	5	t_{hold}	0	60		ns	
	10		0	20		ns	
	15		0	15		ns	
Minimum EL pulse width; HIGH	5	t_{WELH}	120	60		ns	
	10		40	20		ns	
	15		30	15		ns	

	V_{DD} V	typical formula for P (μW)	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
Dynamic power dissipation per package (P)	5	$1100 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	10	$5500 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$16\,000 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	



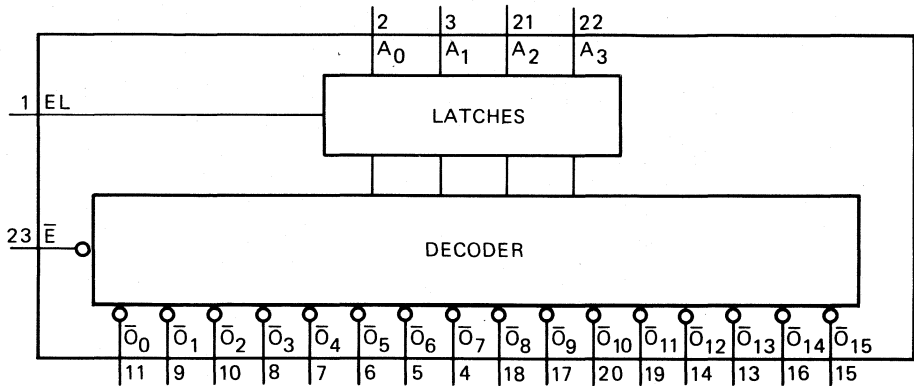
7Z74552

Fig. 5 Waveforms showing minimum pulse width for EL, set-up and hold times for A_n to EL. Set-up and hold times are shown as positive values but may be specified as negative values.

1-OF-16 DECODER/DEMULTIPLEXER WITH INPUT LATCHES

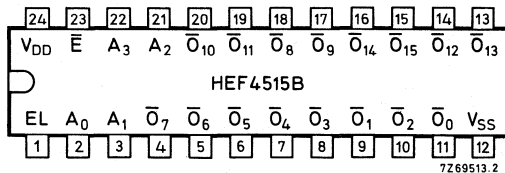


The HEF4515B is a 1-of-16 decoder/demultiplexer, having four binary weighted address inputs (A_0 to A_3), a latch enable input (EL), and an active LOW enable input (\bar{E}). The 16 outputs (\bar{O}_0 to \bar{O}_{15}) are mutually exclusive active LOW. When EL is HIGH, the selected output is determined by the data on A_n . When EL goes LOW, the last data present at A_n are stored in the latches and the outputs remain stable. When \bar{E} is LOW, the selected output, determined by the contents of the latch, is LOW. At \bar{E} HIGH, all outputs are HIGH. The enable input (\bar{E}) does not affect the state of the latch. When the HEF 4515B is used as a demultiplexer, \bar{E} is the data input and A_0 to A_3 are the address inputs.



7Z84275

Fig. 1 Functional diagram.



PINNING

- A_0 to A_3 address inputs
- \bar{E} enable input (active LOW)
- EL latch enable input
- \bar{O}_0 to \bar{O}_{15} outputs (active LOW)

Fig. 2 Pinning diagram.

HEF4515BP: 24-lead DIL; plastic (SOT-101A).

HEF4515BD: 24-lead DIL; ceramic (SOT-94).

APPLICATION INFORMATION

Some examples of applications for the HEF4515B are:

- Digital multiplexing.
- Address decoding.
- Hexadecimal/BCD decoding.

FAMILY DATA

I_{DD} LIMITS category MSI

} see Family Specifications

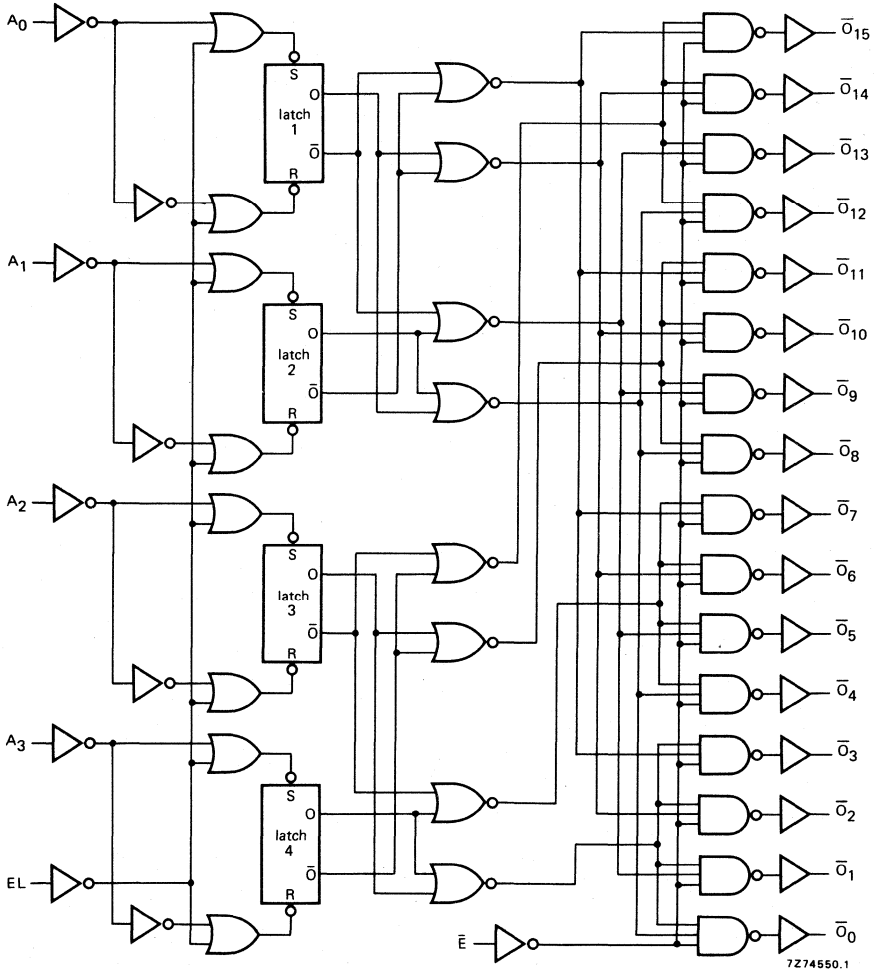


Fig. 3 Logic diagram.

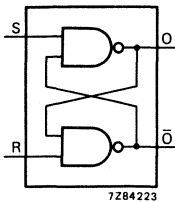


Fig. 4 Logic diagram (one latch).

TRUTH TABLE

inputs					outputs																
\bar{E}	A ₀	A ₁	A ₂	A ₃	\bar{O}_0	\bar{O}_1	\bar{O}_2	\bar{O}_3	\bar{O}_4	\bar{O}_5	\bar{O}_6	\bar{O}_7	\bar{O}_8	\bar{O}_9	\bar{O}_{10}	\bar{O}_{11}	\bar{O}_{12}	\bar{O}_{13}	\bar{O}_{14}	\bar{O}_{15}	
H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	H	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	H	L	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	H	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L

EL = HIGH
 H = HIGH state (the more positive voltage)
 L = LOW state (the less positive voltage)
 X = state is immaterial

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

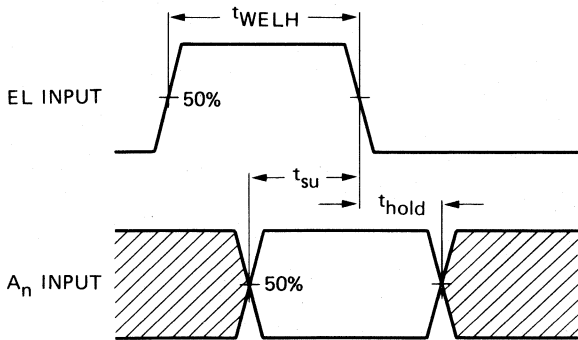
	V _{DD} V	symbol	typ.	max.	typical extrapolation formula	
Propagation delays A _n , EL → \bar{O}_n HIGH to LOW	5	t _{PHL}	260	520	ns	233 ns + (0,55 ns/pF) C _L
	10		95	190	ns	84 ns + (0,23 ns/pF) C _L
	15		65	130	ns	57 ns + (0,16 ns/pF) C _L
LOW to HIGH	5	t _{PLH}	270	550	ns	243 ns + (0,55 ns/pF) C _L
	10		95	190	ns	84 ns + (0,23 ns/pF) C _L
	15		65	130	ns	57 ns + (0,16 ns/pF) C _L
\bar{E} → \bar{O}_n HIGH to LOW	5	t _{PHL}	175	350	ns	148 ns + (0,55 ns/pF) C _L
	10		65	130	ns	54 ns + (0,23 ns/pF) C _L
	15		45	90	ns	37 ns + (0,16 ns/pF) C _L
LOW to HIGH	5	t _{PLH}	200	400	ns	173 ns + (0,55 ns/pF) C _L
	10		70	140	ns	59 ns + (0,23 ns/pF) C _L
	15		50	100	ns	42 ns + (0,16 ns/pF) C _L

A.C. CHARACTERISTICS

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^\circ\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	symbol	min.	typ.	max.	typical extrapolation formula
Output transition times HIGH to LOW	5	t_{THL}		90	180	$40\text{ ns} + (1,0\text{ ns/pF}) C_L$
	10		35	65	$14\text{ ns} + (0,42\text{ ns/pF}) C_L$	
	15		25	50	$11\text{ ns} + (0,28\text{ ns/pF}) C_L$	
LOW to HIGH	5	t_{TLH}		85	170	$35\text{ ns} + (1,0\text{ ns/pF}) C_L$
	10		35	70	$14\text{ ns} + (0,42\text{ ns/pF}) C_L$	
	15		25	50	$11\text{ ns} + (0,28\text{ ns/pF}) C_L$	
Set-up time $A_n \rightarrow$ EL	5	t_{su}	120	60	ns	} see also waveforms Fig. 5
	10		40	20	ns	
	15		30	15	ns	
Hold time $A_n \rightarrow$ EL	5	t_{hold}	0	60	ns	
	10		0	20	ns	
	15		0	15	ns	
Minimum EL pulse width; HIGH	5	t_{WELH}	120	60	ns	
	10		40	20	ns	
	15		30	15	ns	

	V_{DD} V	typical formula for P (μW)	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
Dynamic power dissipation per package (P)	5	$1100 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	10	$5500 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$16000 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	



7274552

Fig. 5 Waveforms showing minimum pulse width for EL, set-up and hold times for A_n to EL. Set-up and hold times are shown as positive values but may be specified as negative values.



BINARY UP/DOWN COUNTER

The HEF4516B is an edge-triggered synchronous up/down 4-bit binary counter with a clock input (CP), an up/down count control input (UP/DN), an active LOW count enable input (\overline{CE}), an asynchronous active HIGH parallel load input (PL), four parallel inputs (P_0 to P_3), four parallel outputs (O_0 to O_3), an active LOW terminal count output (\overline{TC}), and an overriding asynchronous master reset input (MR).

Information on P_0 to P_3 is loaded into the counter while PL is HIGH, independent of all other input conditions except MR which must be LOW. When PL and \overline{CE} are LOW, the counter changes on the LOW to HIGH transition of CP. Input UP/DN determines the direction of the count, HIGH for counting up, LOW for counting down. When counting up, \overline{TC} is LOW when O_0 to O_3 are HIGH and \overline{CE} is LOW. When counting down, \overline{TC} is LOW when O_0 to O_3 and \overline{CE} are LOW. A HIGH on MR resets the counter (O_0 to $O_3 = \text{LOW}$) independent of all other input conditions.

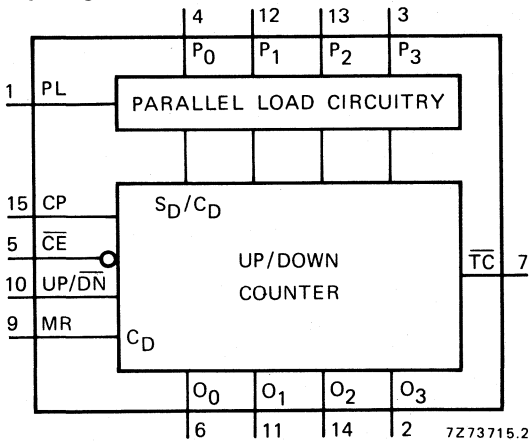


Fig. 1 Functional diagram.

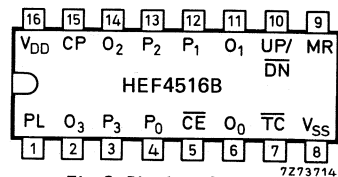


Fig. 2 Pinning diagram.

HEF4516BP: 16-lead DIL; plastic (SOT-38Z).
HEF4516BD: 16-lead DIL; ceramic (SOT-74).
HEF4516BT: 16-lead flat pack; plastic (SO-16; SOT-109A).

PINNING

PL	parallel load input (active HIGH)	UP/DN	up/down count control input
P_0 to P_3	parallel inputs	MR	master reset input
\overline{CE}	count enable input (active LOW)	\overline{TC}	terminal count output (active LOW)
CP	clock pulse input (LOW to HIGH, edge triggered)	O_0 to O_3	parallel outputs

FAMILY DATA

I_{DD} LIMITS category MSI

} see Family Specifications

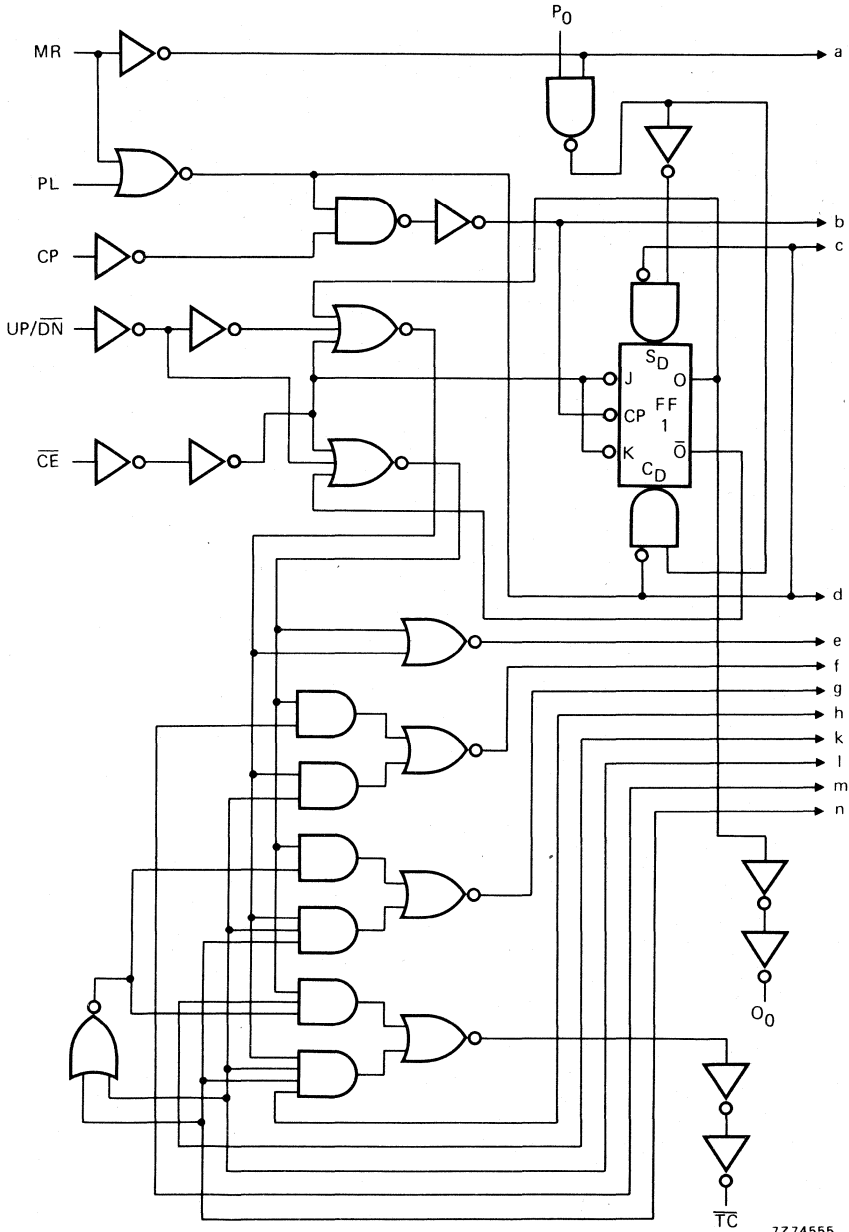
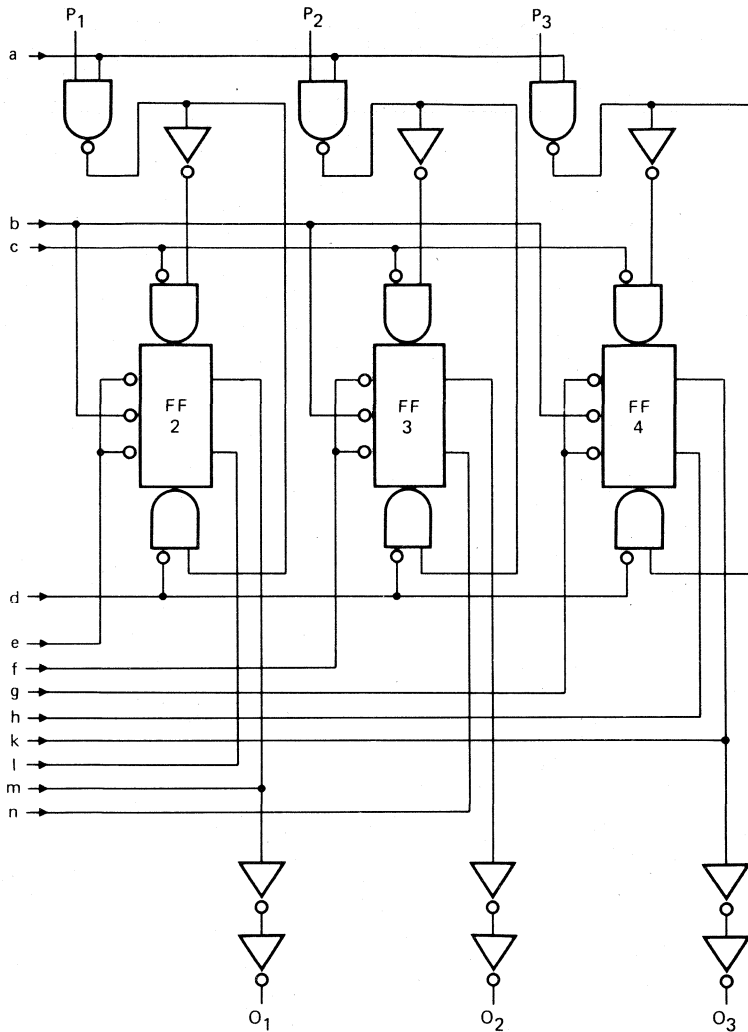


Fig. 3a Logic diagram (continued in Fig. 3b).

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Fig. 3b Logic diagram (continued from Fig. 3a).

FUNCTION TABLE

MR	PL	UP/DN	CE	CP	mode
L	H	X	X	X	parallel load
L	L	X	H	X	no change
L	L	L	L	/	count down
L	L	H	L	/	count up
H	X	X	X	X	reset

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

X = state is immaterial

/ = positive-going transition

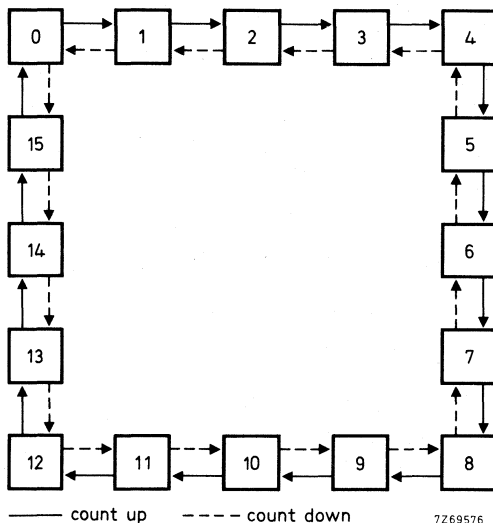


Fig. 4 State diagram.

Logic equation for terminal count:

$$\overline{TC} = \overline{CE} \cdot \{ (UP/DN) \cdot O_0 \cdot O_1 \cdot O_2 \cdot O_3 + (UP/DN) \cdot \overline{O_0} \cdot \overline{O_1} \cdot \overline{O_2} \cdot \overline{O_3} \}$$

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ≤ 20 ns

	V _{DD} V	typical formula for P (μW)	where f _i = input freq. (MHz) f _o = output freq. (MHz) C _L = load capacitance (pF) Σ(f _o C _L) = sum of outputs V _{DD} = supply voltage (V)
Dynamic power dissipation per package (P)	5	1000 f _i + Σ(f _o C _L) × V _{DD} ²	
	10	4500 f _i + Σ(f _o C _L) × V _{DD} ²	
	15	11 200 f _i + Σ(f _o C _L) × V _{DD} ²	

A.C. CHARACTERISTICS

 $V_{SS} = 0 \text{ V}$; $T_{amb} = 25 \text{ }^\circ\text{C}$; $C_L = 50 \text{ pF}$; input transition times $\leq 20 \text{ ns}$

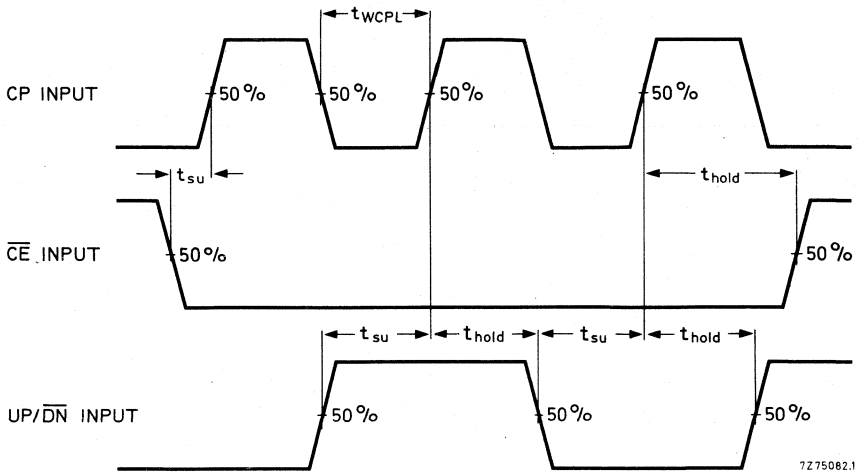
	V_{DD} V	symbol	min.	typ.	max.	typical extrapolation formula
Propagation delays						
CP \rightarrow O_n	5			145	290 ns	$118 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
HIGH to LOW	10	tPHL		60	120 ns	$49 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
	15			45	90 ns	$37 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
	5			155	310 ns	$128 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
LOW to HIGH	10	tPLH		65	130 ns	$54 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
	15			45	90 ns	$37 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
CP \rightarrow \overline{TC}	5			260	525 ns	$233 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
HIGH to LOW	10	tPHL		105	210 ns	$94 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
	15			75	150 ns	$67 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
	5			180	360 ns	$153 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
LOW to HIGH	10	tPLH		75	150 ns	$64 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
	15			55	115 ns	$47 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
PL \rightarrow O_n	5			125	255 ns	$98 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
HIGH to LOW	10	tPHL		55	110 ns	$44 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
	15			40	85 ns	$32 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
	5			170	340 ns	$143 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
LOW to HIGH	10	tPLH		70	140 ns	$59 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
	15			50	105 ns	$42 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
PL \rightarrow \overline{TC}	5			250	500 ns	$223 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
HIGH to LOW	10	tPHL		110	220 ns	$99 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
	15			80	160 ns	$72 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
	5			250	500 ns	$223 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
LOW to HIGH	10	tPLH		110	220 ns	$99 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
	15			80	160 ns	$72 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
$\overline{CE} \rightarrow \overline{TC}$	5			165	330 ns	$138 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
HIGH to LOW	10	tPHL		65	135 ns	$54 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
	15			50	100 ns	$42 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
	5			145	290 ns	$118 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
LOW to HIGH	10	tPLH		60	125 ns	$49 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
	15			45	95 ns	$37 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
MR \rightarrow O_n, \overline{TC}	5			205	405 ns	$178 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
HIGH to LOW	10	tPHL		65	130 ns	$54 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
	15			45	85 ns	$37 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
MR \rightarrow \overline{TC}	5			225	450 ns	$198 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
LOW to HIGH	10	tPLH		75	150 ns	$64 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
	15			50	100 ns	$42 \text{ ns} + (0,16 \text{ ns/pF}) C_L$

A.C. CHARACTERISTICS

 $V_{SS} = 0 \text{ V}$; $T_{amb} = 25 \text{ }^\circ\text{C}$; $C_L = 50 \text{ pF}$; input transition times $\leq 20 \text{ ns}$

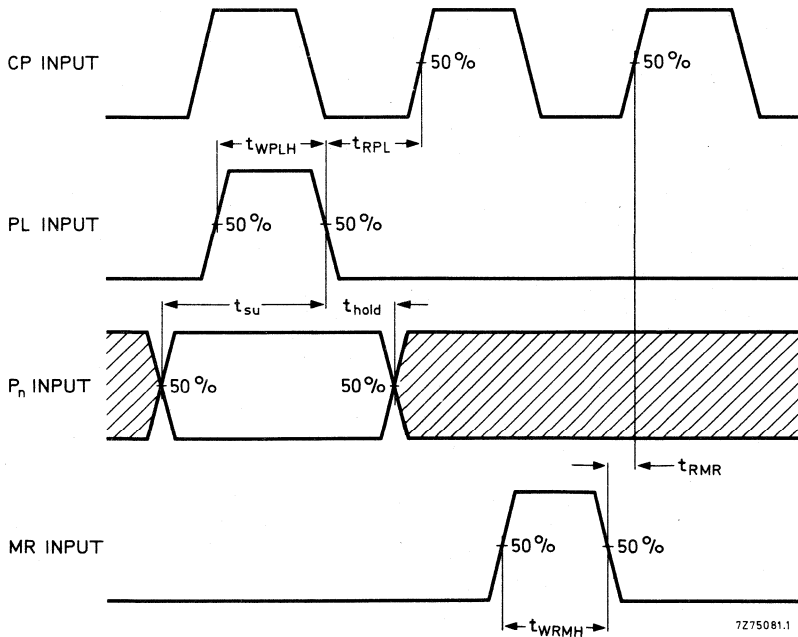
	V_{DD} V	symbol	min.	typ.	max.	typical extrapolation formula	
Output transition times HIGH to LOW	5	t_{THL}		60	120	ns	
	10			30	60	ns	
	15			20	40	ns	
	LOW to HIGH	5	t_{TLH}		60	120	ns
		10			30	60	ns
		15			20	40	ns
Minimum clock pulse width; LOW	5	t_{WCPL}	95	45		ns	
	10		35	20		ns	
	15		25	15		ns	
Minimum PL pulse width; HIGH	5	t_{WPLH}	105	55		ns	
	10		45	25		ns	
	15		35	15		ns	
Minimum MR pulse width; HIGH	5	t_{WMRH}	120	60		ns	
	10		50	25		ns	
	15		40	20		ns	
Recovery time for MR	5	t_{RMR}	130	65		ns	
	10		45	20		ns	
	15		30	15		ns	
Recovery time for PL	5	t_{RPL}	150	75		ns	
	10		50	25		ns	
	15		30	15		ns	
Set-up times $P_n \rightarrow PL$	5	t_{su}	100	50		ns	
	10		50	25		ns	
	15		40	20		ns	
$UP/\overline{DN} \rightarrow CP$	5	t_{su}	250	125		ns	
	10		100	50		ns	
	15		75	35		ns	
$\overline{CE} \rightarrow CP$	5	t_{su}	120	60		ns	
	10		40	20		ns	
	15		25	10		ns	
Hold times $P_n \rightarrow PL$	5	t_{hold}	10	-40		ns	
	10		5	-20		ns	
	15		0	-20		ns	
$UP/\overline{DN} \rightarrow CP$	5	t_{hold}	35	-90		ns	
	10		15	-35		ns	
	15		15	-25		ns	
$\overline{CE} \rightarrow CP$	5	t_{hold}	20	-40		ns	
	10		5	-15		ns	
	15		5	-10		ns	
Maximum clock pulse frequency	5	f_{max}	5	10		MHz	
	10		12	24		MHz	
	15		17	34		MHz	

 see also waveforms
Figs 5 and 6



7275082.1

Fig. 5 Waveforms showing minimum pulse width for CP, set-up and hold times for \overline{CE} to CP and UP/ \overline{DN} to CP.



7275081.1

Fig. 6 Waveforms showing minimum pulse width for PL and MR, recovery time for PL and MR and set-up and hold times for P_n to PL.

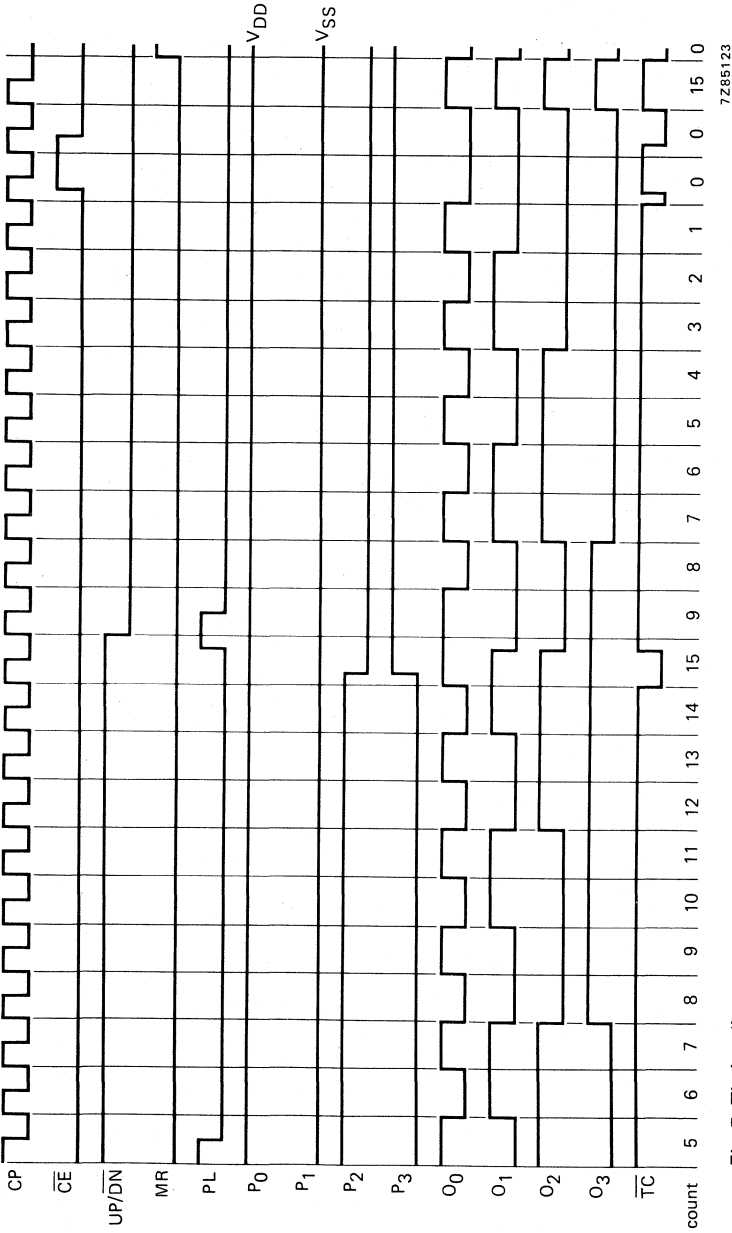


Fig. 7 Timing diagram.

APPLICATION INFORMATION

Some examples of applications for the HEF4516B are:

- Up/down difference counting
- Synchronous frequency dividers

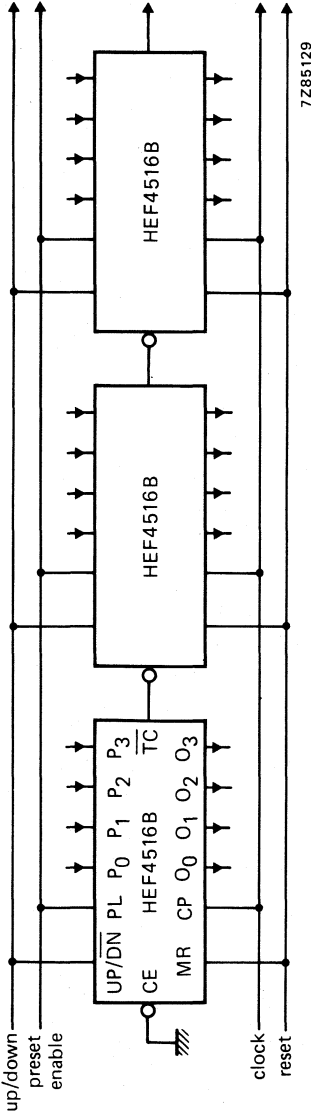


Fig. 8 Example of parallel clocking when cascading HEF4516B ICs.

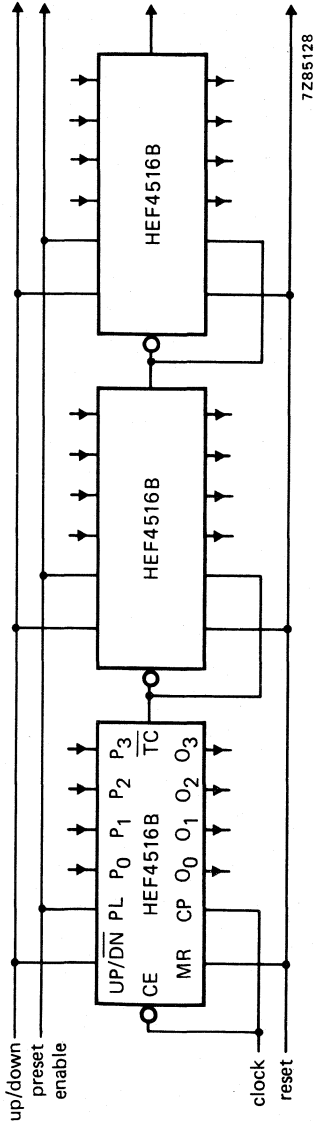


Fig. 9 Example of ripple clocking when cascading HEF4516B ICs. Ripple clocking mode: the up/down control can be changed at any count; the only restriction on changing the up/down control is that the clock input to the first counting stage must be HIGH.



DUAL 64-BIT STATIC SHIFT REGISTER

The HEF4517B consists of two identical, independent 64-bit static shift registers. Each register has separate clock (CP), data input (D), parallel input-enable/output-enable (PE/ \overline{EO}) and four 3-state outputs of the 16th, 32nd, 48th and 64th bit positions (O_{16} to O_{64}). Data at the D input is entered into the first bit on the LOW to HIGH transition of the clock, regardless of the state of PE/ \overline{EO} .

When PE/ \overline{EO} is LOW the outputs are enabled and the device is in the 64-bit serial mode.

When PE/ \overline{EO} is HIGH the outputs are disabled (high impedance OFF-state), the 64-bit shift register is divided into four 16-bit shift registers with D, O_{16} , O_{32} and O_{48} as data inputs of the 1st, 17th, 33rd, and 49th bit respectively.

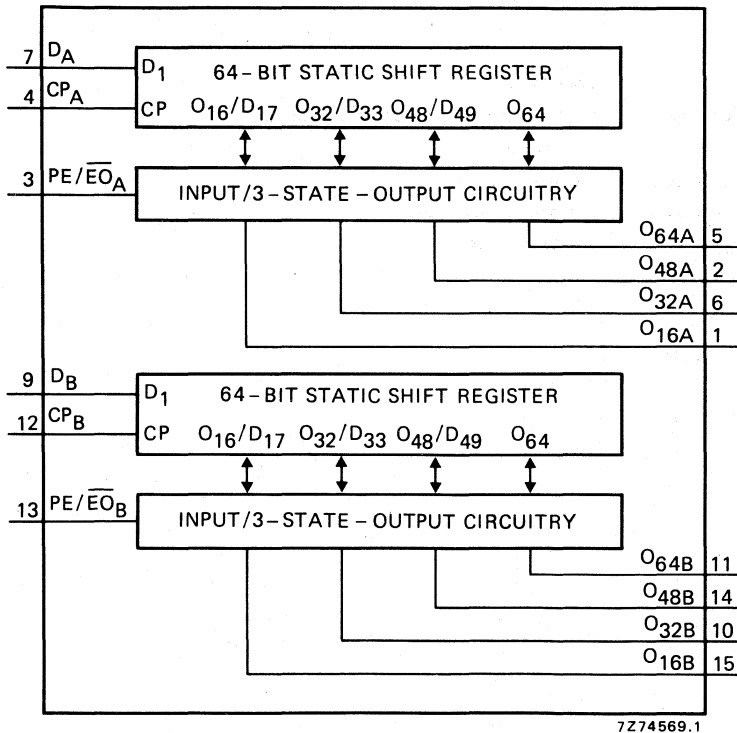


Fig. 1 Functional diagram.

FAMILY DATA

I_{DD} LIMITS category LSI

see Family Specifications

HEF4517B
LSI

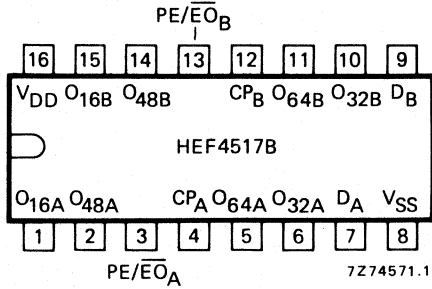


Fig. 2 Pinning diagram.

HEF4517BP: 16-lead DIL; plastic (SOT-38Z).
HEF4517BD: 16-lead DIL; ceramic (SOT-74).

PINNING

CP _A , CP _B	clock inputs
PE/ \overline{EO}_A , PE/ \overline{EO}_B	parallel input-enable/output-enable inputs
D _A , D _B	data inputs
O _{16A} , O _{32A} , O _{48A}	3-state outputs/inputs
O _{16B} , O _{32B} , O _{48B}	3-state outputs/inputs
O _{64A} , O _{64B}	3-state outputs

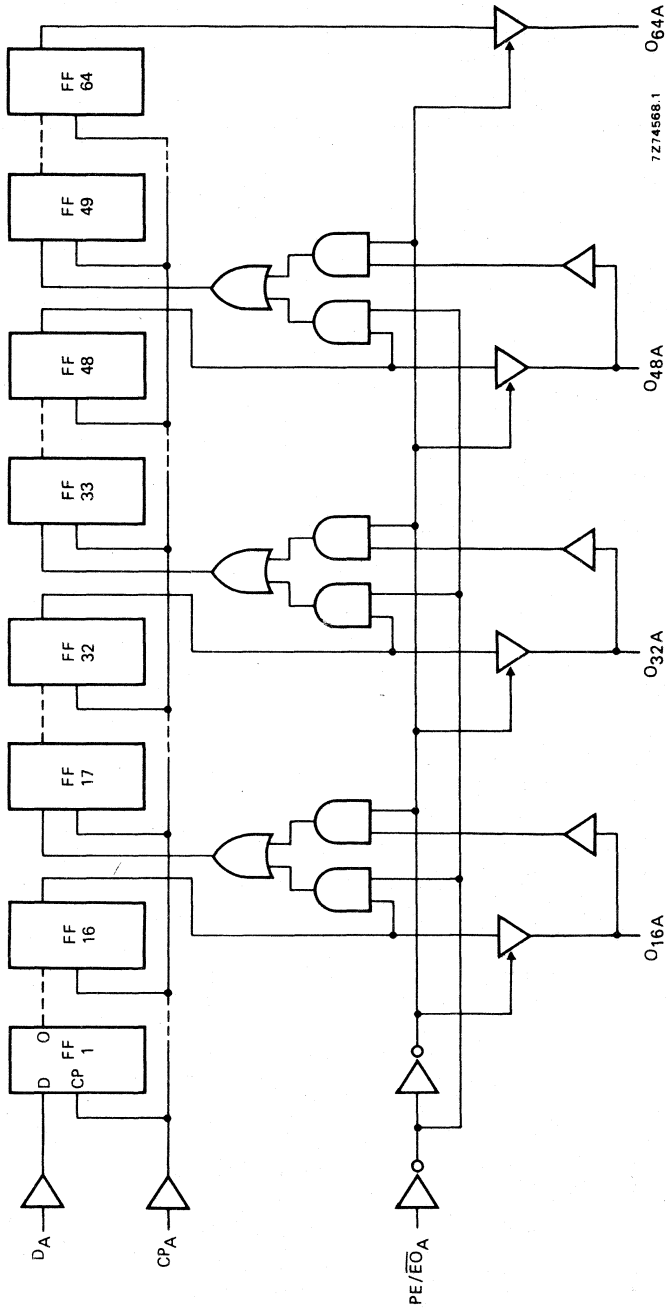


Fig. 3 Logic diagram (one shift register).

FUNCTION TABLE

CP	inputs		inputs/outputs				mode
	D	PE/EO	O16	O32	O48	O64	
∩	data entered into 1st bit	L	content of 16th bit displayed	content of 32nd bit displayed	content of 48th bit displayed	content of 64th bit displayed	One 64-bit shift register. The content of the shift register is shifted over one stage
∩	data entered into 1st bit	H	data at O16 entered into 17th bit	data at O32 entered into 33rd bit	data at O48 entered into 49th bit	remains in 'Z' state	Four 16-bit shift register. The content of the shift registers is shifted over one stage.
∩	X	L	no change	no change	no change	no change	no change
∩	X	H	Z	Z	Z	Z	no change

H = HIGH state (the more positive voltage)
 L = LOW state (the less positive voltage)
 X = state is immaterial
 Z = high impedance state
 ∩ = positive-going transition
 ∩ = negative-going transition

A.C. CHARACTERISTICS

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	typical formula for P (μW)	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
Dynamic power dissipation per package (P)	5	$7\,000 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	10	$28\,000 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$70\,000 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

A.C. CHARACTERISTICS

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	symbol	min.	typ.	max.	typical extrapolation formula	
Propagation delays $CP \rightarrow Q_n$ HIGH to LOW	5	t_{PHL}		220	440	ns	$193\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10		85	170	ns	$74\text{ ns} + (0,23\text{ ns/pF}) C_L$	
	15		60	120	ns	$52\text{ ns} + (0,16\text{ ns/pF}) C_L$	
LOW to HIGH	5	t_{PLH}		190	380	ns	$163\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10		75	150	ns	$64\text{ ns} + (0,23\text{ ns/pF}) C_L$	
	15		50	100	ns	$42\text{ ns} + (0,16\text{ ns/pF}) C_L$	
Output transition times HIGH to LOW	5	t_{THL}		60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$
	10		30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$	
	15		20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$	
LOW to HIGH	5	t_{TLH}		60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$
	10		30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$	
	15		20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$	

A.C. CHARACTERISTICS

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^\circ\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	symbol	min.	typ.	max.	
Minimum clock pulse width; LOW	5	t_{WCPL}		95	190	ns
	10			40	30	ns
	15			30	60	ns
Set-up times $O_n, D \rightarrow CP$	5	t_{su}	30	10		ns
	10		25	5		ns
	15		20	5		ns
Hold time $O_n, D \rightarrow CP$	5	t_{hold}	45	15		ns
	10		30	10		ns
	15		25	10		ns
3-state propagation delays						
Output disable times $PE/\bar{E}O \rightarrow O_n$ HIGH	5	t_{PHZ}		40	80	ns
	10			30	60	ns
	15			25	50	ns
LOW	5	t_{PLZ}		50	100	ns
	10			30	60	ns
	15			25	50	ns
Output enable times $PE/\bar{E}O \rightarrow O_n$ HIGH	5	t_{PZH}		45	90	ns
	10			25	50	ns
	15			20	40	ns
LOW	5	t_{PZL}		60	120	ns
	10			30	60	ns
	15			25	50	ns
Maximum clock pulse frequency	5	f_{max}	2	5		MHz
	10		6	12		MHz
	15		8	16		MHz

see also waveforms
Fig. 4.

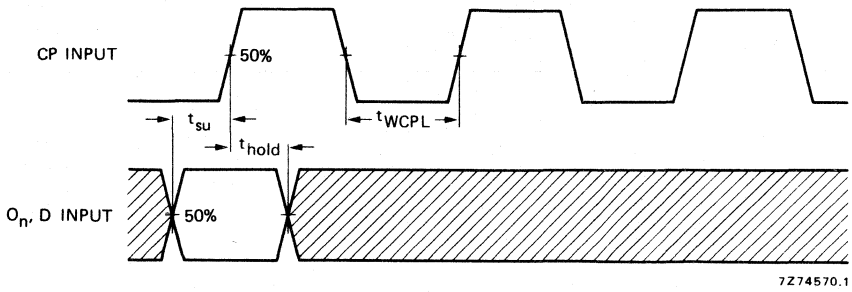


Fig. 4 Waveforms showing minimum clock pulse width, set-up and hold times for O_n (as data input) and D to CP.

DUAL BCD COUNTER



The HEF4518B is a dual 4-bit internally synchronous BCD counter. The counter has an active HIGH clock input (CP_0) and an active LOW clock input (\overline{CP}_1), buffered outputs from all four bit positions (O_0 to O_3) and an active HIGH overriding asynchronous master reset input (MR). The counter advances on either the LOW to HIGH transition of the CP_0 input if \overline{CP}_1 is HIGH or the HIGH to LOW transition of the \overline{CP}_1 input if CP_0 is LOW. Either CP_0 or \overline{CP}_1 may be used as the clock input to the counter and the other clock input may be used as a clock enable input. A HIGH on MR resets the counter (O_0 to $O_3 = \text{LOW}$) independent of CP_0 , \overline{CP}_1 .

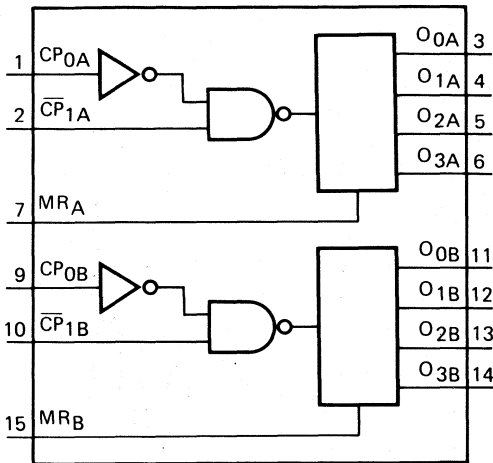


Fig. 1 Functional diagram.

7269556.1

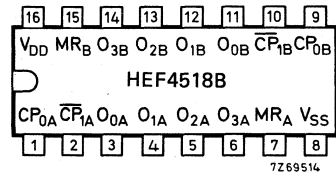


Fig. 2 Pinning diagram.

HEF4518BP: 16-lead DIL; plastic (SOT-38Z).
 HEF4518BD: 16-lead DIL; ceramic (SOT-74).
 HEF4518BT: 16-lead flat pack; plastic (SO-16; SOT-109A).

PINNING

CP_{0A} , CP_{0B} clock inputs (L to H triggered)
 \overline{CP}_{1A} , \overline{CP}_{1B} clock inputs (H to L triggered)
 MR_A , MR_B master reset inputs
 O_{0A} to O_{3A} outputs
 O_{0B} to O_{3B} outputs

APPLICATION INFORMATION

Some examples of applications for the HEF4518B are:

- Multistage synchronous counting.
- Multistage asynchronous counting.
- Frequency dividers.

FAMILY DATA

I_{DD} LIMITS category MSI

} see Family Specifications

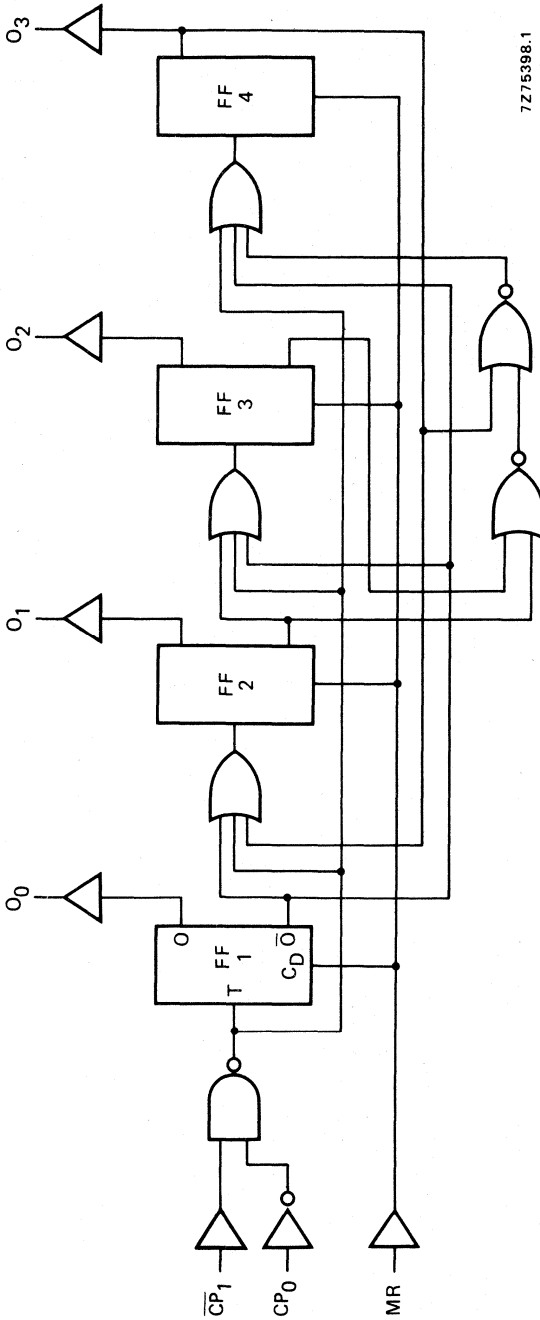


Fig. 3 Logic diagram (one counter).

FUNCTION TABLE

CP0	$\overline{CP1}$	MR	mode
∕	H	L	counter advances
L	∖	L	counter advances
∖	X	L	no change
∕	∕	L	no change
H	∖	L	no change
X	X	H	O0 to O3 = LOW

H = HIGH state (the more positive voltage)
 L = LOW state (the less positive voltage)
 X = state is immaterial
 ∕ = positive-going transition
 ∖ = negative-going transition

A.C. CHARACTERISTICS

 $V_{SS} = 0 \text{ V}$; $T_{amb} = 25 \text{ }^\circ\text{C}$; $C_L = 50 \text{ pF}$; input transition times $\leq 20 \text{ ns}$

	V_{DD} V	symbol	min.	typ.	max.	typical extrapolation formula	
Propagation delays $CP_0, \overline{CP}_1 \rightarrow O_n$ HIGH to LOW	5	t_{PHL}		170	340 ns	$143 \text{ ns} + (0,55 \text{ ns/pF}) C_L$	
	10			75	145 ns	$64 \text{ ns} + (0,23 \text{ ns/pF}) C_L$	
	15			50	105 ns	$42 \text{ ns} + (0,16 \text{ ns/pF}) C_L$	
LOW to HIGH	5	t_{PLH}		145	290 ns	$118 \text{ ns} + (0,55 \text{ ns/pF}) C_L$	
	10			65	130 ns	$54 \text{ ns} + (0,23 \text{ ns/pF}) C_L$	
	15			50	100 ns	$42 \text{ ns} + (0,16 \text{ ns/pF}) C_L$	
MR $\rightarrow O_n$ HIGH to LOW	5	t_{PHL}		145	290 ns	$118 \text{ ns} + (0,55 \text{ ns/pF}) C_L$	
	10			60	120 ns	$49 \text{ ns} + (0,23 \text{ ns/pF}) C_L$	
	15			45	90 ns	$37 \text{ ns} + (0,16 \text{ ns/pF}) C_L$	
Output transition times HIGH to LOW	5	t_{THL}		60	120 ns	$10 \text{ ns} + (1,0 \text{ ns/pF}) C_L$	
	10			30	60 ns	$9 \text{ ns} + (0,42 \text{ ns/pF}) C_L$	
	15			20	40 ns	$6 \text{ ns} + (0,28 \text{ ns/pF}) C_L$	
LOW to HIGH	5	t_{TLH}		60	120 ns	$10 \text{ ns} + (1,0 \text{ ns/pF}) C_L$	
	10			30	60 ns	$9 \text{ ns} + (0,42 \text{ ns/pF}) C_L$	
	15			20	40 ns	$6 \text{ ns} + (0,28 \text{ ns/pF}) C_L$	
Minimum CP_0 pulse width; LOW	5	t_{WCPL}	165	85	ns		
	10			65	30	ns	
	15			45	25	ns	
Minimum \overline{CP}_1 pulse width; HIGH	5	t_{WCPH}	165	85	ns		
	10			65	30	ns	
	15			45	25	ns	
Minimum MR pulse width; HIGH	5	t_{WMRH}	90	45	ns		
	10			40	20	ns	
	15			30	15	ns	
Recovery time for MR	5	t_{RMR}	50	25	ns	see also waveforms Figs 4 and 5	
	10			30	15		ns
	15			20	10		ns
Set-up times $CP_0 \rightarrow \overline{CP}_1$	5	t_{su}	180	90	ns		
	10			70	35	ns	
	15			50	25	ns	
$\overline{CP}_1 \rightarrow CP_0$	5	t_{su}	150	75	ns		
	10			60	30	ns	
	15			40	20	ns	
Maximum clock pulse frequency	5	f_{max}	3	6	MHz		
	10			7	15	MHz	
	15			10	21	MHz	

A.C. CHARACTERISTICS

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^\circ\text{C}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	typical formula for P (μW)	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
Dynamic power dissipation per package (P)	5	$750 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	10	$3300 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$8100 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

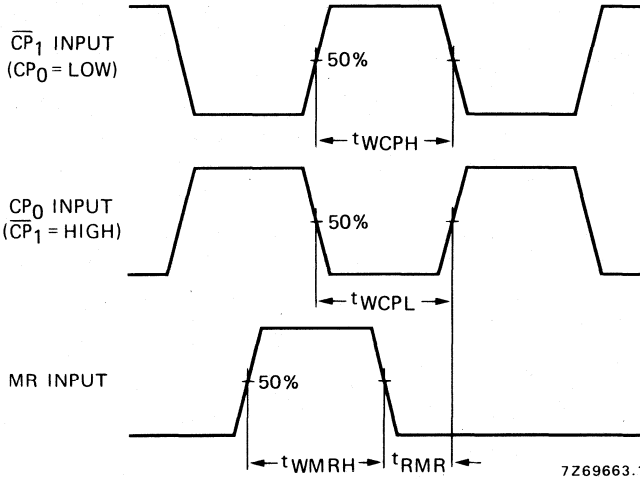


Fig. 4 Waveforms showing recovery time for MR; minimum CP_0 , CP_1 and MR pulse widths.

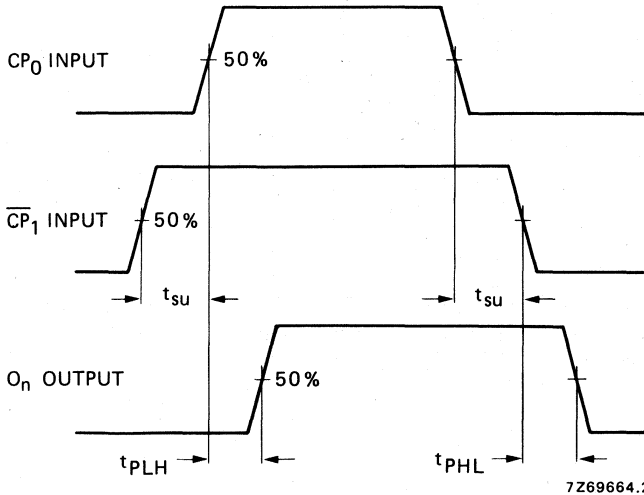


Fig. 5 Waveforms showing set-up times for CP_0 to CP_1 and CP_1 to CP_0 , and propagation delays.

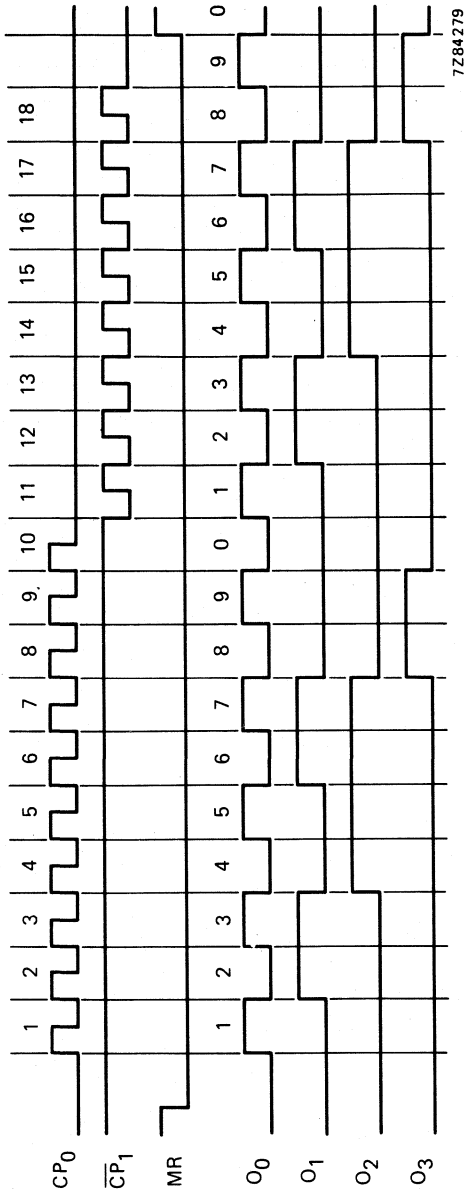


Fig. 6 Timing diagram.

QUADRUPLE 2-INPUT MULTIPLEXER



The HEF4519B provides four multiplexing circuits with common select inputs (S_A , S_B); each circuit contains two inputs (A_n , B_n) and one output (O_n). It may be used to select four bits of information from one of two sources.

The 'A' inputs are selected when S_A is HIGH, the 'B' inputs when S_B is HIGH. When S_A and S_B are HIGH, the output (O_n) is the logical EXCLUSIVE-NOR of the A_n and B_n inputs ($O_n = A_n \odot B_n$).

When S_A and S_B are LOW, the output (O_n) is LOW, independent of the multiplexer inputs (A_n and B_n).

The HEF4519B cannot be used to multiplex analogue signals. The outputs utilize standard buffers for best performance.

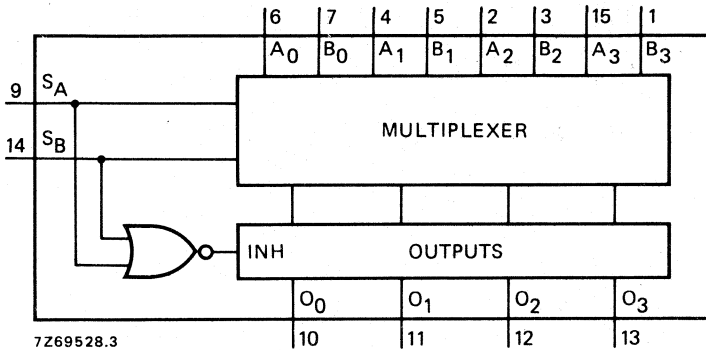


Fig. 1 Functional diagram.



Fig. 2 Pinning diagram.

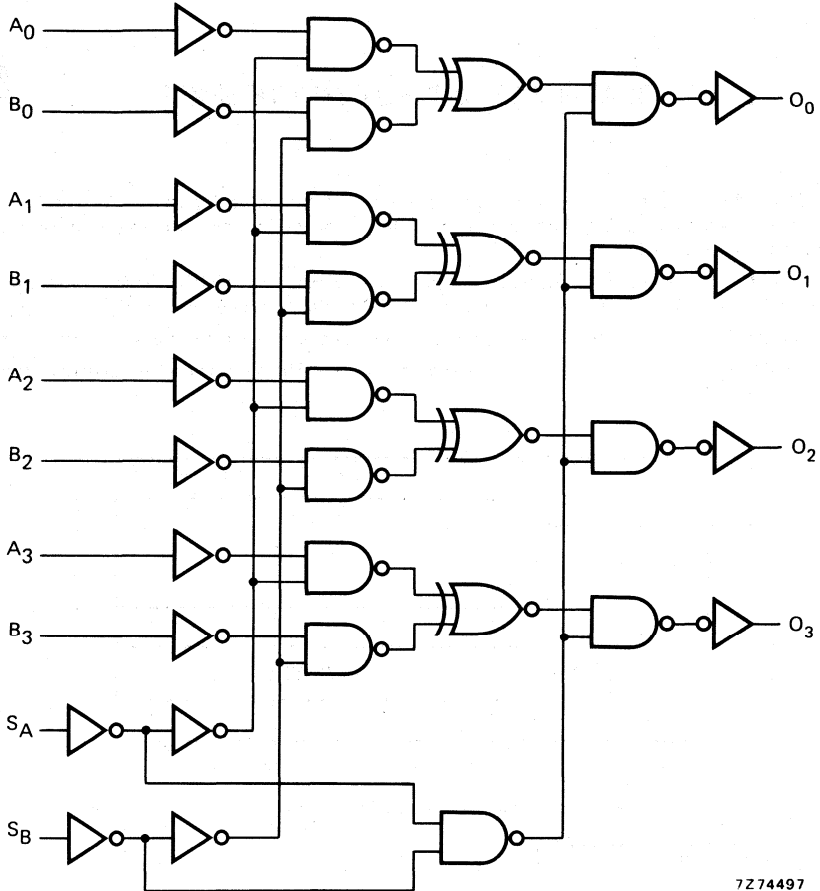
- HEF4519BP: 16-lead DIL; plastic (SOT-38Z).
- HEF4519BD: 16-lead DIL; ceramic (SOT-74).
- HEF4519BT: 16-lead flat pack; plastic (SO-16; SOT-109A).

PINNING

- S_A , S_B selects inputs (active HIGH)
- A_0 to A_3 multiplexer inputs
- B_0 to B_3 multiplexer inputs
- O_0 to O_3 multiplexer outputs

FAMILY DATA

I_{DD} LIMITS category MSI } see Family Specifications



7Z74497

Fig. 3 Logic diagram.

FUNCTION TABLE

inputs				output
S_A	S_B	A_n	B_n	O_n
L	L	X	X	L
H	L	A_n	X	A_n
L	H	X	B_n	B_n
H	H	L	L	H
H	H	H	L	L
H	H	L	H	L
H	H	H	H	H

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

A.C. CHARACTERISTICS

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	symbol	typ.	max.		typical extrapolation formula
Propagation delays $A_n, B_n \rightarrow O_n$ HIGH to LOW	5	t _{PHL}	100	200	ns	$73\text{ ns} + (0,55\text{ ns/pF})C_L$
	10		45	90	ns	$34\text{ ns} + (0,23\text{ ns/pF})C_L$
	15		35	65	ns	$27\text{ ns} + (0,16\text{ ns/pF})C_L$
LOW to HIGH	5	t _{PLH}	90	180	ns	$63\text{ ns} + (0,55\text{ ns/pF})C_L$
	10		40	80	ns	$29\text{ ns} + (0,23\text{ ns/pF})C_L$
	15		30	60	ns	$22\text{ ns} + (0,16\text{ ns/pF})C_L$
$S_A, S_B \rightarrow O_n$ HIGH to LOW	5	t _{PHL}	95	190	ns	$68\text{ ns} + (0,55\text{ ns/pF})C_L$
	10		40	80	ns	$29\text{ ns} + (0,23\text{ ns/pF})C_L$
	15		30	55	ns	$22\text{ ns} + (0,16\text{ ns/pF})C_L$
LOW to HIGH	5	t _{PLH}	85	165	ns	$58\text{ ns} + (0,55\text{ ns/pF})C_L$
	10		40	80	ns	$29\text{ ns} + (0,23\text{ ns/pF})C_L$
	15		30	60	ns	$22\text{ ns} + (0,16\text{ ns/pF})C_L$
Output transition times HIGH to LOW	5	t _{THL}	60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF})C_L$
	10		30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF})C_L$
	15		20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF})C_L$
LOW to HIGH	5	t _{TLH}	60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF})C_L$
	10		30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF})C_L$
	15		20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF})C_L$

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$1000 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz)
	10	$6000 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_o = output freq. (MHz)
	15	$17\,000 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	C_L = load capacitance (pF)
			$\Sigma(f_o C_L)$ = sum of outputs
			V_{DD} = supply voltage (V)

APPLICATION INFORMATION

Some examples of applications for the HEF4519B are:

- 2-input multiplexers.
- True/complement selectors.

DUAL BINARY COUNTER



The HEF4520B is a dual 4-bit internally synchronous binary counter. The counter has an active HIGH clock input (CP_0) and an active LOW clock input (\overline{CP}_1), buffered outputs from all four bit positions (O_0 to O_3) and an active HIGH overriding asynchronous master reset input (MR). The counter advances on either the LOW to HIGH transition of the CP_0 input if \overline{CP}_1 is HIGH or the HIGH to LOW transition of the \overline{CP}_1 input if CP_0 is LOW. Either CP_0 or \overline{CP}_1 may be used as the clock input to the counter and the other clock input may be used as a clock enable input. A HIGH on MR resets the counter (O_0 to $O_3 = \text{LOW}$) independent of CP_0 , \overline{CP}_1 .

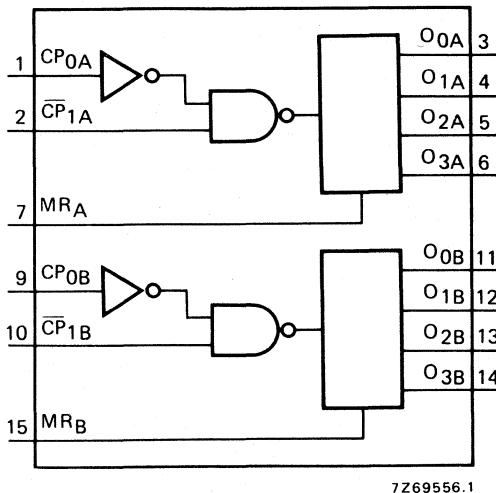


Fig. 1 Functional diagram.

PINNING

CP_{0A} , CP_{0B} clock inputs (L to H triggered)
 \overline{CP}_{1A} , \overline{CP}_{1B} clock inputs (H to L triggered)
 MR_A , MR_B master reset inputs
 O_{0A} to O_{3A} outputs
 O_{0B} to O_{3B} outputs

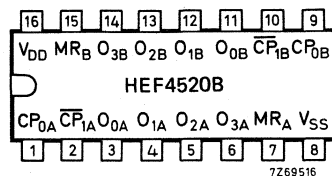


Fig. 2 Pinning diagram.

HEF4520BP: 16-lead DIL; plastic (SOT-38Z).
 HEF4520BD: 16-lead DIL; ceramic (SOT-74).
 HEF4520BT: 16-lead flat pack; plastic (SO-16; SOT-109A).

FAMILY DATA

} see Family Specifications

I_{DD} LIMITS category MSI

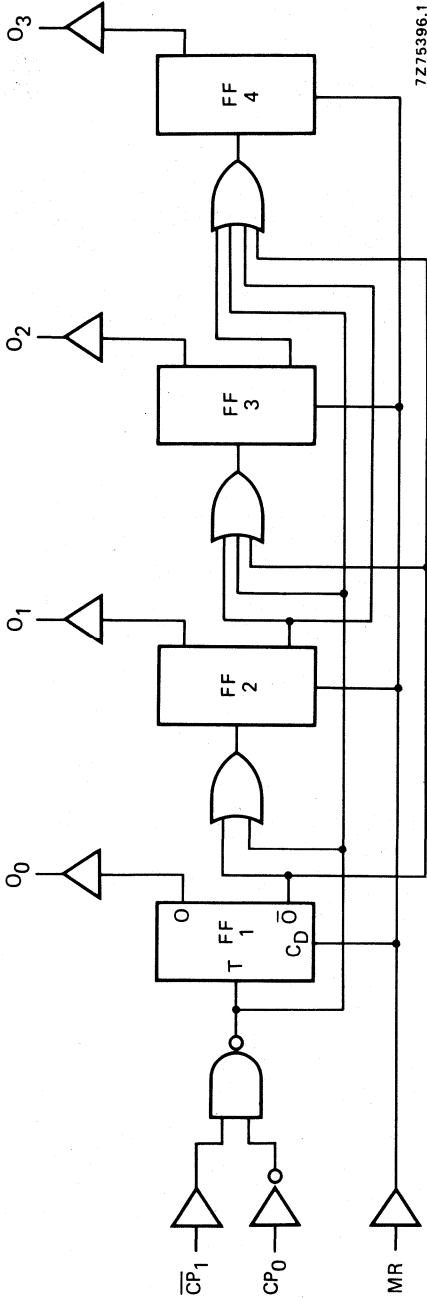


Fig. 3 Logic diagram (one counter).

H = HIGH state (the more positive voltage)
 L = LOW state (the less positive voltage)
 X = state is immaterial
 / = positive-going transition
 \ = negative-going transition

FUNCTION TABLE

CP0	CP1	MR	mode
/	H	L	counter advances
L	\	L	counter advances
\	X	L	no change
X	/	L	no change
/	H	L	no change
H	\	L	no change
X	X	H	O ₀ to O ₃ = LOW

A.C. CHARACTERISTICS

 $V_{SS} = 0 \text{ V}$; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$; $C_L = 50 \text{ pF}$; input transition times $\leq 20 \text{ ns}$

	V_{DD} V	symbol	min.	typ.	max.	typical extrapolation formula
Propagation delays $CP_0, \overline{CP_1} \rightarrow O_n$ HIGH to LOW	5	t _{PHL}		170	340 ns	143 ns + (0,55 ns/pF) C _L
	10		75	145 ns	64 ns + (0,23 ns/pF) C _L	
	15		50	105 ns	42 ns + (0,16 ns/pF) C _L	
LOW to HIGH	5	t _{PLH}		145	290 ns	118 ns + (0,55 ns/pF) C _L
	10		65	130 ns	54 ns + (0,23 ns/pF) C _L	
	15		50	100 ns	42 ns + (0,16 ns/pF) C _L	
MR $\rightarrow O_n$ HIGH to LOW	5	t _{PHL}		145	290 ns	118 ns + (0,55 ns/pF) C _L
	10		60	120 ns	49 ns + (0,23 ns/pF) C _L	
	15		45	90 ns	37 ns + (0,16 ns/pF) C _L	
Output transition times HIGH to LOW	5	t _{THL}		60	120 ns	10 ns + (1,0 ns/pF) C _L
	10		30	60 ns	9 ns + (0,42 ns/pF) C _L	
	15		20	40 ns	6 ns + (0,28 ns/pF) C _L	
LOW to HIGH	5	t _{TLH}		60	120 ns	10 ns + (1,0 ns/pF) C _L
	10		30	60 ns	9 ns + (0,42 ns/pF) C _L	
	15		20	40 ns	6 ns + (0,28 ns/pF) C _L	
Minimum CP ₀ pulse width; LOW	5	t _{WCPL}	165	85	ns	see also waveforms Figs 4 and 5
	10		65	30	ns	
	15		45	25	ns	
Minimum $\overline{CP_1}$ pulse width; HIGH	5	t _{WCPH}	165	85	ns	
	10		65	30	ns	
	15		45	25	ns	
Minimum MR pulse width; HIGH	5	t _{WMRH}	90	45	ns	
	10		40	20	ns	
	15		30	15	ns	
Recovery time for MR	5	t _{RMRR}	50	25	ns	
	10		30	15	ns	
	15		20	10	ns	
Set-up times $CP_0 \rightarrow \overline{CP_1}$	5	t _{su}	180	90	ns	
	10		70	35	ns	
	15		50	25	ns	
$\overline{CP_1} \rightarrow CP_0$	5	t _{su}	150	75	ns	
	10		60	30	ns	
	15		40	20	ns	
Maximum clock pulse frequency	5	f _{max}	3	6	MHz	
	10		7	15	MHz	
	15		10	21	MHz	

A.C. CHARACTERISTICS

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^\circ\text{C}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	typical formula for P (μW)	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
Dynamic power dissipation per package (P)	5	$750 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	10	$3300 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$8100 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

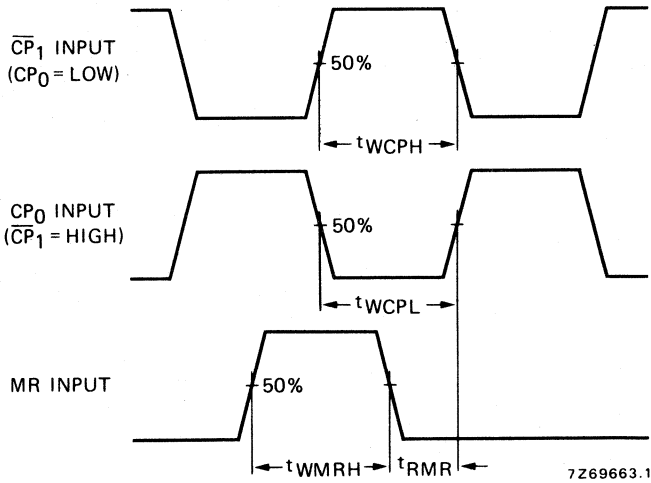


Fig. 4 Waveforms showing recovery time for MR; minimum CP_0 , \overline{CP}_1 and MR pulse widths.

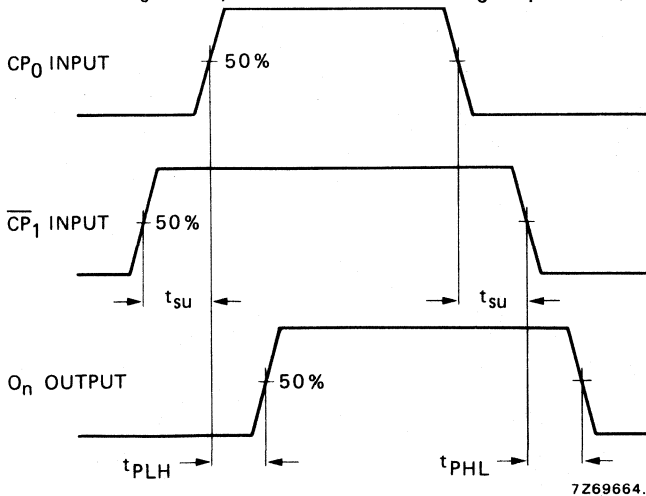
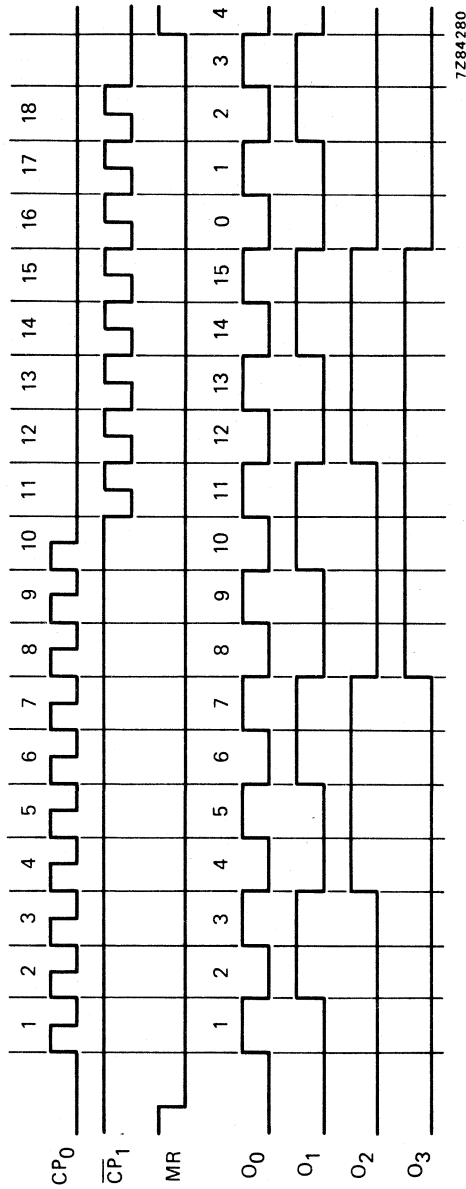


Fig. 5 Waveforms showing set-up times for CP_0 to \overline{CP}_1 and \overline{CP}_1 to CP_0 , and propagation delays.



7284280

Fig. 6 Timing diagram.



24-STAGE FREQUENCY DIVIDER

The HEF4521B consists of a chain of 24 toggle flip-flops with an overriding asynchronous master reset input (MR), and an input circuit that allows three modes of operation. The single inverting stage (I_2/O_2) will function as a crystal oscillator, or in combination with I_1 as an RC oscillator, or as an input buffer for an external oscillator. Low-power operation as a crystal oscillator is enabled by connecting external resistors to pins 3 (V_{SS}') and 5 (V_{DD}'). Each flip-flop divides the frequency of the previous flip-flop by two, consequently the HEF4521B will count up to $2^{24} = 16\,777\,216$. The counting advances on the HIGH to LOW transition of the clock (I_2). The outputs of the last seven stages are available for additional flexibility.

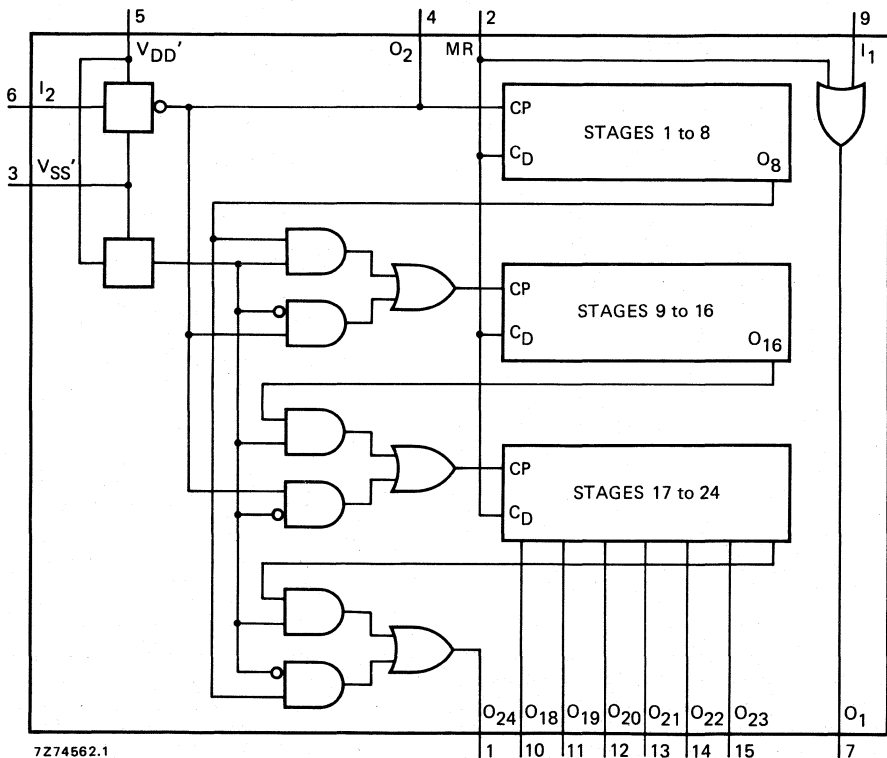


Fig. 1 Functional diagram.

FAMILY DATA
 I_{DD} LIMITS category MSI } see Family Specifications

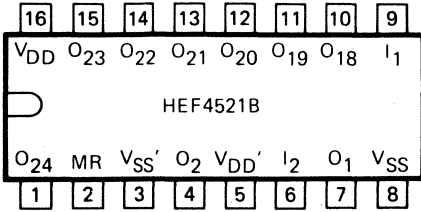


Fig. 2 Pinning diagram. 7274563

HEF4521BP: 16-lead DIL; plastic (SOT-38Z).
HEF4521BD: 16-lead DIL; ceramic (SOT-74).
HEF4521BT: 16-lead flat pack; plastic (SO-16; SOT-109A).

COUNT CAPACITY

output	count capacity
O18	2 ¹⁸ = 262 144
O19	2 ¹⁹ = 524 288
O20	2 ²⁰ = 1 048 576
O21	2 ²¹ = 2 097 152
O22	2 ²² = 4 194 304
O23	2 ²³ = 8 388 608
O24	2 ²⁴ = 16 777 216

FUNCTIONAL TEST SEQUENCE

inputs		control terminals			outputs	remarks
MR	I ₂	O ₂	V _{SS} '	V _{DD} '	O ₁₈ to O ₂₄	
H	L	L	V _{DD}	V _{SS}	L	counter is in three 8-stage sections in parallel mode; I ₂ and O ₂ are interconnected (O ₂ is now input); counter is reset by MR
L	⌈	⌈	V _{DD}	V _{SS}	H	255 pulses are clocked into I ₂ , O ₂ (the counter advances on the LOW to HIGH transition)
L	L	L	V _{SS}	V _{SS}	H	V _{SS} ' is connected to V _{SS}
L	H	L	V _{SS}	V _{SS}	H	the input I ₂ is made HIGH
L	H	L	V _{SS}	V _{DD}	H	V _{DD} ' is connected to V _{DD} ; O ₂ is now made floating and becomes an output; the device is now in the 2 ²⁴ mode
L	∖		V _{SS}	V _{DD}	L	counter ripples from an all HIGH state to an all LOW state

A test function has been included for the reduction of the test time required to exercise all 24 counter stages. This test function divides the counter into three 8-stage sections by connecting V_{SS}' to V_{DD} and V_{DD}' to V_{SS}. Via I₂ (connected to O₂) 255 counts are loaded into each of the 8-stage sections in parallel. All flip-flops are now at a HIGH state. The counter is now returned to the normal 24-stage in series configuration by connecting V_{SS}' to V_{SS} and V_{DD}' to V_{DD}. One more pulse is entered into input I₂, which will cause the counter to ripple from an all HIGH state to an all LOW state.

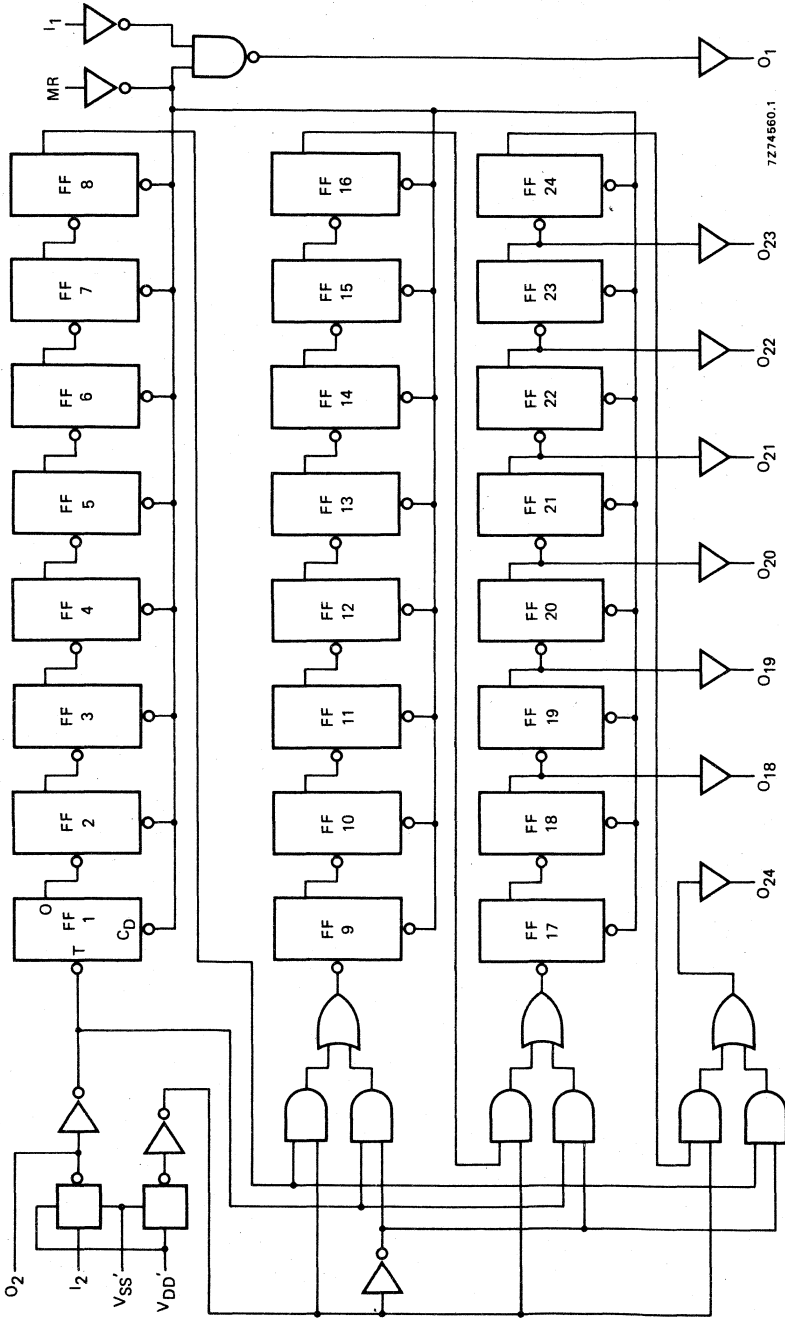


Fig. 3 Logic diagram; for schematic diagram of clock circuit see Fig. 4.

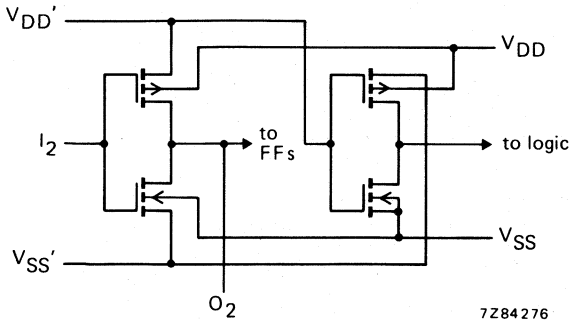


Fig. 4 Schematic diagram of clock input circuitry.

A.C. CHARACTERISTICS

VSS = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V _{DD} V	symbol	min.	typ.	max.	typical extrapolation formula
Propagation delays I ₂ → O ₁₈ HIGH to LOW	5	t _{PHL}		950	1900 ns	923 ns + (0,55 ns/pF) C _L
	10		350	700 ns	339 ns + (0,23 ns/pF) C _L	
	15		220	440 ns	212 ns + (0,16 ns/pF) C _L	
LOW to HIGH	5	t _{PLH}		950	1900 ns	923 ns + (0,55 ns/pF) C _L
	10		350	700 ns	339 ns + (0,23 ns/pF) C _L	
	15		220	440 ns	212 ns + (0,16 ns/pF) C _L	
O _n → O _{n+1} HIGH to LOW	5	t _{PHL}		40	80 ns	13 ns + (0,55 ns/pF) C _L
	10		15	30 ns	4 ns + (0,23 ns/pF) C _L	
	15		10	20 ns	2 ns + (0,16 ns/pF) C _L	
LOW to HIGH	5	t _{PLH}		15	40 ns	13 ns + (0,55 ns/pF) C _L
	10		10	30 ns	0 ns + (0,23 ns/pF) C _L	
	15		8	20 ns	0 ns + (0,16 ns/pF) C _L	
MR → O _n HIGH to LOW	5	t _{PHL}		120	240 ns	93 ns + (0,55 ns/pF) C _L
	10		55	110 ns	44 ns + (0,23 ns/pF) C _L	
	15		40	80 ns	32 ns + (0,16 ns/pF) C _L	
I ₁ → O ₁ HIGH to LOW	5	t _{PHL}		90	180 ns	63 ns + (0,55 ns/pF) C _L
	10		35	70 ns	24 ns + (0,23 ns/pF) C _L	
	15		25	50 ns	17 ns + (0,16 ns/pF) C _L	
LOW to HIGH	5	t _{PLH}		60	120 ns	33 ns + (0,55 ns/pF) C _L
	10		30	60 ns	19 ns + (0,23 ns/pF) C _L	
	15		20	40 ns	12 ns + (0,16 ns/pF) C _L	
Output transition times HIGH to LOW	5	t _{THL}		60	120 ns	10 ns + (1,0 ns/pF) C _L
	10		30	60 ns	9 ns + (0,42 ns/pF) C _L	
	15		20	40 ns	6 ns + (0,28 ns/pF) C _L	
LOW to HIGH	5	t _{TLH}		60	120 ns	10 ns + (1,0 ns/pF) C _L
	10		30	60 ns	9 ns + (0,42 ns/pF) C _L	
	15		20	40 ns	6 ns + (0,28 ns/pF) C _L	

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V _{DD} V	symbol	min.	typ.	max.	
Minimum I ₂ pulse width; HIGH	5	t _{WI2H}	80	40	ns	} see also waveforms Fig. 5
	10		40	20	ns	
	15		30	15	ns	
Minimum MR pulse width; HIGH	5	t _{WMRH}	70	35	ns	
	10		40	20	ns	
	15		30	15	ns	
Recovery time for MR	5	t _{RMR}	20	-10	ns	
	10		15	-5	ns	
	15		15	0	ns	
Maximum clock pulse frequency	5	f _{max}	6	12	MHz	
	10		12	25	MHz	
	15		17	35	MHz	

	V _{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	1 200 f _i + Σ(f _o C _L) × V _{DD} ²	f _i = input freq. (MHz)
	10	5 100 f _i + Σ(f _o C _L) × V _{DD} ²	f _o = output freq. (MHz)
	15	13 050 f _i + Σ(f _o C _L) × V _{DD} ²	C _L = load capacitance (pF)
			Σ(f _o C _L) = sum of outputs
			V _{DD} = supply voltage (V)

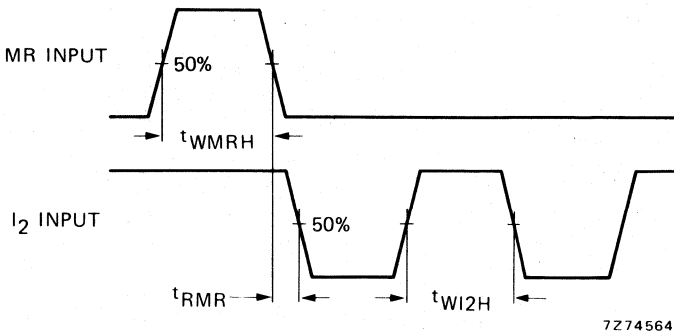
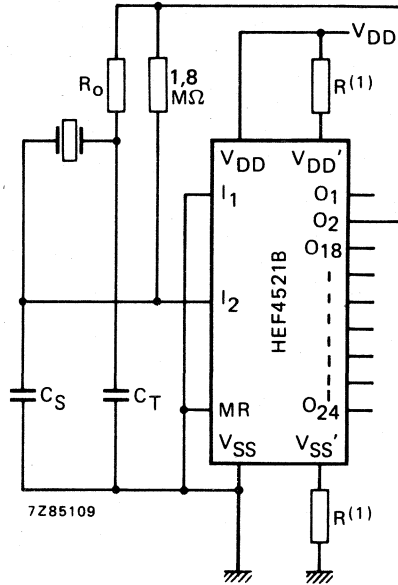


Fig. 5 Waveforms showing minimum pulse widths for MR and I₂, recovery time for MR.

APPLICATION INFORMATION



(1) Optional for low power operation.
Fig. 6 Crystal oscillator circuit.

Typical characteristics for crystal oscillator circuit (Fig. 6):

	500 kHz circuit	50 kHz circuit	unit
Crystal characteristics			
resonance frequency	500	50	kHz
crystal cut	S	N	—
equivalent resistance; R_S	1	6,2	k Ω
External resistor/capacitor values			
R_0	47	750	k Ω
C_T	82	82	pF
C_S	20	20	pF

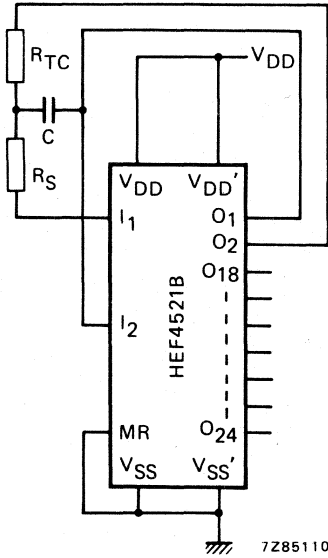
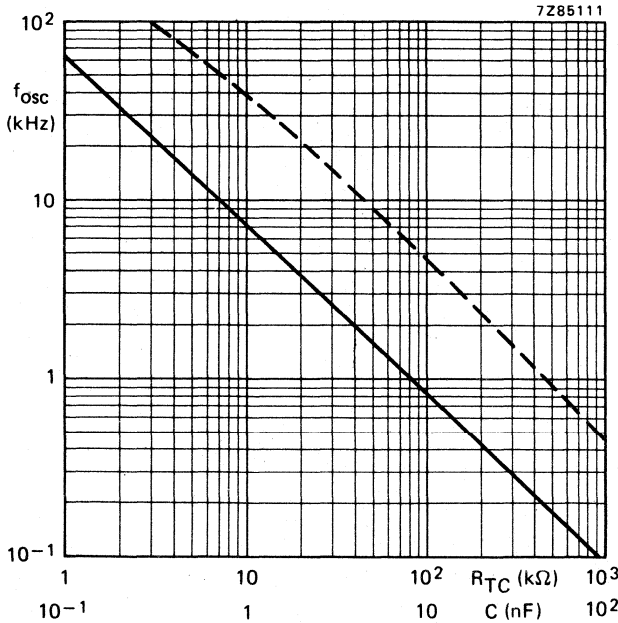


Fig. 7 RC oscillator circuit;

$$f \approx \frac{1}{2,3 \times R_{TC} \times C}; R_S \geq 2 R_{TC}, \text{ in which:}$$

f in Hz, R in Ω , C in F.



— $R_{TC}; C = 1 \text{ nF}; R_S \approx 2 R_{TC}$
 - - - $C; R_{TC} = 56 \text{ k}\Omega;$
 . . . $R_S = 120 \text{ k}\Omega$

Fig. 8 Oscillator frequency as a function of R_{TC} and C ; $V_{DD} = 10 \text{ V}$; test circuit is Fig. 7.

APPLICATION INFORMATION (continued)

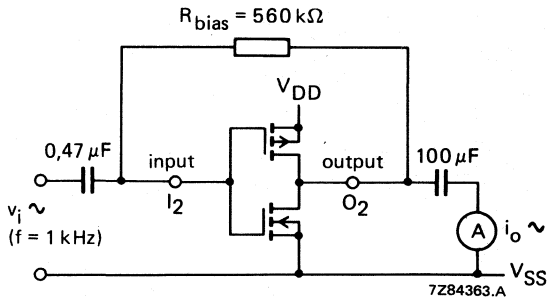
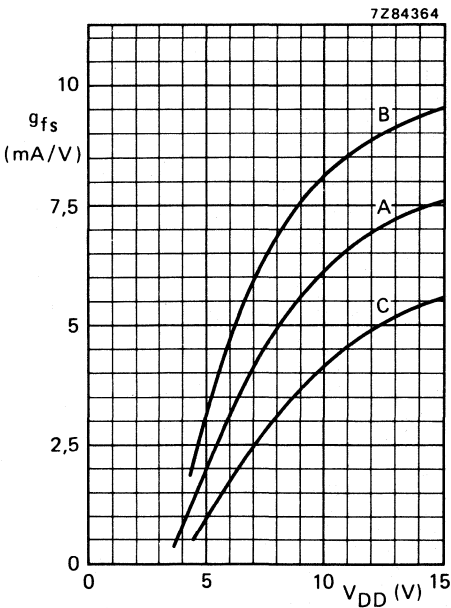


Fig. 9 Test set-up for measuring forward transconductance $g_{fs} = di_o/dv_i$ at v_o is constant (see also graph Fig. 10).



Curves in Fig. 10:

- A: average,
- B: average + 2 s,
- C: average - 2 s, in which:
's' is the observed standard deviation.

Fig. 10 Typical forward transconductance g_{fs} as a function of the supply voltage at $T_{amb} = 25\text{ }^{\circ}\text{C}$.

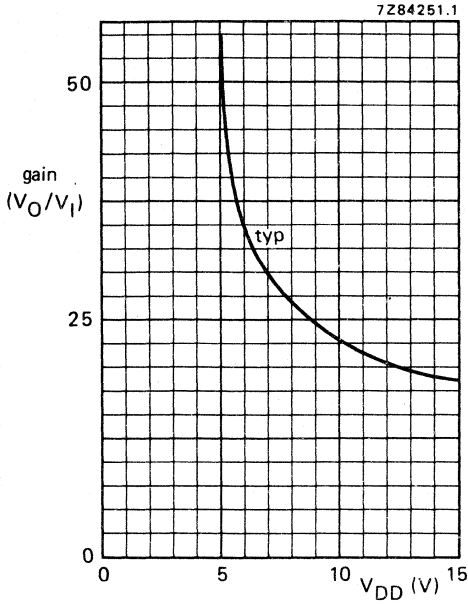


Fig. 11 Voltage gain (V_O/V_I) as a function of supply voltage.

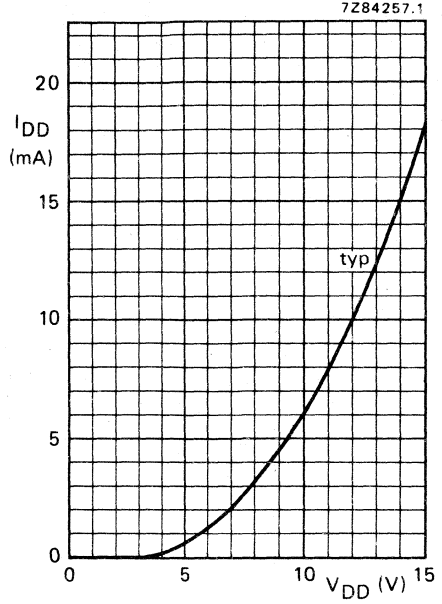


Fig. 12 Supply current as a function of supply voltage.

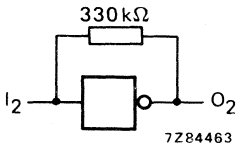


Fig. 13 Test set-up for measuring graphs of Figs 11 and 12.



PROGRAMMABLE 4-BIT BCD DOWN COUNTER



The HEF4522B is a synchronous programmable 4-bit BCD down counter with an active HIGH and an active LOW clock input (CP_0 , \overline{CP}_1), an asynchronous parallel load input (PL), four parallel inputs (P_0 to P_3), a cascade feedback input (CF), four buffered parallel outputs (O_0 to O_3), a terminal count output (TC) and an overriding asynchronous master reset input (MR).

This device is a programmable, cascadable down counter with a decoded TC output for divide-by-n applications. In single stage applications the TC output is connected to PL. CF allows cascade divide-by-n operation with no additional gates required.

Information on P_0 to P_3 is loaded into the counter while PL is HIGH, independent of all other input conditions except MR, which must be LOW. When PL and \overline{CP}_1 are LOW, the counter advances on a LOW to HIGH transition of CP_0 . When PL is LOW and CP_0 is HIGH, the counter advances on a HIGH to LOW transition of \overline{CP}_1 . TC is HIGH when the counter is in the zero state ($O_0 = O_1 = O_2 = O_3 = \text{LOW}$) and CF is HIGH and PL is LOW. A HIGH on MR resets the counter (O_0 to $O_3 = \text{LOW}$) independent of other input conditions.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to clock rise and fall times.

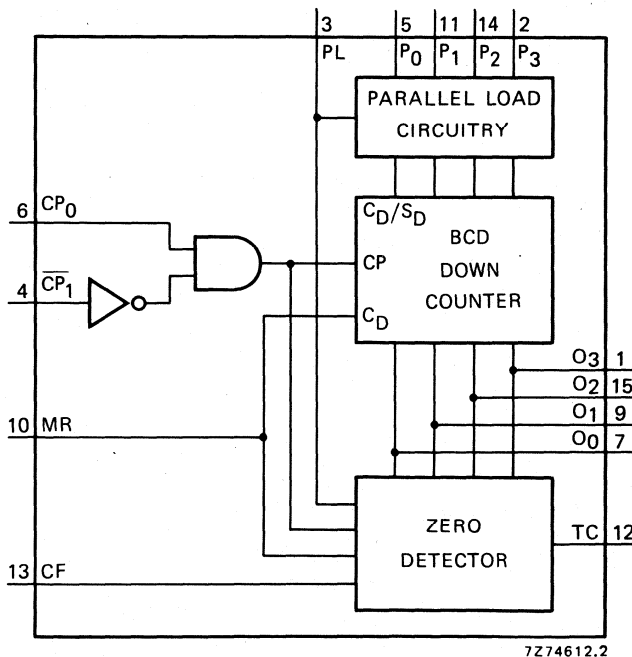


Fig. 1 Functional diagram.

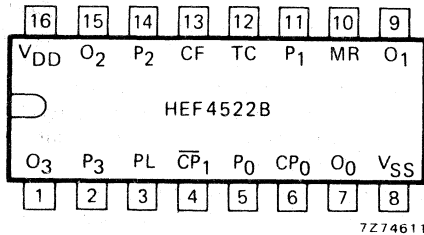
FAMILY DATA

I_{DD} LIMITS category MSI

} see Family Specifications

HEF4522B

MSI



HEF4522BP: 16-lead DIL; plastic (SOT-38Z).
 HEF4522BD: 16-lead DIL; ceramic (SOT-74).
 HEF4522BT: 16-lead flat pack; plastic (SO-16; SOT-109A).

Fig. 2 Pinning diagram.

PINNING

- PL parallel load input
- P₀ to P₃ parallel inputs
- CF cascade feedback input
- CP₀ clock input (LOW to HIGH, triggered)
- CP₁ clock input (HIGH to LOW, triggered)
- MR asynchronous master reset input
- TC terminal count output
- O₀ to O₃ buffered parallel outputs

COUNTING MODE

CF = HIGH; PL = LOW; MR = LOW

FUNCTION TABLE

count	outputs			
	O ₃	O ₂	O ₁	O ₀
9	H	L	L	H
8	H	L	L	L
7	L	H	H	H
6	L	H	H	L
5	L	H	L	H
4	L	H	L	L
3	L	L	H	H
2	L	L	H	L
1	L	L	L	H
0	L	L	L	L

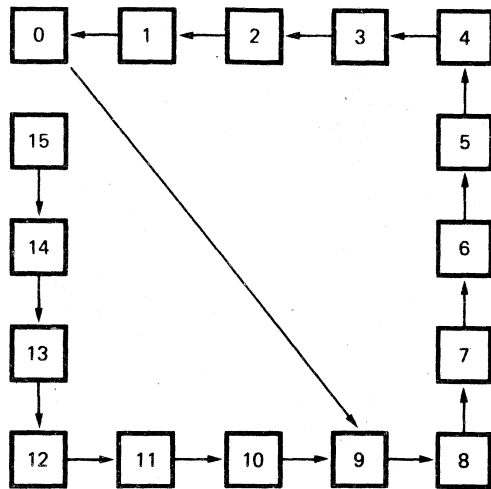
MR	PL	CP ₀	CP ₁	mode
H	X	X	X	reset (asynchronous)
L	H	X	X	preset (asynchronous)
L	L	∕	H	no change
L	L	L	∖	no change
L	L	∖	X	no change
L	L	X	∕	no change
L	L	∕	L	counter advances
L	L	H	∖	counter advances

H = HIGH state (the more positive voltage)
 L = LOW state (the less positive voltage)
 X = state is immaterial
 ∕ = positive-going transition
 ∖ = negative-going transition

SINGLE STAGE OPERATION

Divide-by-n; MR = LOW; CF = HIGH; \overline{CP}_1 = LOW

PL	P ₃	P ₂	P ₁	P ₀	divide by	TC output pulse width
L	X	X	X	X	10	one clock period
TC	H	H	H	H	15	clock pulse HIGH
TC	H	H	H	L	14	
TC	H	H	L	H	13	
TC	H	H	L	L	12	
TC	H	L	H	H	11	
TC	H	L	H	L	10	
TC	H	L	L	H	9	
TC	H	L	L	L	8	
TC	L	H	H	H	7	
TC	L	H	H	L	6	
TC	L	H	L	H	5	
TC	L	H	L	L	4	
TC	L	L	H	H	3	
TC	L	L	H	L	2	
TC	L	L	L	H	1	
TC	L	L	L	L	no operation	



7274617

Fig. 3 State diagram.

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ≤ 20 ns

	V _{DD} V	typical formula for P (μW)	where f _i = input freq. (MHz) f _o = output freq. (MHz) C _L = load capacitance (pF) Σ(f _o C _L) = sum of outputs V _{DD} = supply voltage (V)
Dynamic power dissipation per package (P)	5	1000 f _i + Σ(f _o C _L) × V _{DD} ²	
	10	4000 f _i + Σ(f _o C _L) × V _{DD} ²	
	15	10 000 f _i + Σ(f _o C _L) × V _{DD} ²	

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V _{DD} V	symbol	min.	typ.	max.	typical extrapolation formula	
Propagation delays CP ₀ , CP ₁ → O _n HIGH to LOW	5	t _{PHL}		150	300	ns	123 ns + (0,55 ns/pF) C _L
	10		65	130	ns	54 ns + (0,23 ns/pF) C _L	
	15		50	100	ns	42 ns + (0,16 ns/pF) C _L	
LOW to HIGH	5	t _{PLH}		150	300	ns	123 ns + (0,55 ns/pF) C _L
	10		65	130	ns	54 ns + (0,23 ns/pF) C _L	
	15		50	100	ns	42 ns + (0,16 ns/pF) C _L	
CP ₀ , CP ₁ → TC HIGH to LOW	5	t _{PHL}		210	420	ns	183 ns + (0,55 ns/pF) C _L
	10		90	180	ns	79 ns + (0,23 ns/pF) C _L	
	15		70	140	ns	62 ns + (0,16 ns/pF) C _L	
LOW to HIGH	5	t _{PLH}		210	420	ns	183 ns + (0,55 ns/pF) C _L
	10		90	180	ns	79 ns + (0,23 ns/pF) C _L	
	15		70	140	ns	62 ns + (0,16 ns/pF) C _L	
PL → O _n HIGH to LOW	5	t _{PHL}		200	400	ns	183 ns + (0,55 ns/pF) C _L
	10		80	160	ns	69 ns + (0,23 ns/pF) C _L	
	15		60	120	ns	52 ns + (0,16 ns/pF) C _L	
LOW to HIGH	5	t _{PLH}		180	360	ns	153 ns + (0,55 ns/pF) C _L
	10		70	140	ns	59 ns + (0,23 ns/pF) C _L	
	15		50	100	ns	42 ns + (0,16 ns/pF) C _L	
MR → O _n HIGH to LOW	5	t _{PHL}		140	280	ns	113 ns + (0,55 ns/pF) C _L
	10		55	110	ns	44 ns + (0,23 ns/pF) C _L	
	15		40	80	ns	32 ns + (0,16 ns/pF) C _L	
Output transition times HIGH to LOW	5	t _{THL}		60	120	ns	10 ns + (1,0 ns/pF) C _L
	10		30	60	ns	9 ns + (0,42 ns/pF) C _L	
	15		20	40	ns	6 ns + (0,28 ns/pF) C _L	
LOW to HIGH	5	t _{TLH}		60	120	ns	10 ns + (1,0 ns/pF) C _L
	10		30	60	ns	9 ns + (0,42 ns/pF) C _L	
	15		20	40	ns	6 ns + (0,28 ns/pF) C _L	

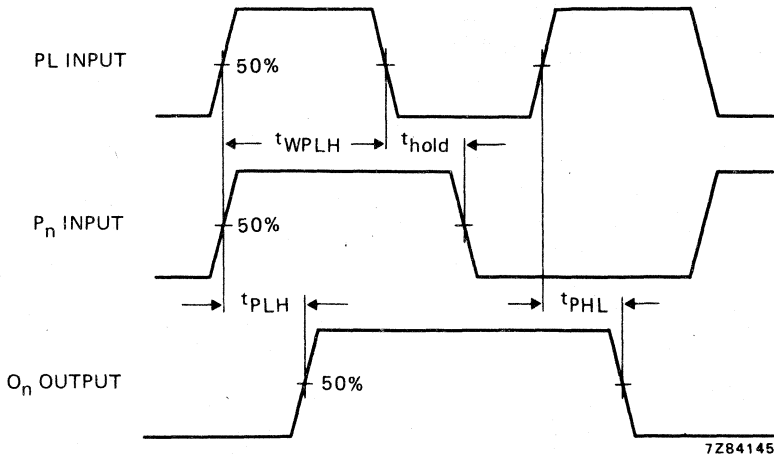
A.C. CHARACTERISTICS

$V_{SS} = 0 \text{ V}$; $T_{amb} = 25 \text{ }^\circ\text{C}$; $C_L = 50 \text{ pF}$; input transition times $\leq 20 \text{ ns}$

	V_{DD} V	symbol	min.	typ.	max.			
Minimum clock pulse width; CP_0 LOW	5	tWCPL	80	40	ns	} see also waveforms Figs 5 and 6		
	10		40	20	ns			
	15		30	15	ns			
Minimum clock pulse width; \overline{CP}_1 HIGH	5	tWCPH	80	40	ns		} see also waveforms Figs 5 and 6	
	10		40	20	ns			
	15		30	15	ns			
Minimum PL pulse width; HIGH	5	tWPLH	100	50	ns			} see also waveforms Figs 5 and 6
	10		40	20	ns			
	15		32	16	ns			
Minimum MR pulse width; HIGH	5	tWMRH	130	65	ns			
	10		50	25	ns			
	15		40	20	ns			
Hold time $P_n \rightarrow PL$	5	t _{hold}	70	35	ns	} see note		
	10		60	30	ns			
	15		50	25	ns			
Maximum clock pulse frequency PL = LOW	5	f _{max}	6	12	MHz		} see note	
	10		12	25	MHz			
	15		16	32	MHz			

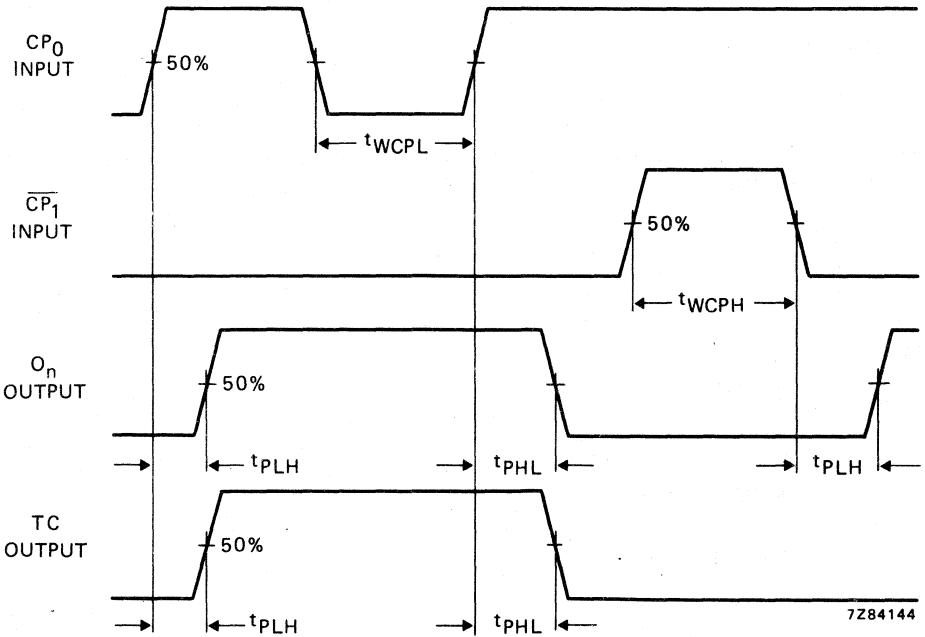
Note

In the divide-by-n mode (PL connected to TC), one has to observe the maximum HIGH to LOW propagation delay for CP to TC, before applying the next clock pulse.



7Z84145

Fig. 5 Waveforms showing minimum PL pulse width, propagation delays for PL, P_n to O_n and hold time for PL to P_n.



7Z84144

Fig. 6 Waveforms showing minimum CP₀ and CP₁ pulse widths, propagation delays for CP₀, CP₁ to O_n and TC.

APPLICATION INFORMATION

Some examples of applications for the HEF4522B are:

- Divide-by-n counter
- Programmable frequency divider

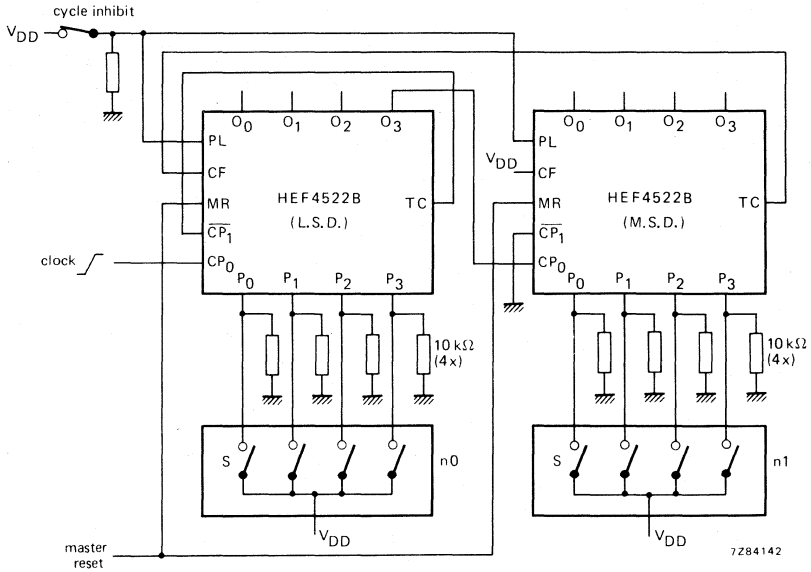
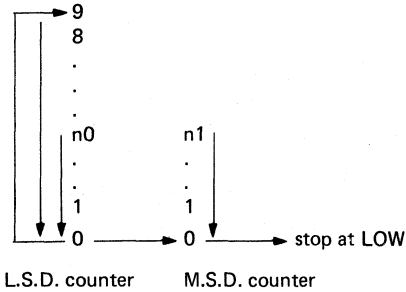


Fig. 7 Typical application of two HEF4522B circuits in a 2-stage programmable down counter (one cycle). S are thumbwheel switches; when open: LOW state.

Counting cycle:



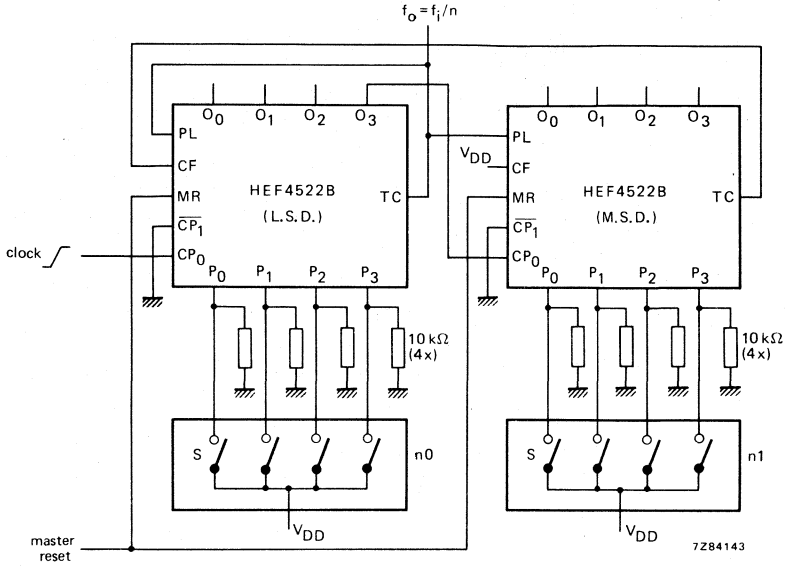
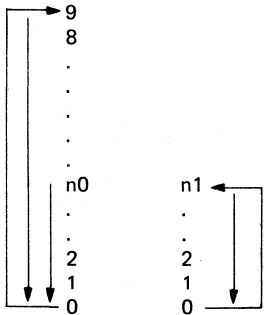


Fig. 8 Typical application of two HEF4522B circuits in a 2-stage programmable frequency divider. S are thumbwheel switches; when open: LOW state.

Counting cycle:



L.S.D. counter

M.S.D. counter

PROGRAMMABLE 4-BIT BINARY DOWN COUNTER



The HEF4526B is a synchronous programmable 4-bit binary down counter with an active HIGH and an active LOW clock input (CP_0 , \overline{CP}_1), an asynchronous parallel load input (PL), four parallel inputs (P_0 to P_3), a cascade feedback input (CF), four buffered parallel outputs (O_0 to O_3), a terminal count output (TC) and an overriding asynchronous master reset input (MR).

This device is a programmable, cascadable down counter with a decoded TC output for divide-by-n applications. In single stage applications the TC output is connected to PL. CF allows cascade divide-by-n operation with no additional gates required.

Information on P_0 to P_3 is loaded into the counter while PL is HIGH, independent of all other input conditions except MR, which must be LOW. When PL and \overline{CP}_1 are LOW, the counter advances on a LOW to HIGH transition of CP_0 . When PL is LOW and CP_0 is HIGH, the counter advances on a HIGH to LOW transition of \overline{CP}_1 . TC is HIGH when the counter is in the zero state ($O_0 = O_1 = O_2 = O_3 = \text{LOW}$) and CF is HIGH and PL is LOW. A HIGH on MR resets the counter (O_0 to $O_3 = \text{LOW}$) independent of other input conditions.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to clock rise and fall times.

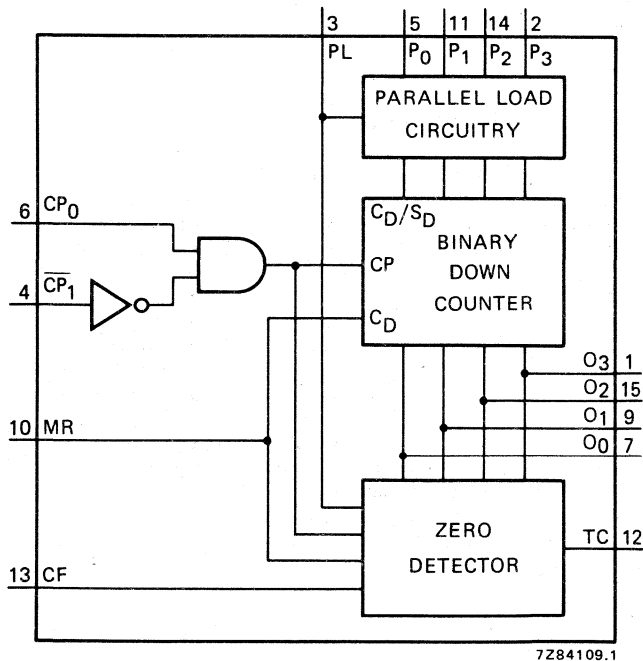


Fig. 1 Functional diagram.

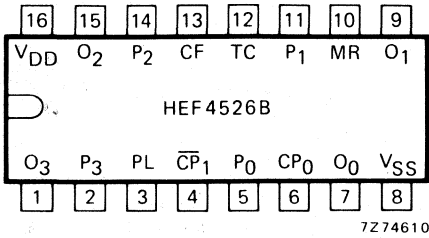
FAMILY DATA

I_{DD} LIMITS category MSI

} see Family Specifications

HEF4526B

MSI



HEF4526BP: 16-lead DIL; plastic (SOT-38Z).
 HEF4526BD: 16-lead DIL; ceramic (SOT-74).
 HEF4526BT: 16-lead flat pack; plastic (SO-16; SOT-109A).

Fig. 2 Pinning diagram.

PINNING

- PL parallel load input
- P₀ to P₃ parallel inputs
- CF cascade feedback input
- CP₀ clock input (LOW to HIGH, triggered)
- CP₁ clock input (HIGH to LOW, triggered)
- MR asynchronous master reset input
- TC terminal count output
- O₀ to O₃ buffered parallel outputs

COUNTING MODE

CF = HIGH; PL = LOW; MR = LOW

count	outputs			
	O ₃	O ₂	O ₁	O ₀
15	H	H	H	H
14	H	H	H	L
13	H	H	L	H
12	H	H	L	L
11	H	L	H	H
10	H	L	H	L
9	H	L	L	H
8	H	L	L	L
7	L	H	H	H
6	L	H	H	L
5	L	H	L	H
4	L	H	L	L
3	L	L	H	H
2	L	L	H	L
1	L	L	L	H
0	L	L	L	L

FUNCTION TABLE

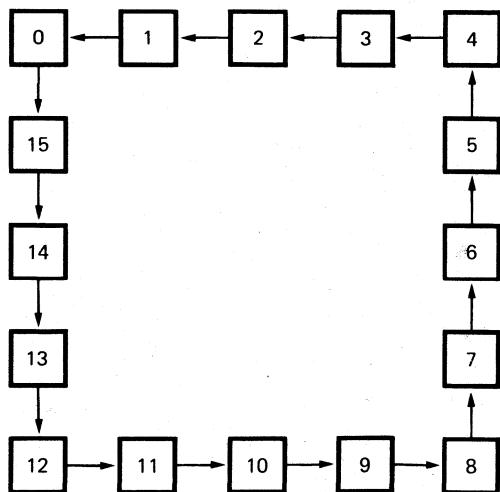
MR	PL	CP ₀	CP ₁	mode
H	X	X	X	reset (asynchronous)
L	H	X	X	preset (asynchronous)
L	L	/	H	no change
L	L	L	\	no change
L	L	\	X	no change
L	L	X	/	no change
L	L	/	L	counter advances
L	L	H	\	counter advances

H = HIGH state (the more positive voltage)
 L = LOW state (the less positive voltage)
 X = state is immaterial
 / = positive-going transition
 \ = negative-going transition

SINGLE STAGE OPERATION

Divide-by-n; MR = LOW; CF = HIGH; \overline{CP}_1 = LOW

PL	P ₃	P ₂	P ₁	P ₀	divide by	TC output pulse width
L	X	X	X	X	16	one clock period
TC	H	H	H	H	15	} clock pulse HIGH
TC	H	H	H	L	14	
TC	H	H	L	H	13	
TC	H	H	L	L	12	
TC	H	L	H	H	11	
TC	H	L	H	L	10	
TC	H	L	L	H	9	
TC	H	L	L	L	8	
TC	L	H	H	H	7	
TC	L	H	H	L	6	
TC	L	H	L	H	5	
TC	L	H	L	L	4	
TC	L	L	H	H	3	
TC	L	L	H	L	2	
TC	L	L	L	H	1	
TC	L	L	L	L	no operation	



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Fig. 3 State diagram.

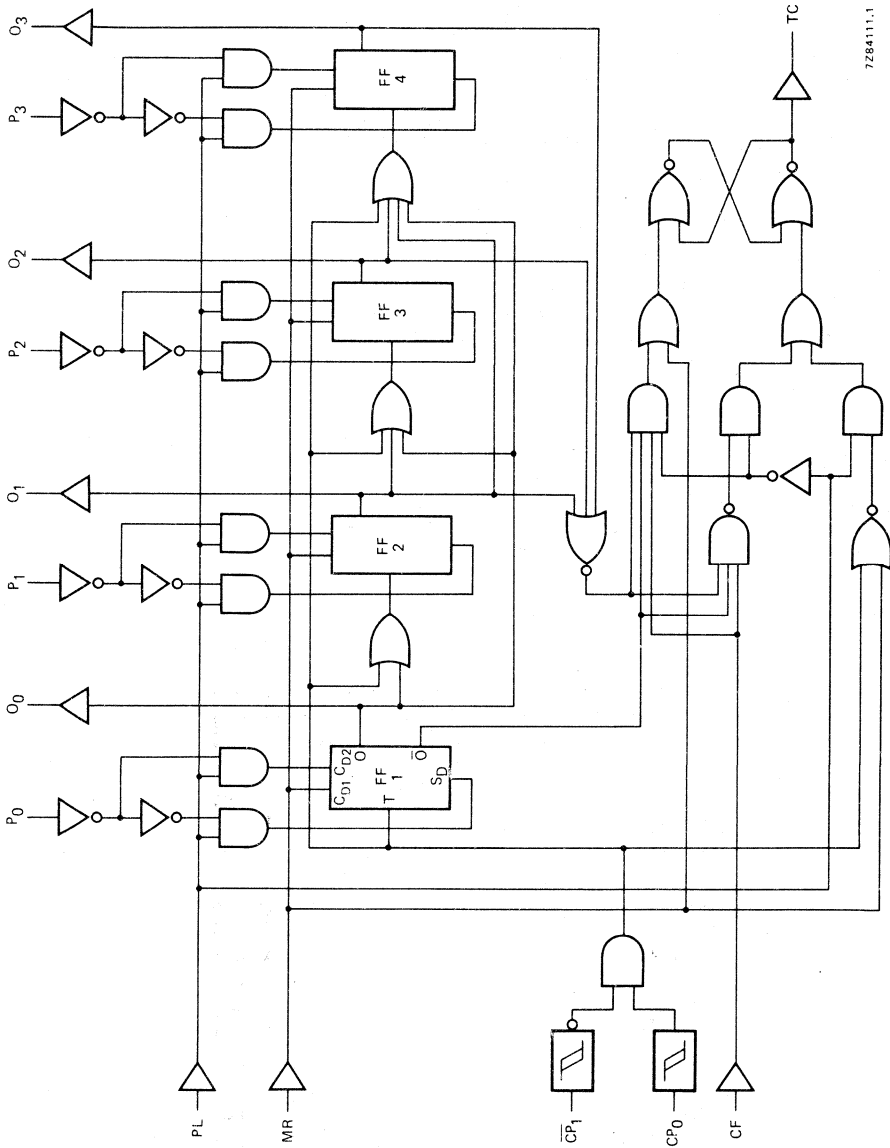


Fig. 4 Logic diagram.

A.C. CHARACTERISTICS

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^\circ\text{C}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	typical formula for P (μW)	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
Dynamic power dissipation per package (P)	5	$1000 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	10	$4000 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$10\,000 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

A.C. CHARACTERISTICS

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^\circ\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	symbol	min.	typ.	max.	typical extrapolation formula
Propagation delays $CP_0, \overline{CP}_1 \rightarrow O_n$ HIGH to LOW	5	tPHL	150	300	ns	$123\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10		65	130	ns	$54\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15		50	100	ns	$42\text{ ns} + (0,16\text{ ns/pF}) C_L$
LOW to HIGH	5	tPLH	150	300	ns	$123\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10		65	130	ns	$54\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15		50	100	ns	$42\text{ ns} + (0,16\text{ ns/pF}) C_L$
$CP_0, \overline{CP}_1 \rightarrow TC$ HIGH to LOW	5	tPHL	210	420	ns	$183\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10		90	180	ns	$79\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15		70	140	ns	$62\text{ ns} + (0,16\text{ ns/pF}) C_L$
LOW to HIGH	5	tPLH	210	420	ns	$183\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10		90	180	ns	$79\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15		70	140	ns	$62\text{ ns} + (0,16\text{ ns/pF}) C_L$
$PL \rightarrow O_n$ HIGH to LOW	5	tPHL	200	400	ns	$183\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10		80	160	ns	$69\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15		60	120	ns	$52\text{ ns} + (0,16\text{ ns/pF}) C_L$
LOW to HIGH	5	tPLH	180	360	ns	$153\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10		70	140	ns	$59\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15		50	100	ns	$42\text{ ns} + (0,16\text{ ns/pF}) C_L$
$MR \rightarrow O_n$ HIGH to LOW	5	tPHL	140	280	ns	$113\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10		55	110	ns	$44\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15		40	80	ns	$32\text{ ns} + (0,16\text{ ns/pF}) C_L$
Output transition times HIGH to LOW	5	tTHL	60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$
	10		30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$
	15		20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$
LOW to HIGH	5	tTLH	60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$
	10		30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$
	15		20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$

A.C. CHARACTERISTICS

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	symbol	min.	typ.	max.	
Minimum clock pulse width CP_0 LOW	5	t_{WCPL}	80	40	ns	} see also waveforms Figs 5 and 6
	10		40	20	ns	
	15		30	15	ns	
Minimum clock pulse width \overline{CP}_1 HIGH	5	t_{WCPH}	80	40	ns	
	10		40	20	ns	
	15		30	15	ns	
Minimum PL pulse width; HIGH	5	t_{WPLH}	100	50	ns	
	10		40	20	ns	
	15		32	16	ns	
Minimum MR pulse width; HIGH	5	t_{WMRH}	130	65	ns	
	10		50	25	ns	
	15		40	20	ns	
Hold time $P_n \rightarrow PL$	5	t_{hold}	70	35	ns	
	10		60	30	ns	
	15		50	25	ns	
Maximum clock pulse frequency $PL = LOW$	5	f_{max}	6	12	MHz	} see note
	10		12	25	MHz	
	15		16	32	MHz	

Note

In the divide-by-n mode (PL connected to TC), one has to observe the maximum HIGH to LOW propagation delay for CP to TC, before applying the next clock pulse.

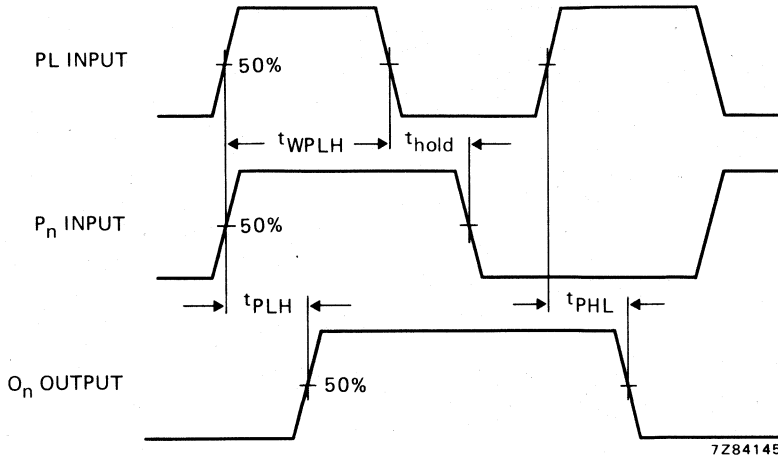


Fig. 5 Waveforms showing minimum PL pulse width, propagation delays for PL, P_n to O_n and hold time for PL to P_n .

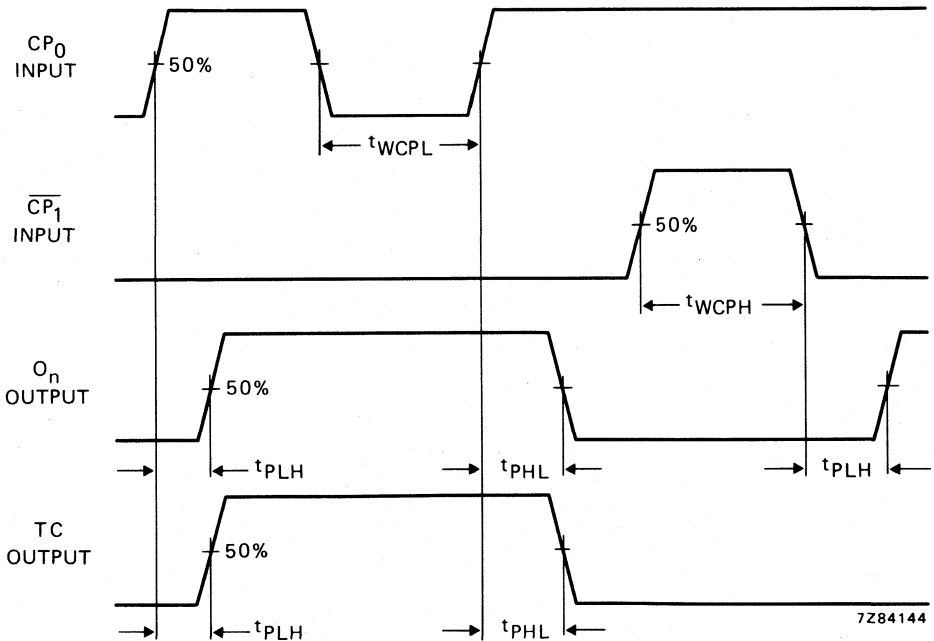


Fig. 6 Waveforms showing minimum CP_0 and \overline{CP}_1 pulse widths, propagation delays for CP_0 , \overline{CP}_1 to O_n and TC.

APPLICATION INFORMATION

Some examples of applications for the HEF4526B are:

- Divide-by-n counter
- Programmable frequency divider

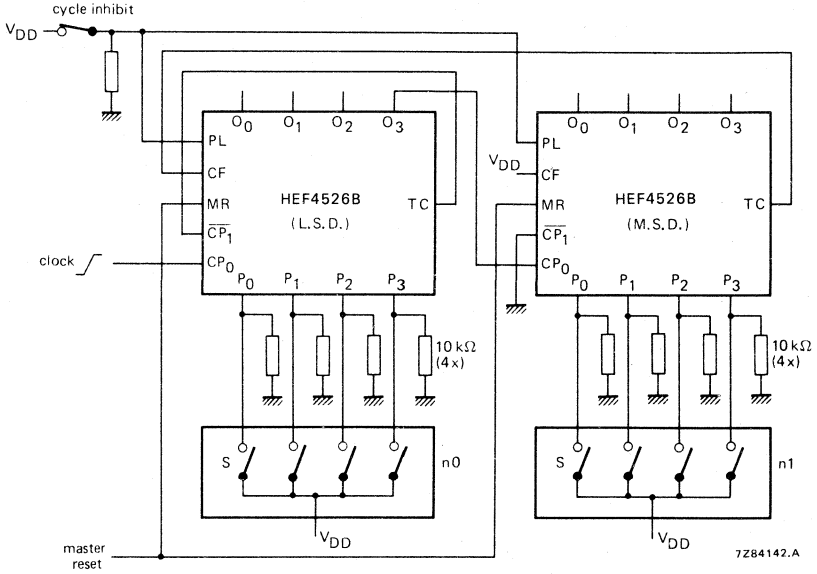
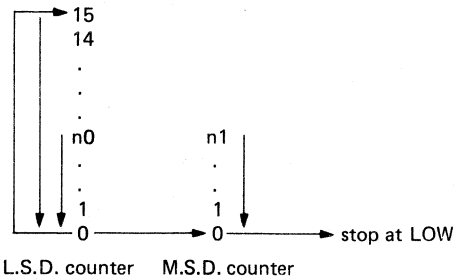


Fig. 7 Typical application of two HEF4526B circuits in a 2-stage programmable down counter (one cycle). S are thumbwheel switches; when open: LOW state.

Counting cycle:



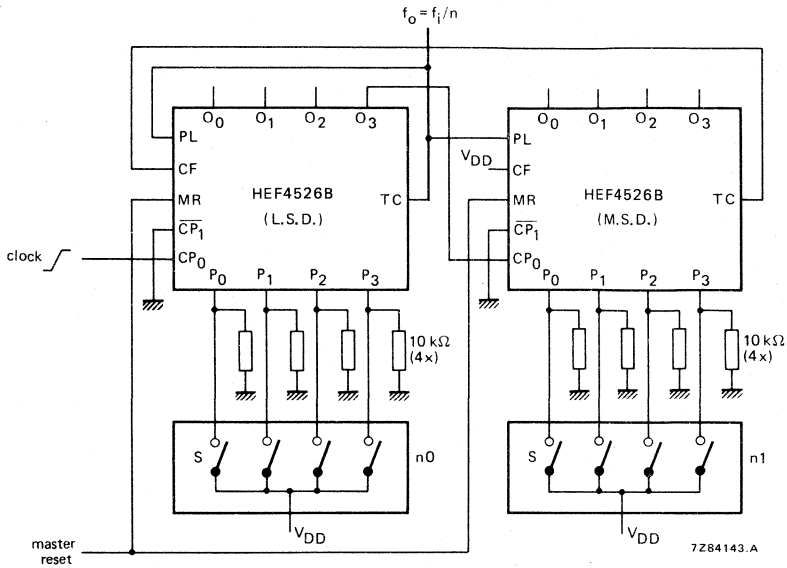
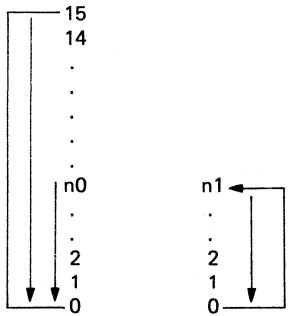


Fig. 8 Typical application of two HEF4526B circuits in a 2-stage programmable frequency divider. S are thumbwheel switches; when open: LOW state.

Counting cycle:



L.S.D. counter M.S.D. counter

DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

HEF4527B

MSI

BCD RATE MULTIPLIER

The HEF4527B is a BCD rate multiplier with two buffered rate outputs (O_1 and \bar{O}_1), two buffered terminal count outputs (TC and \bar{TC}), four BCD rate select inputs (S_A, S_B, S_C, S_D), a common clock input (CP), a preset input (PL), an overriding asynchronous clear input (CL), a strobe input (STR), a cascade input (CAS) and an active LOW count enable input (\bar{CE}).

The BCD rate multiplier provides an output pulse rate based upon the BCD input number. For example, if 6 is the BCD number, there will be six output pulses for every ten clock input pulses. The output is clocked on the negative-going transition of the clock.

When \bar{CE} , STR, CAS, CL and PL are LOW, the rate pulses are available at the outputs O_1 and \bar{O}_1 , the terminal count pulses at TC and \bar{TC} .

A HIGH on CL resets the counter, independent of all other input conditions and a rate of 10 pulses is available at O_1 and \bar{O}_1 when S_D is HIGH. When \bar{CE} is HIGH, the counter is disabled, the state of the outputs (O_1, \bar{O}_1) depend on the content of the counter.

A HIGH on PL sets the counter in the '9' state and TC becomes HIGH.

A HIGH on STR inhibits the outputs O_1 and \bar{O}_1 . A HIGH on CAS forces the output O_1 to HIGH, while the state of \bar{O}_1 depends on the inputs S_A to S_D (see lines 1 to 16 of function table).

This device may be used to perform arithmetic operations. For the add mode and multiply mode see Figs 5 and 6.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower rise and fall times.

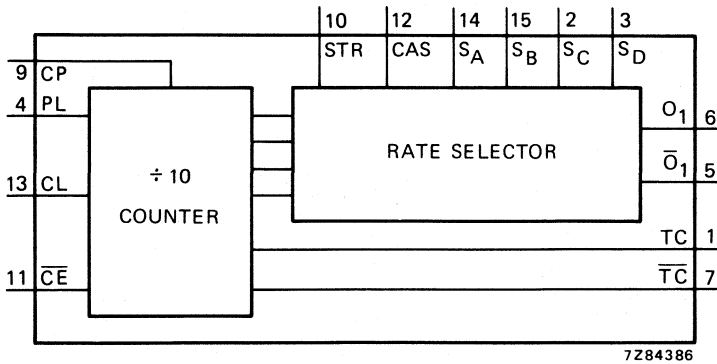


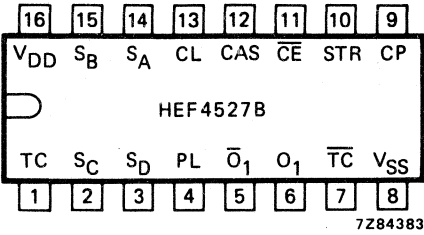
Fig. 1 Functional diagram.

FAMILY DATA

I_{DD} LIMITS category MSI

see Family Specifications

HEF4527B
MSI



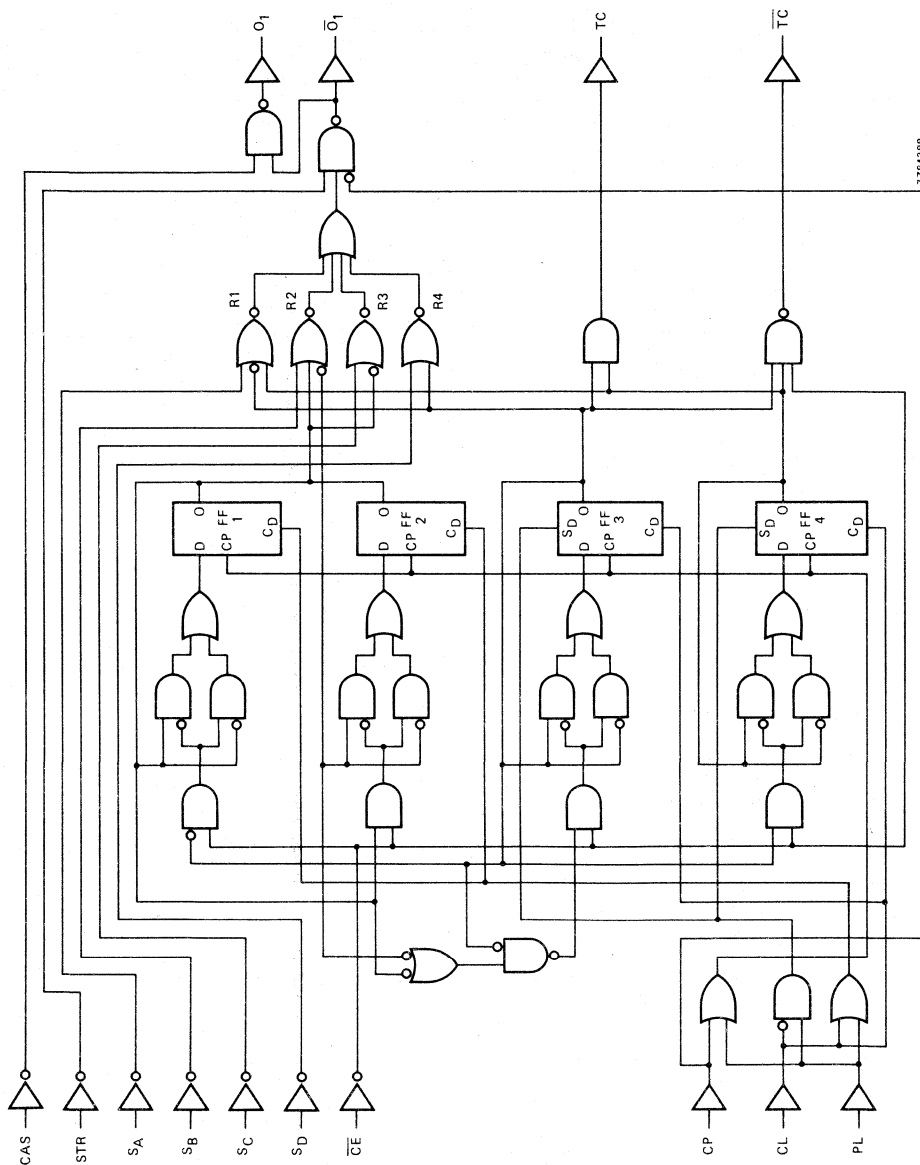
HEF4527BP : 16-lead DIL; plastic (SOT-38Z).
HEF4526BD : 16-lead DIL; ceramic (SOT-74).

Fig. 2 Pinning diagram.

PINNING

- CP clock input
- PL preset to '9' input
- CL counter clear input
- \overline{CE} count enable input (active LOW)
- STR strobe input
- CAS cascade input
- S_A to S_D rate select inputs
- O_1 to \overline{O}_1 rate outputs
- TC terminal count output (active HIGH)
- \overline{TC} terminal count output (active LOW)

DEVELOPMENT SAMPLE DATA



7264388

Fig. 3 Logic diagram.

FUNCTION TABLE

inputs										outputs				mode of operation
number of pulses or logic level										number of pulses or logic level				
S _D	S _C	S _B	S _A	CP	\overline{CE}	STR	CAS	CL	PL	O ₁	\overline{O}_1	\overline{TC}	TC	
L	L	L	L	10	L	L	L	L	L	L	H	1	1	rate pulses at the outputs depend on the BCD input number at S _A to S _D
L	L	L	H	10	L	L	L	L	L	1	1	1	1	
L	L	H	L	10	L	L	L	L	L	2	2	1	1	
L	L	H	H	10	L	L	L	L	L	3	3	1	1	
L	H	L	L	10	L	L	L	L	L	4	4	1	1	
L	H	L	H	10	L	L	L	L	L	5	5	1	1	
L	H	H	L	10	L	L	L	L	L	6	6	1	1	
L	H	H	H	10	L	L	L	L	L	7	7	1	1	
H	L	L	L	10	L	L	L	L	L	8	8	1	1	
H	L	L	H	10	L	L	L	L	L	9	9	1	1	
H	L	H	L	10	L	L	L	L	L	8	8	1	1	
H	L	H	H	10	L	L	L	L	L	9	9	1	1	
H	H	L	L	10	L	L	L	L	L	8	8	1	1	
H	H	L	H	10	L	L	L	L	L	9	9	1	1	
H	H	H	L	10	L	L	L	L	L	8	8	1	1	
H	H	H	H	10	L	L	L	L	L	9	9	1	1	
X	X	X	X	10	H	L	L	L	L	▲	▲	H	▲	$\overline{CE} = H$; counter disabled
X	X	X	X	10	L	H	L	L	L	L	H	1	1	outputs O ₁ and O ₂ disabled
X	X	X	X	10	L	L	H	L	L	H	*	1	1	output O ₁ disabled
H	X	X	X	10	L	L	L	H	X	10	10	H	L	CL = H
L	X	X	X	10	L	L	L	H	X	L	H	H	L	counter reset
X	X	X	X	10	L	L	L	L	H	L	H	L	H	PL = H; preset to '9'

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

X = state is immaterial

* Same output as the first 16 lines of this function table (depends on the values of S_A to S_D).

▲ Depends on internal state of the counter.

A.C. CHARACTERISTICS

 $V_{SS} = 0 \text{ V}$; $T_{amb} = 25 \text{ }^\circ\text{C}$; $C_L = 50 \text{ pF}$; input transition times $\leq 20 \text{ ns}$.

DEVELOPMENT SAMPLE DATA

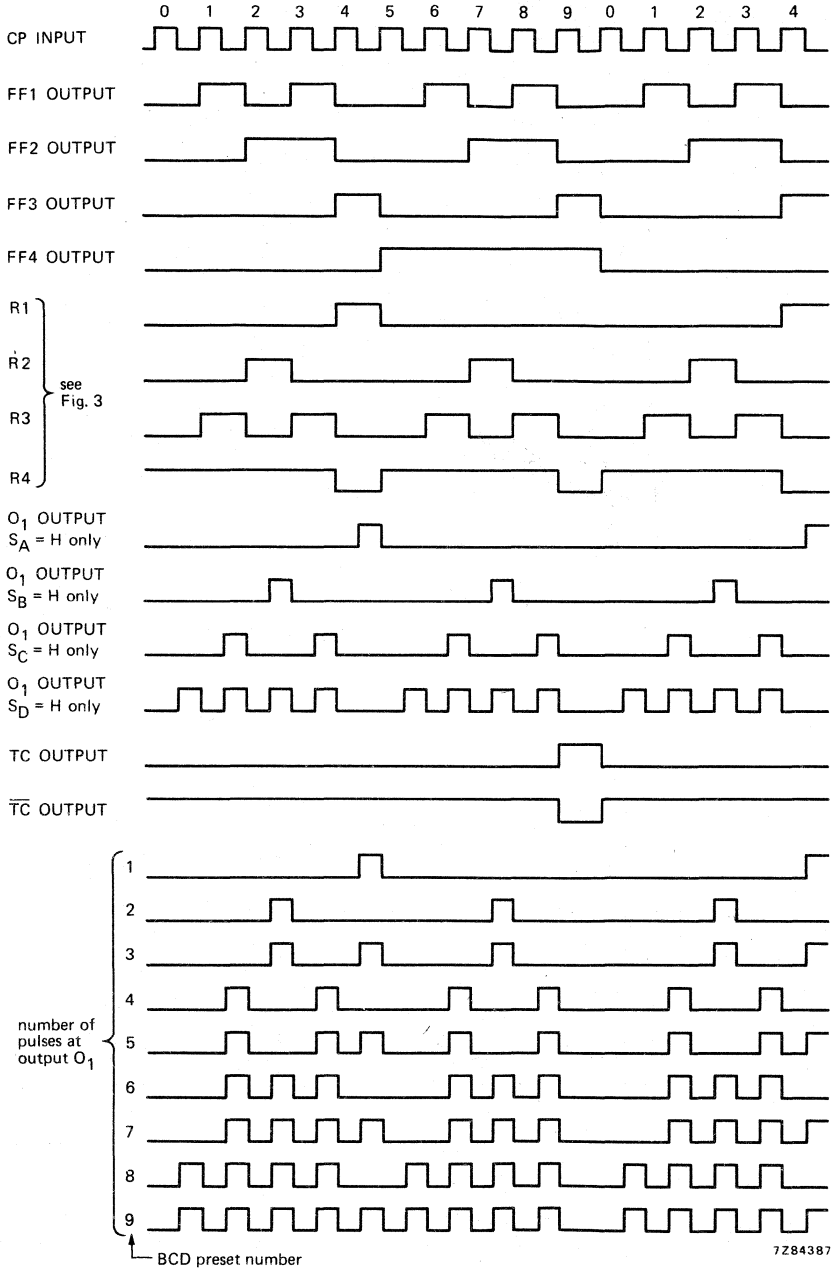
	V_{DD} V	symbol	min.	typ.	max.	typical extrapolation formula
Propagation delays CP \rightarrow O_1, \bar{O}_1 HIGH to LOW	5	t _{PHL}		125	ns	
	10		80	ns		
	15		60	ns		
LOW to HIGH	5	t _{PLH}		125	ns	
	10		80	ns		
	15		60	ns		
CP \rightarrow T_C, \bar{T}_C HIGH to LOW	5	t _{PHL}		125	ns	
	10		80	ns		
	15		60	ns		
LOW to HIGH	5	t _{PLH}		125	ns	
	10		80	ns		
	15		60	ns		
CAS \rightarrow O_1 HIGH to LOW	5	t _{PHL}		100	ns	
	10		70	ns		
	15		50	ns		
LOW to HIGH	5	t _{PLH}		100	ns	
	10		70	ns		
	15		50	ns		
STR \rightarrow O_1, \bar{O}_1 HIGH to LOW	5	t _{PHL}		100	ns	
	10		70	ns		
	15		50	ns		
LOW to HIGH	5	t _{PLH}		100	ns	
	10		70	ns		
	15		50	ns		
$\bar{C}E \rightarrow \bar{T}_C$ HIGH to LOW	5	t _{PHL}		100	ns	
	10		70	ns		
	15		50	ns		
LOW to HIGH	5	t _{PLH}		100	ns	
	10		70	ns		
	15		50	ns		
CL \rightarrow O_1, \bar{O}_1 HIGH to LOW	5	t _{PHL}		120	ns	
	10		80	ns		
	15		60	ns		
LOW to HIGH	5	t _{PLH}		120	ns	
	10		80	ns		
	15		60	ns		
PL \rightarrow O_1, \bar{O}_1 HIGH to LOW	5	t _{PHL}		125	ns	
	10		80	ns		
	15		60	ns		
LOW to HIGH	5	t _{PLH}		125	ns	
	10		80	ns		
	15		60	ns		

A.C. CHARACTERISTICS (continued)

 $V_{SS} = 0 \text{ V}$; $T_{amb} = 25 \text{ }^\circ\text{C}$; $C_L = 50 \text{ pF}$; input transition times $\leq 20 \text{ ns}$.

	V_{DD} V	symbol	min.	typ.	max.
Minimum clock pulse width	5			125	ns
	10	tWCPL		70	ns
	15			50	ns
HIGH	5			125	ns
	10	tWCPH		10	ns
	15			15	ns
Minimum CL pulse width; LOW	5			80	ns
	10	tWCLL		60	ns
	15			40	ns
Minimum PL pulse width; HIGH	5			80	ns
	10	tWPLH		60	ns
	15			40	ns
Set-up times CL \rightarrow CP	5			40	ns
	10	t _{su}		30	ns
	15			20	ns
PL \rightarrow CP	5			40	ns
	10	t _{su}		30	ns
	15			20	ns
$\overline{\text{CE}}$ \rightarrow CP	5			50	ns
	10	t _{su}		40	ns
	15			30	ns
Recovery times CL \rightarrow CP	5			40	ns
	10	t _{RCL}		30	ns
	15			20	ns
PL \rightarrow CP	5			40	ns
	10	t _{RPL}		30	ns
	15			20	ns
$\overline{\text{CE}}$ \rightarrow CP	5			50	ns
	10	t _{RCE}		40	ns
	15			30	ns
Maximum clock pulse frequency	5			4	MHz
	10	f _{max}		7	MHz
	15			10	MHz

DEVELOPMENT SAMPLE DATA



7284387

Fig. 4 Timing diagram.

APPLICATION INFORMATION
Add mode

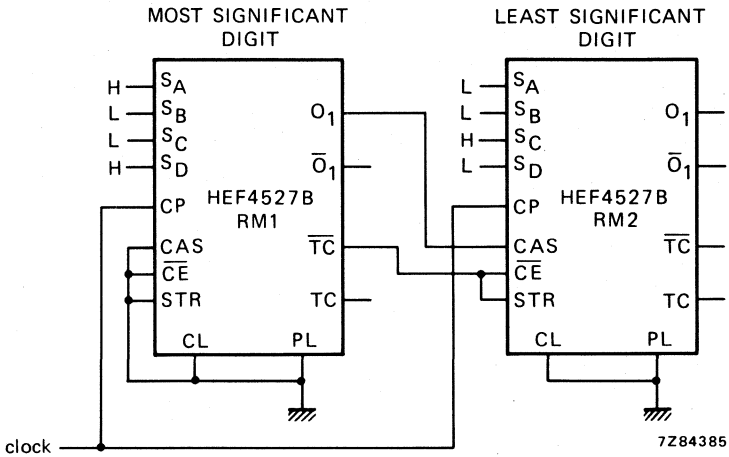


Fig. 5 Two HEF4527B cascaded in the add mode.
Output rate = $10^n (0,1 \text{ BCD}_1 + 0,01 \text{ BCD}_2 + 0,01 \text{ BCD}_3 + \dots)$, in where n = number of cascaded RMs. Example: RM1 preset to 9 and RM2 preset to 4, output rate is $10^2 (0,1 \times 9 \times 0,01 \times 4) = 94$.

Multiply mode

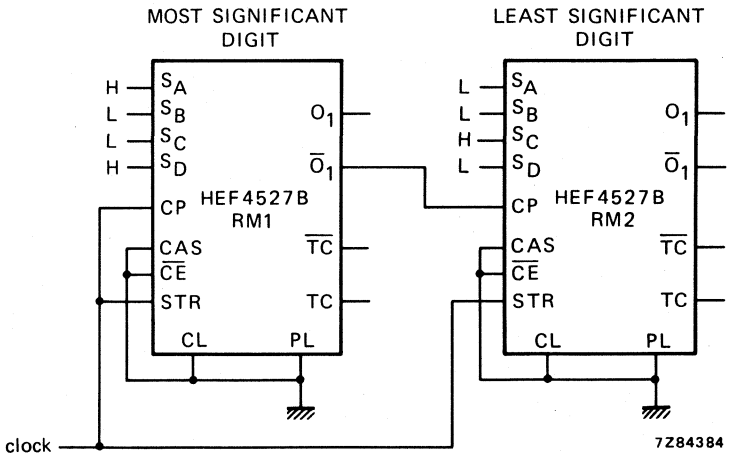


Fig. 6 Two HEF4527B cascaded in the multiply mode.
Output rate = $10^n (0,1 \text{ BCD}_1 \times 0,1 \text{ BCD}_2 \times 0,1 \text{ BCD}_3 \times \dots)$, in where n = number of cascaded RMs. Example: RM1 preset to 9 and RM2 preset to 4, output rate is $10^2 (0,1 \times 9 \times 0,1 \times 4) = 36$.

DUAL MONOSTABLE MULTIVIBRATOR



The HEF4528B is a dual retriggerable-resettable monostable multivibrator. Each multivibrator has an active LOW input (\bar{I}_0), and active HIGH input (I_1), an active LOW clear direct input (\bar{C}_D), an output (O) and its complement (\bar{O}), and two pins for connecting the external timing components (C_{TC} , RC_{TC}).

An external timing capacitor (C_T) must be connected between C_{TC} and RC_{TC} and an external resistor (R_T) must be connected between RC_{TC} and V_{DD} . The duration of the output pulse is determined by the external timing components C_T and R_T .

A HIGH to LOW transition on \bar{I}_0 when I_1 is LOW or a LOW to HIGH transition on I_1 when \bar{I}_0 is HIGH produces a positive pulse (LOW-HIGH-LOW) on O and a negative pulse (HIGH-LOW-HIGH) on \bar{O} if the \bar{C}_D is HIGH. A LOW on \bar{C}_D forces O LOW, \bar{O} HIGH and inhibits any further pulses until \bar{C}_D is HIGH.

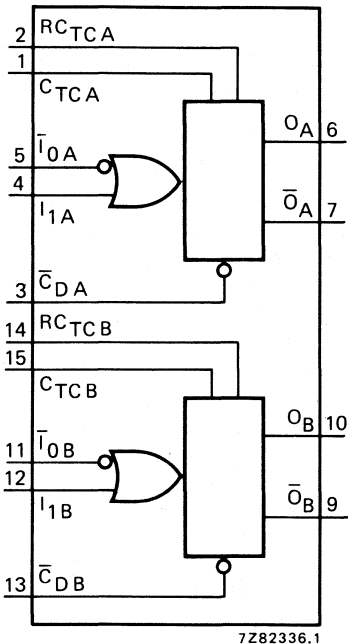


Fig. 1 Functional diagram.

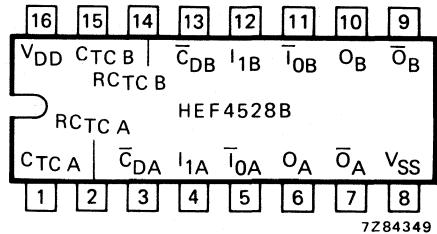


Fig. 2 Pinning diagram.

HEF4528BP: 16-lead DIL; plastic (SOT-38Z).

HEF4528BD: 16-lead DIL; ceramic (SOT-74).

HEF4528BT: 16-lead flat pack; plastic (SO-16; SOT-109A)

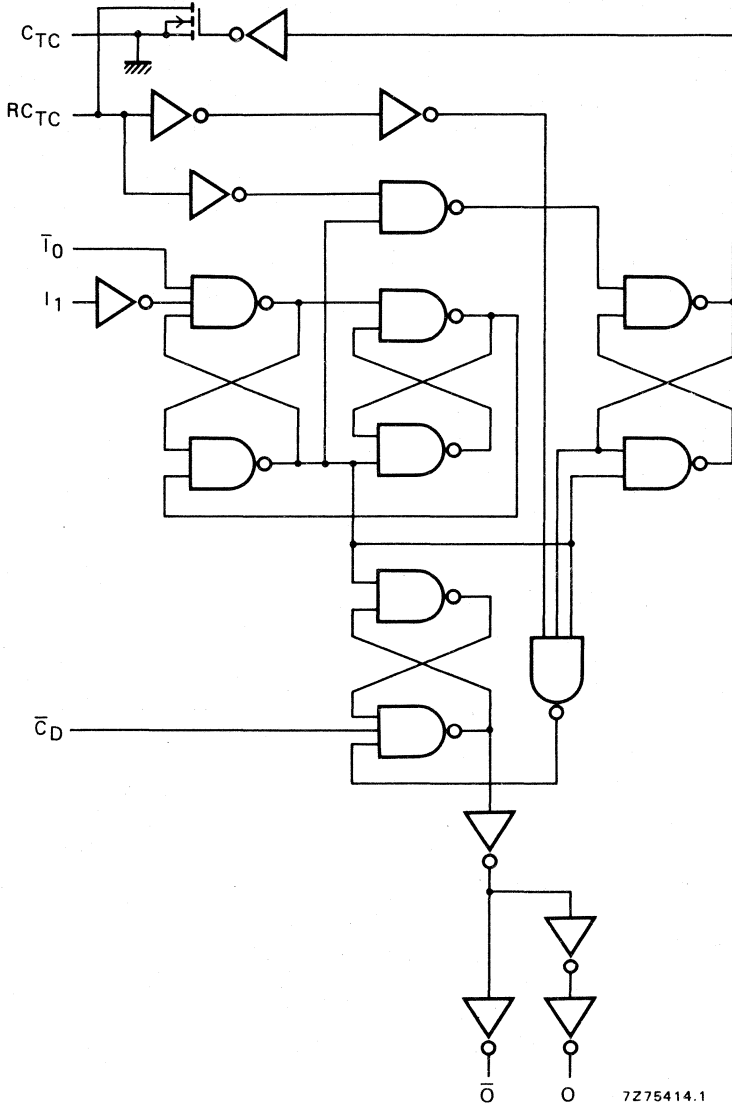
PINNING

- $\bar{I}_{0A}, \bar{I}_{0B}$ input (HIGH to LOW triggered)
- I_{1A}, I_{1B} input (LOW to HIGH triggered)
- $\bar{C}_{DA}, \bar{C}_{DB}$ clear direct input (active LOW)
- O_A, O_B output
- \bar{O}_A, \bar{O}_B complementary output (active LOW)
- C_{TCA}, C_{TCB} external capacitor connections
- RC_{TCA}, RC_{TCB} external capacitor/resistor connections

FAMILY DATA

I_{DD} LIMITS category MSI

} see Family Specifications



7275414.1

Fig. 3 Logic diagram (one monostable multivibrator).

FUNCTION TABLE

inputs			outputs	
$\overline{T_0}$	I_1	$\overline{C_D}$	O	\overline{O}
\downarrow	L	H	\uparrow	\downarrow
H	\downarrow	H	\uparrow	\downarrow
X	X	L	L	H

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

X = state is immaterial

 \downarrow = positive-going transition \uparrow = negative-going transition $\uparrow\downarrow$ = positive or negative output pulse; width is determined by C_t and R_t

A.C. CHARACTERISTICS

 $V_{SS} = 0$ V; $T_{amb} = 25$ °C; $C_L = 50$ pF; input transition times ≤ 20 ns

	V_{DD} V	symbol	min.	typ.	max.	typical extrapolation formula	
Propagation delays $\overline{T_0}, I_1 \rightarrow \overline{O}$ HIGH to LOW	5	tPHL		140	280	ns	113 ns + (0,55 ns/pF) C_L
	10			50	100	ns	39 ns + (0,23 ns/pF) C_L
	15			35	70	ns	27 ns + (0,16 ns/pF) C_L
$\overline{T_0}, I_1 \rightarrow O$ LOW to HIGH	5	tPLH		155	305	ns	128 ns + (0,55 ns/pF) C_L
	10			60	115	ns	49 ns + (0,23 ns/pF) C_L
	15			40	80	ns	32 ns + (0,16 ns/pF) C_L
$\overline{C_D} \rightarrow O$ HIGH to LOW	5	tPHL		105	210	ns	78 ns + (0,55 ns/pF) C_L
	10			40	85	ns	29 ns + (0,23 ns/pF) C_L
	15			30	60	ns	22 ns + (0,16 ns/pF) C_L
$\overline{C_D} \rightarrow \overline{O}$ LOW to HIGH	5	tPLH		120	240	ns	93 ns + (0,55 ns/pF) C_L
	10			50	105	ns	39 ns + (0,23 ns/pF) C_L
	15			35	70	ns	27 ns + (0,16 ns/pF) C_L
Output transition times HIGH to LOW	5	tTHL		60	120	ns	10 ns + (1,0 ns/pF) C_L
	10			30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
LOW to HIGH	5	tTLH		60	120	ns	10 ns + (1,0 ns/pF) C_L
	10			30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L

A.C. CHARACTERISTICS

 $V_{SS} = 0$ V; $T_{amb} = 25$ °C; input transition times ≤ 20 ns; $R_t = 5$ k Ω ; $C_t = 15$ pF

	V_{DD} V	typical formula for P (μ W)	where
Dynamic power dissipation per package (P)	5	$4000 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz)
	10	$20\,000 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_o = output freq. (MHz)
	15	$59\,000 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	C_L = load capacitance (pF)
			$\Sigma(f_o C_L)$ = sum of outputs
			V_{DD} = supply voltage (V)

A.C. CHARACTERISTICS

$V_{SS} = 0 \text{ V}$; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$; $C_L = 50 \text{ pF}$; input transition times $\leq 20 \text{ ns}$; see also waveforms Fig. 5.

	V_{DD} V	symbol	min.	typ.	max.		
Recovery time for \bar{C}_D	5	t_{RCD}	0	-75	ns		
	10		0	-30	ns		
	15		0	-25	ns		
Minimum \bar{I}_O pulse width; LOW	5	t_{WIOL}	50	25	ns		
	10		30	15	ns		
	15		20	10	ns		
Minimum I_1 pulse width; HIGH	5	t_{WI1H}	50	25	ns		
	10		30	15	ns		
	15		20	10	ns		
Minimum \bar{C}_D pulse width; LOW	5	t_{WCDL}	60	30	ns		
	10		35	15	ns		
	15		25	10	ns		
Set-up time $\bar{C}_D \rightarrow \bar{I}_O$ or I_1	5	t_{su}	0	-105	ns		} to avoid change in output
	10		0	-40	ns		
	15		0	-25	ns		
Output O pulse width; HIGH	5	t_{WOH}	-	235	ns	} note 1	
	10		-	155	ns		
	15		-	140	ns		
Output O pulse width; HIGH	5	t_{WOH}	-	5,45	μs	} note 2	
	10		-	4,95	μs		
	15		-	4,85	μs		
Change in output O pulse width over temperature	5	Δt_{WO}	-	± 3	%	} note 3	
	10		-	± 2	%		
	15		-	± 2	%		
Change in output O pulse width over V_{DD}	5	Δt_{WO}	-	± 2	%	} $V_{DD} \pm 5\%$	
	10		-	± 1	%		
	15		-	± 1	%		
External timing resistor	5	R_t	5	-	2000 k Ω		
	10		5	-	2000 k Ω		
	15		5	-	2000 k Ω		
External timing capacitor	5	C_t	no limits				
	10		no limits				
	15		no limits				

Notes

- $R_t = 5 \text{ k}\Omega$; $C_t = 15 \text{ pF}$; for other R_t , C_t combinations and $C_t < 0,01 \mu\text{F}$ see graph Fig. 4.
- $R_t = 10 \text{ k}\Omega$; $C_t = 1000 \text{ pF}$; for other R_t , C_t combinations and $C_t > 0,01 \mu\text{F}$ use formula $t_{\text{WO}} = K \cdot R_t \cdot C_t$.

where: t_{WO} = output pulse width (s)

R_t = external timing resistor (Ω)

C_t = external timing capacitor (F)

$K = 0,42$ for $V_{DD} = 5 \text{ V}$

$K = 0,32$ for $V_{DD} = 10 \text{ V}$

$K = 0,30$ for $V_{DD} = 15 \text{ V}$

- $T_{\text{amb}} = -40$ to $+85 \text{ }^\circ\text{C}$; Δt_{WO} is referenced to t_{WO} at $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$.

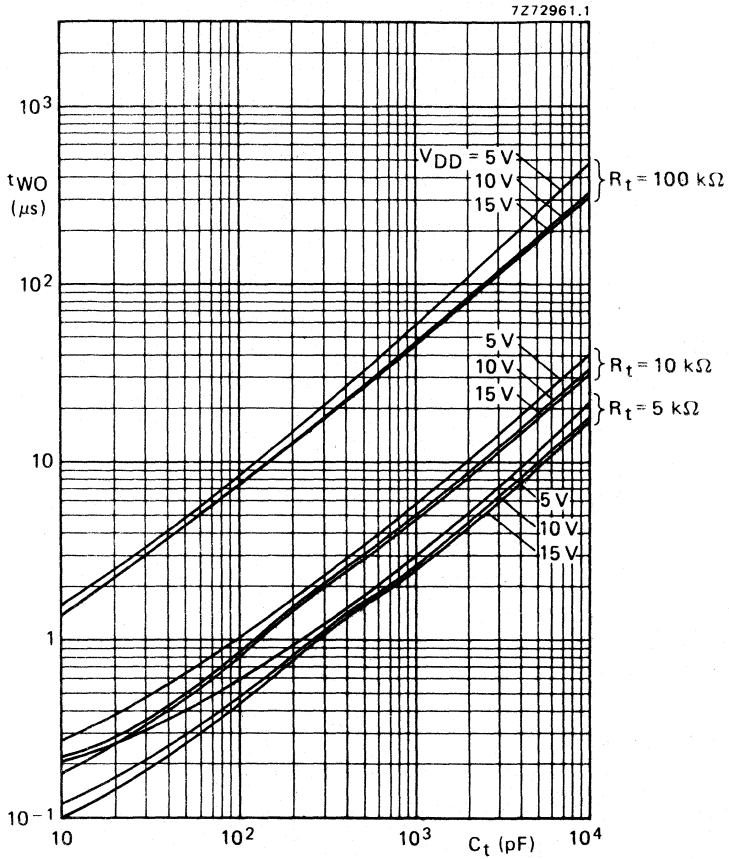
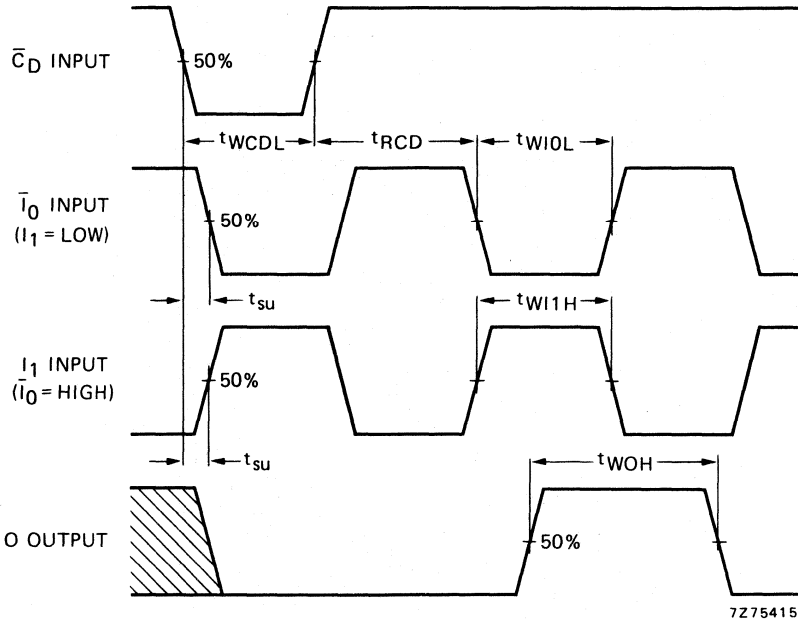


Fig. 4 Output pulse width (t_{WO}) as a function of external timing capacitor (C_t).





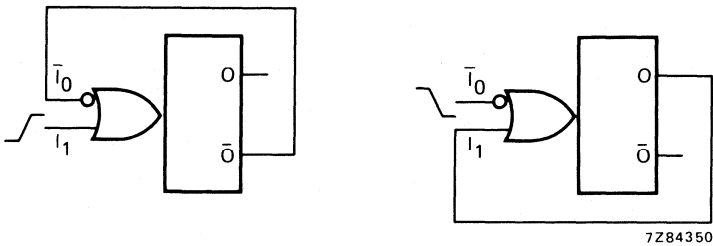
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Fig. 5 Waveforms showing minimum \bar{I}_0 , I_1 and O pulse widths, set-up and recovery times. Set-up and recovery times are shown as positive values but may be specified as negative values.

APPLICATION INFORMATION

An example of an application for the HEF4528B is:

- Non-retriggerable monostable multivibrator



7Z84350

Fig. 6 Two examples for a non-retriggerable monostable multivibrator using half of HEF4528B (LOW to HIGH and HIGH to LOW triggered).

13-INPUT PARITY CHECKER/GENERATOR



The HEF4531B is a parity checker/generator with 13 parity inputs (I_0 to I_{12}) and a parity output (O). When the number of parity inputs that are HIGH is even, the output is LOW. When the number of parity inputs that are HIGH is odd, the output is HIGH. For words of 12 bits or less, the output can be used to generate either odd or even parity by appropriate termination of the unused parity input(s). For words of 14 or more bits, the devices can be cascaded by connecting the output of one device to any parity input of another device. When cascading devices, it is recommended that the output of one device be connected to the I_{12} input of the other device since there is less delay to the output from the I_{12} input than from any other input (I_0 to I_{11}).

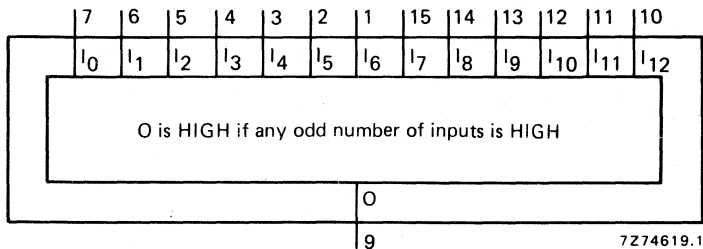


Fig. 1 Functional diagram.

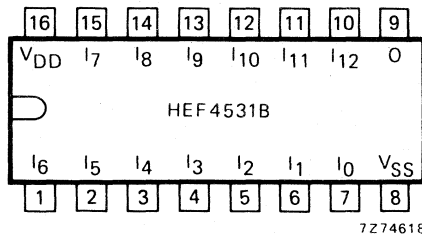


Fig. 2 Pinning diagram.

HEF4531BP: 16-lead DIL; plastic (SOT-38Z).

HEF4531BD: 16-lead DIL; ceramic (SOT-74).

HEF4531BT: 16-lead flat pack; plastic
(SO-16; SOT-109A).

FAMILY DATA

IDD LIMITS category MSI

} see Family Specifications



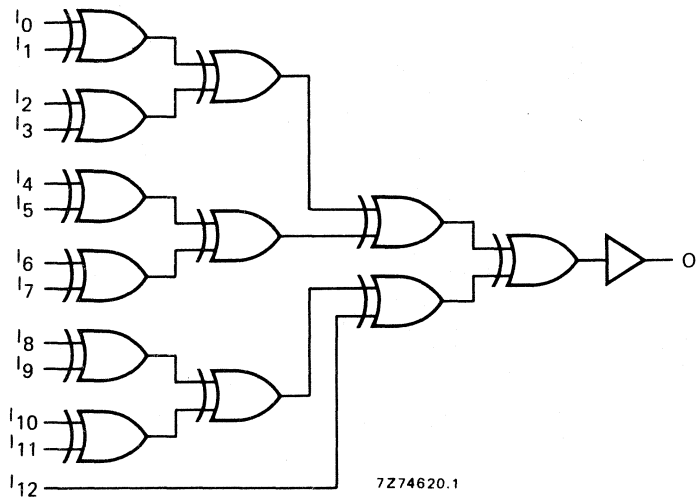


Fig. 3 Logic diagram.

FUNCTION TABLE

inputs												output	
I ₀	I ₁	I ₂	I ₃	I ₄	I ₅	I ₆	I ₇	I ₈	I ₉	I ₁₀	I ₁₁	I ₁₂	O
L	L	L	L	L	L	L	L	L	L	L	L	L	L
any odd number of inputs HIGH												H	
any even number of inputs HIGH												L	
H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ≤ 20 ns

	V _{DD} V	typical formula for P (μW)	where f _i = input freq. (MHz) f _o = output freq. (MHz) C _L = load capacitance (pF) Σ(f _o C _L) = sum of outputs V _{DD} = supply voltage (V)
Dynamic power dissipation per package (P)	5	425 f _i + Σ(f _o C _L) × V _{DD} ²	
	10	2 400 f _i + Σ(f _o C _L) × V _{DD} ²	
	15	7 700 f _i + Σ(f _o C _L) × V _{DD} ²	

A.C. CHARACTERISTICS

$V_{SS} = 0 \text{ V}$; $T_{amb} = 25 \text{ }^\circ\text{C}$; $C_L = 50 \text{ pF}$; input transition times $\leq 20 \text{ ns}$

	V_{DD} V	symbol	typ. max.			typical extrapolation formula
			typ.	max.		
Propagation delays I_0 to $I_{11} \rightarrow O$ HIGH to LOW	5	t _{PHL}	145	290	ns	118 ns + (0,55 ns/pF) C_L
	10		60	120	ns	49 ns + (0,23 ns/pF) C_L
	15		45	90	ns	37 ns + (0,16 ns/pF) C_L
LOW to HIGH	5	t _{PLH}	135	270	ns	108 ns + (0,55 ns/pF) C_L
	10		55	110	ns	44 ns + (0,23 ns/pF) C_L
	15		45	90	ns	37 ns + (0,16 ns/pF) C_L
$I_{12} \rightarrow O$ HIGH to LOW	5	t _{PHL}	105	210	ns	78 ns + (0,55 ns/pF) C_L
	10		45	90	ns	34 ns + (0,23 ns/pF) C_L
	15		35	70	ns	27 ns + (0,16 ns/pF) C_L
LOW to HIGH	5	t _{PLH}	85	170	ns	58 ns + (0,55 ns/pF) C_L
	10		35	70	ns	24 ns + (0,23 ns/pF) C_L
	15		25	50	ns	17 ns + (0,16 ns/pF) C_L
Output transition times HIGH to LOW	5	t _{THL}	60	120	ns	10 ns + (1,0 ns/pF) C_L
	10		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L
LOW to HIGH	5	t _{TLH}	60	120	ns	10 ns + (1,0 ns/pF) C_L
	10		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L

8-INPUT PRIORITY ENCODER



The HEF4532B is an 8-input priority encoder with eight active HIGH priority inputs (I_0 to I_7), three active HIGH outputs (O_0 to O_2), an active HIGH enable input (E_{in}), an active HIGH enable output (E_{out}) and an active HIGH group select output (GS).

Data is accepted on inputs I_0 to I_7 . The binary code corresponding to the highest priority input (I_0 to I_7) which is HIGH, is generated on O_0 to O_2 if E_{in} is HIGH. Input I_7 is assigned the highest priority. GS is HIGH when one or more priority inputs and E_{in} are HIGH. E_{out} is HIGH when I_0 to I_7 are LOW and E_{in} is HIGH. E_{in} , when LOW, forces all outputs (O_0 to O_2 , GS, E_{out}) LOW.

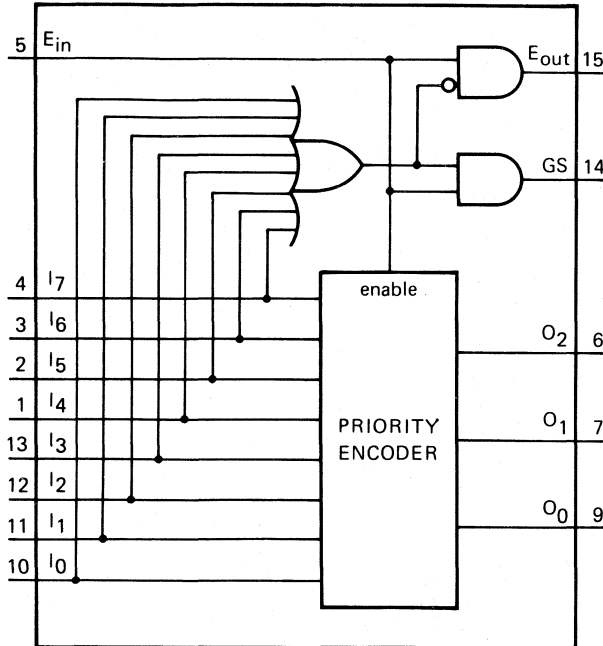
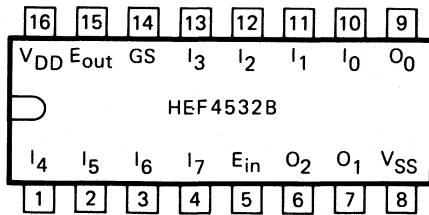


Fig. 1 Functional diagram.

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Fig. 2 Pinning diagram.

HEF4532BP: 16-lead DIL; plastic (SOT-38Z).

HEF4532BD: 16-lead DIL; ceramic (SOT-74).

HEF4532BT: 16-lead flat pack; plastic (SO-16; SOT-109A).

PINNING

I_0 to I_7 priority inputs
 E_{in} enable input
 E_{out} enable output
 GS group select output
 O_0 to O_2 outputs

FAMILY DATA

 I_{DD} LIMITS category MSI

see Family Specifications

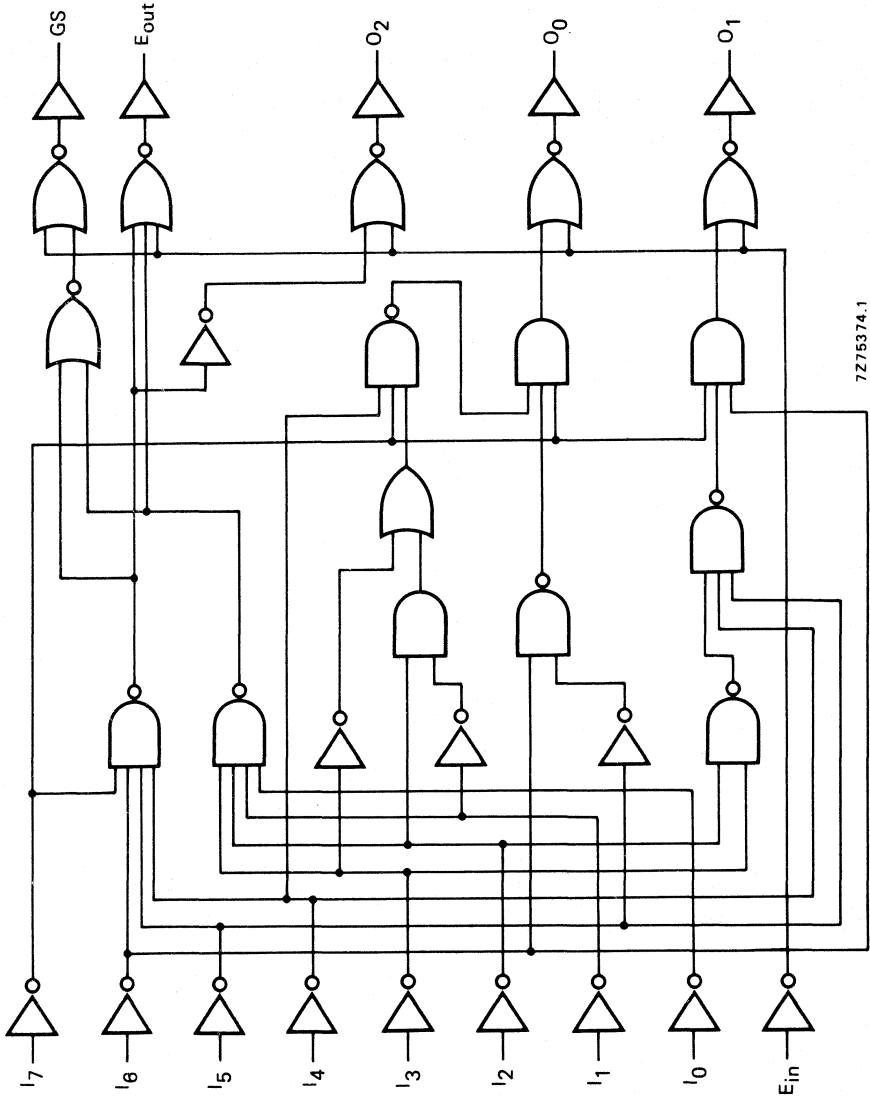


Fig. 3 Logic diagram.

TRUTH TABLE

inputs									outputs				
E _{in}	I ₇	I ₆	I ₅	I ₄	I ₃	I ₂	I ₁	I ₀	GS	O ₂	O ₁	O ₀	E _{out}
L	X	X	X	X	X	X	X	X	L	L	L	L	L
H	L	L	L	L	L	L	L	L	L	L	L	L	H
H	H	X	X	X	X	X	X	X	H	H	H	H	L
H	L	H	X	X	X	X	X	X	H	H	H	L	L
H	L	L	X	X	X	X	X	X	H	H	L	H	L
H	L	L	L	H	X	X	X	X	H	H	L	L	L
H	L	L	L	L	H	X	X	X	H	L	H	H	L
H	L	L	L	L	L	H	X	X	H	L	H	L	L
H	L	L	L	L	L	L	H	X	H	L	L	H	L
H	L	L	L	L	L	L	L	H	H	L	L	L	L

H = HIGH state (the more positive voltage)
 L = LOW state (the less positive voltage)
 X = state is immaterial

LOGIC EQUATIONS

$$O_2 = E_{in} \cdot (I_4 + I_5 + I_6 + I_7)$$

$$O_1 = E_{in} \cdot (I_2 \cdot \bar{I}_4 \cdot \bar{I}_5 + I_3 \cdot \bar{I}_4 \cdot \bar{I}_5 + I_6 + I_7)$$

$$O_0 = E_{in} \cdot (I_1 \cdot \bar{I}_2 \cdot \bar{I}_4 \cdot \bar{I}_6 + I_3 \cdot \bar{I}_4 \cdot \bar{I}_6 + I_5 \cdot \bar{I}_6 + I_7)$$

$$E_{out} = E_{in} \cdot \bar{I}_0 \cdot \bar{I}_1 \cdot \bar{I}_2 \cdot \bar{I}_3 \cdot \bar{I}_4 \cdot \bar{I}_5 \cdot \bar{I}_6 \cdot \bar{I}_7$$

$$GS = E_{in} \cdot (I_0 + I_1 + I_2 + I_3 + I_4 + I_5 + I_6 + I_7)$$

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ≤ 20 ns

	V _{DD} V	typical formula for P (μW)	where f _i = input freq. (MHz) f _o = output freq. (MHz) C _L = load capacitance (pF) Σ(f _o C _L) = sum of outputs V _{DD} = supply voltage (V)
Dynamic power dissipation per package (P)	5 10 15	1 620 f _i + Σ(f _o C _L) × V _{DD} ² 6 600 f _i + Σ(f _o C _L) × V _{DD} ² 15 970 f _i + Σ(f _o C _L) × V _{DD} ²	

A.C. CHARACTERISTICS

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$; see also waveforms Fig. 4

	V_{DD} V	symbol	min.	typ.	max.	typical extrapolation formula	
Propagation delays $E_{in} \rightarrow E_{out}$ HIGH to LOW	5	tPHL		95	190	ns	$68\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10		45	90	ns	$34\text{ ns} + (0,23\text{ ns/pF}) C_L$	
	15		35	70	ns	$27\text{ ns} + (0,16\text{ ns/pF}) C_L$	
LOW to HIGH	5	tPLH		80	160	ns	$53\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10		35	70	ns	$24\text{ ns} + (0,23\text{ ns/pF}) C_L$	
	15		30	60	ns	$22\text{ ns} + (0,16\text{ ns/pF}) C_L$	
$E_{in} \rightarrow GS$ HIGH to LOW	5	tPHL		85	170	ns	$58\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10		45	90	ns	$34\text{ ns} + (0,23\text{ ns/pF}) C_L$	
	15		35	70	ns	$27\text{ ns} + (0,16\text{ ns/pF}) C_L$	
LOW to HIGH	5	tPLH		80	160	ns	$53\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10		40	80	ns	$29\text{ ns} + (0,23\text{ ns/pF}) C_L$	
	15		30	60	ns	$22\text{ ns} + (0,16\text{ ns/pF}) C_L$	
$E_{in} \rightarrow O_n$ HIGH to LOW	5	tPHL		80	160	ns	$53\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10		40	80	ns	$29\text{ ns} + (0,23\text{ ns/pF}) C_L$	
	15		30	60	ns	$22\text{ ns} + (0,16\text{ ns/pF}) C_L$	
LOW to HIGH	5	tPLH		85	170	ns	$58\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10		40	80	ns	$29\text{ ns} + (0,23\text{ ns/pF}) C_L$	
	15		30	60	ns	$22\text{ ns} + (0,16\text{ ns/pF}) C_L$	
$I_n \rightarrow O_n$ HIGH to LOW	5	tPHL		115	230	ns	$88\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10		50	100	ns	$39\text{ ns} + (0,23\text{ ns/pF}) C_L$	
	15		35	70	ns	$27\text{ ns} + (0,16\text{ ns/pF}) C_L$	
LOW to HIGH	5	tPLH		115	230	ns	$88\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10		50	100	ns	$39\text{ ns} + (0,23\text{ ns/pF}) C_L$	
	15		35	70	ns	$27\text{ ns} + (0,16\text{ ns/pF}) C_L$	
$I_n \rightarrow GS$ HIGH to LOW	5	tPHL		115	230	ns	$88\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10		50	100	ns	$39\text{ ns} + (0,23\text{ ns/pF}) C_L$	
	15		40	80	ns	$32\text{ ns} + (0,16\text{ ns/pF}) C_L$	
LOW to HIGH	5	tPLH		115	230	ns	$88\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10		50	100	ns	$39\text{ ns} + (0,23\text{ ns/pF}) C_L$	
	15		40	80	ns	$32\text{ ns} + (0,16\text{ ns/pF}) C_L$	
Output transition times HIGH to LOW	5	tTHL		60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$
	10		30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$	
	15		20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$	
LOW to HIGH	5	tTLH		60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$
	10		30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$	
	15		20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$	

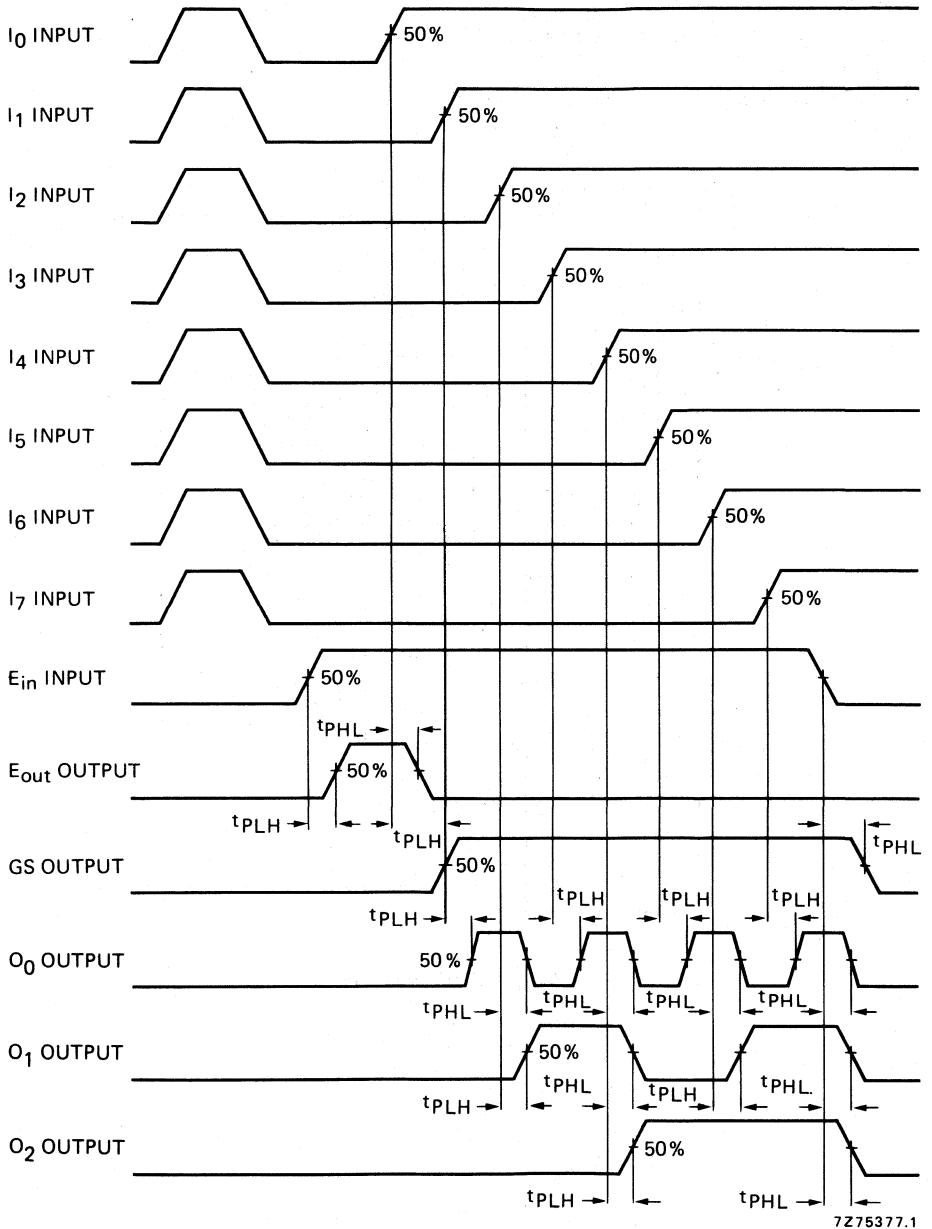


Fig. 4 Waveforms showing propagation delays from inputs to outputs.

APPLICATION INFORMATION

Some examples of applications for the HEF4532B are:

- Priority encoder
- Keyboard encoder

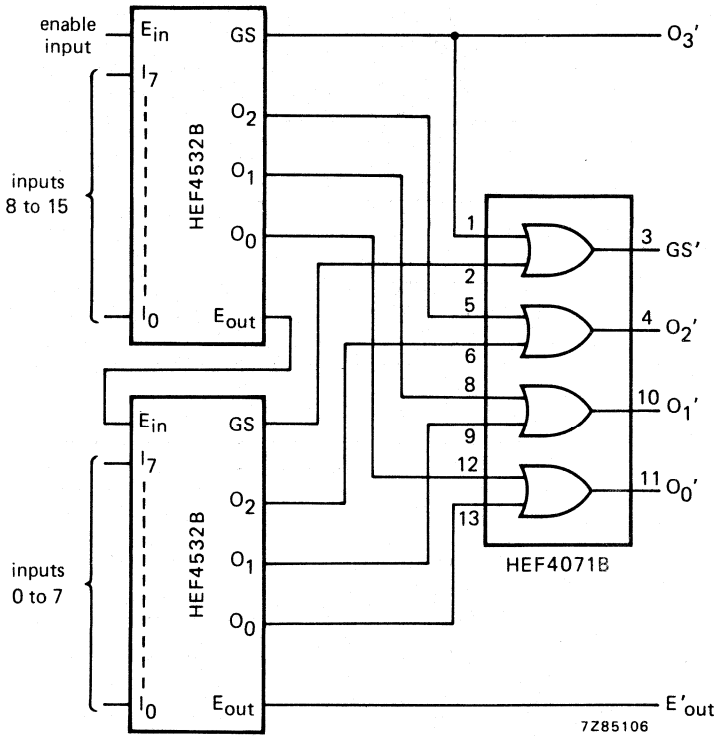
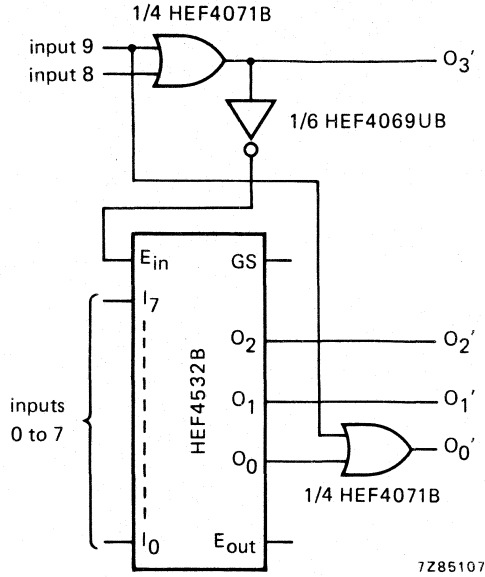


Fig. 5 16-level priority encoder.



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Fig. 6 0-to-9 keyboard encoder.

TRUTH TABLE (for Fig. 6)

inputs										outputs				
9	8	7	6	5	4	3	2	1	0	GS	O ₃ '	O ₂ '	O ₁ '	O ₀ '
H	X	X	X	X	X	X	X	X	X	L	H	L	L	H
L	H	X	X	X	X	X	X	X	X	L	H	L	L	L
L	L	H	X	X	X	X	X	X	X	H	L	H	H	H
L	L	L	H	X	X	X	X	X	X	H	L	H	H	L
L	L	L	L	H	X	X	X	X	X	H	L	H	L	L
L	L	L	L	L	H	X	X	X	X	H	L	L	H	H
L	L	L	L	L	L	H	X	X	X	H	L	L	L	L
L	L	L	L	L	L	L	H	X	X	H	L	L	L	L
L	L	L	L	L	L	L	L	H	H	H	L	L	L	L

H = HIGH state (the more positive voltage)
 L = LOW state (the less positive voltage)
 X = state is immaterial

REAL TIME 5-DECADE COUNTER

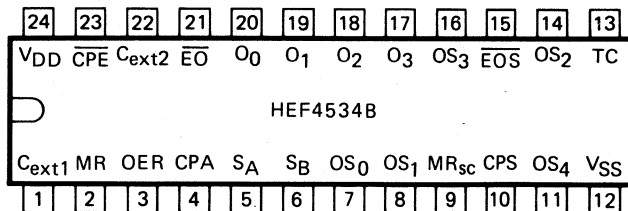


The HEF4534B is a 5-decade ripple counter. The binary outputs of the decade counters are time-multiplexed by an internal scanner on four BCD outputs (O_0 to O_3). The selected decade is indicated by a logic HIGH on the appropriate digit select output (OS_0 : units, 1; OS_1 : tens, 10; OS_2 : hundreds, 10^2 ; OS_3 : thousands, 10^3 ; OS_4 : ten thousands, 10^4).

The binary outputs (O_0 to O_3) and the select outputs (OS_0 to OS_4) are 3-state controlled via enable inputs \overline{EO} and \overline{EOS} respectively, allowing interface with other bus orientated devices. Cascading may be accomplished by using the carry out (TC). The counter is triggered by a LOW to HIGH transition on the decade clock (CPA) and is reset by a HIGH level on the master reset (MR). The scanner is triggered by a LOW to HIGH transition on the scanner clock (CPS) and is reset (select ten thousand counter) by a HIGH level on the scanner reset (MR_{sc}).

The counter can operate in four modes depending on the state of the mode select inputs (S_A , S_B). The error detector will detect an error when a positive edge on CPA is not accompanied by a negative edge on the error detector clock \overline{CPE} or vice versa, within time limits adjusted by external capacitors connected to C_{ext1} and C_{ext2} . Three or more detected errors result in a HIGH level on the error output (OER). The error detector is reset by a HIGH level on MR.

Schmitt-trigger action in the clock inputs makes the circuit highly tolerant to slower clock rise and fall times.



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Fig. 1 Pinning diagram.

HEF4534BP: 24-lead DIL; plastic (SOT-101A).

HEF4534BD: 24-lead DIL; ceramic (SOT-94).

PINNING

O_1 to O_3	BCD outputs	\overline{CPE}	error detector clock input
OS_0 to OS_3	digit select outputs	S_A , S_B	mode select inputs
OER	error output	MR	master reset input
CPA	decade clock input	MR_{sc}	scanner reset input
CPS	scanner clock input	TC	carry out

FAMILY DATA

I_{DD} LIMITS category LSI

} see Family Specifications

MODE CONTROL FUNCTION TABLE

select inputs		1st decade output	carry to 2nd stage	carry to 4th stage	mode
S _A	S _B				
L	L	normal count and display	at 9 to 0 transition of the 1st decade	at 9 to 0 transition of the 3rd decade	5-decade counter
L	H	inhibited	input clock	input clock	test purposes: clock directly into stages 1, 2 and 4
H	H	inhibited	at 4 to 5 transition of the 1st decade	at 9 to 0 transition of the 3rd decade	4-decade counter with ÷10 and round-off at front end
H	L	display counts: 3, 4, 5, 6, 7 = 5 8, 9, 0, 1, 2 = 0	at 7 to 8 transition of the 1st decade	at 9 to 0 transition of the 3rd decade	4-decade counter; ½-pence capability

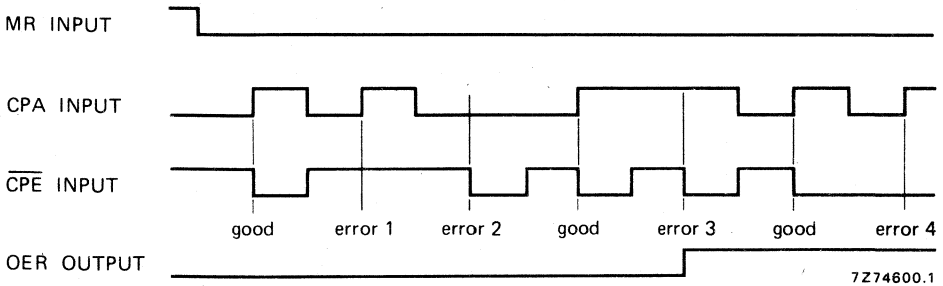


Fig. 3 Error detection timing diagram.

The skew time is the time difference between the LOW to HIGH transition of CPA and the HIGH to LOW transition of CPE or vice versa (see Fig. 4). The skew time is typically proportional to the external capacitor (C_{ext}) connected from C_{ext1} and C_{ext2} (pins 1 and 22) to V_{SS} . The error detector will count an error when a positive edge on the counter clock CPA is not succeeded by a negative edge on the error detector clock CPE within a skew time t_{SK1} (adjustable by C_{ext1} at pin 1). The same holds for a negative edge at CPE succeeded by a positive on CPA within a skew time t_{SK2} (adjustable by C_{ext2} at pin 22). If error detection is not needed, CPE must be either HIGH or LOW and no C_{ext} is applied. For further information see Fig. 5.

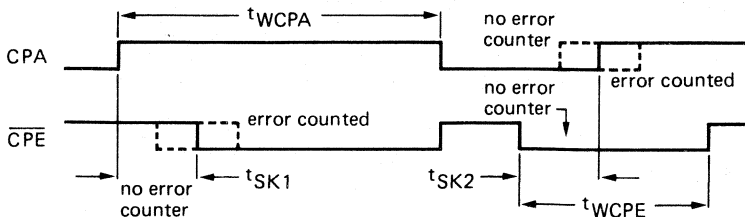


Fig. 4 Skew times timing diagram; $t_{WCPA} > t_{SK1}$; $t_{WCPE} > t_{SK2}$.

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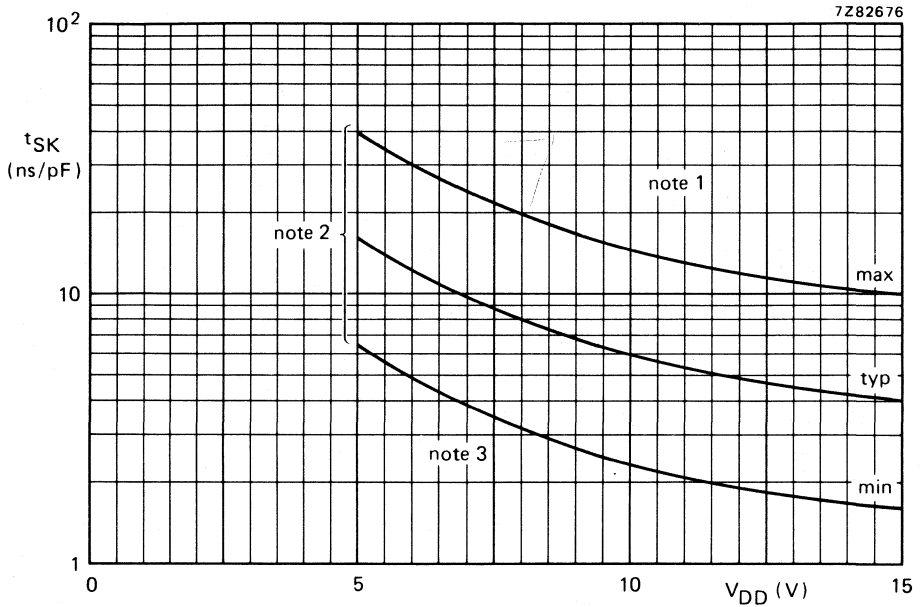


Fig. 5 Typical clock skew as a function of the supply voltage. This graph is accurate for $C_{ext} \geq 100$ pF and $T_{amb} = 25$ °C.

Notes to Fig. 5

1. Skew in this area results in counted error.
2. Skew in the area between max. and min. curves may or may not result in counted error.
3. Skew in this area results in no error counted.

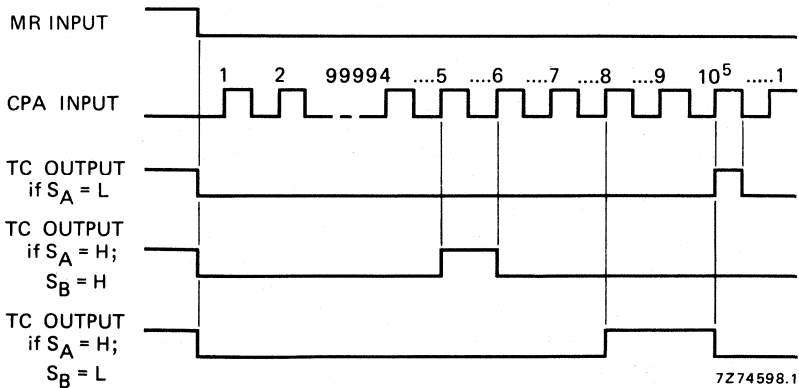


Fig. 6 Carry timing diagram.

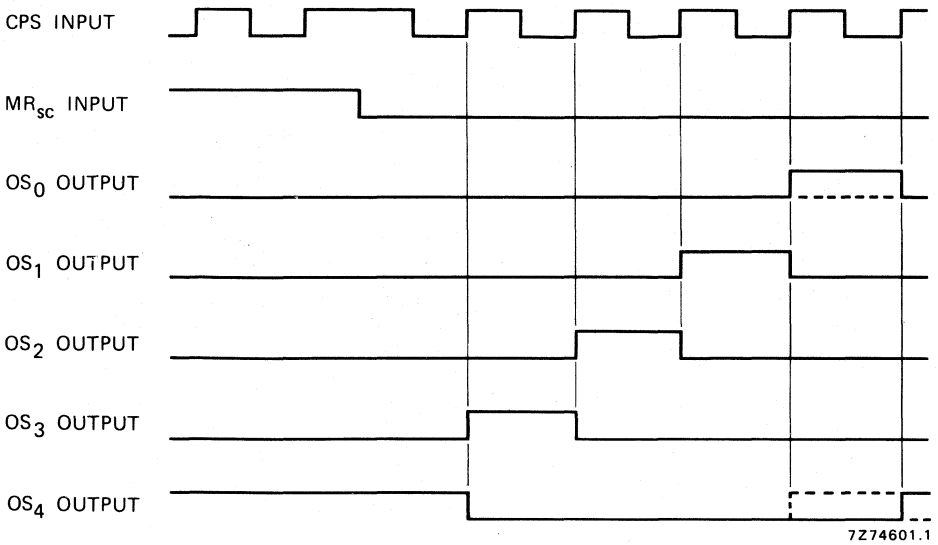


Fig. 7 Scanner timing diagram.

Note: If $S_B = H$, the 1st decade is inhibited and the cycle will be shortened to four stages (see dotted lines).

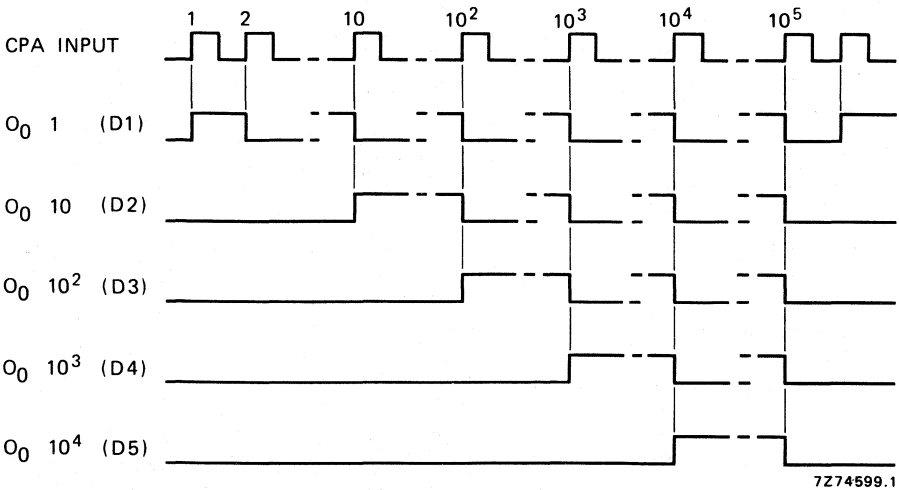


Fig. 8 Counter timing diagram.

A.C. CHARACTERISTICS

 $V_{SS} = 0 \text{ V}; T_{amb} = 25 \text{ }^\circ\text{C}; C_L = 50 \text{ pF};$ input transition times $\leq 20 \text{ ns}$

	V_{DD} V	symbol	min.	typ.	max.	typical extrapolation formula	
Propagation delays							
CPA \rightarrow O_n	5			300	600	ns	283 ns + (0,55 ns/pF) C_L
D1 selected	10	t_{PHL}		130	260	ns	119 ns + (0,23 ns/pF) C_L
HIGH to LOW	15			95	190	ns	87 ns + (0,16 ns/pF) C_L
	5			240	480	ns	213 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		100	200	ns	89 ns + (0,23 ns/pF) C_L
	15			75	150	ns	67 ns + (0,16 ns/pF) C_L
CPA \rightarrow O_n	5			550	1100	ns	523 ns + (0,55 ns/pF) C_L
D5 selected	10	t_{PHL}		230	460	ns	219 ns + (0,23 ns/pF) C_L
HIGH to LOW	15			170	340	ns	162 ns + (0,16 ns/pF) C_L
	5			550	1100	ns	523 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		230	460	ns	219 ns + (0,23 ns/pF) C_L
	15			170	340	ns	162 ns + (0,16 ns/pF) C_L
CPA \rightarrow TC	5			420	840	ns	393 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		190	380	ns	179 ns + (0,23 ns/pF) C_L
	15			140	280	ns	132 ns + (0,16 ns/pF) C_L
MR \rightarrow O_n	5			200	400	ns	173 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		85	170	ns	74 ns + (0,23 ns/pF) C_L
	15			60	120	ns	52 ns + (0,16 ns/pF) C_L
MR \rightarrow OER	5			140	280	ns	113 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		65	130	ns	54 ns + (0,23 ns/pF) C_L
	15			50	100	ns	42 ns + (0,16 ns/pF) C_L
CPS \rightarrow O_n	5			225	450	ns	198 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		95	190	ns	84 ns + (0,23 ns/pF) C_L
	15			70	140	ns	62 ns + (0,16 ns/pF) C_L
	5			225	450	ns	198 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		95	190	ns	84 ns + (0,23 ns/pF) C_L
	15			70	140	ns	62 ns + (0,16 ns/pF) C_L
CPS \rightarrow OS_n	5			170	340	ns	143 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		70	140	ns	59 ns + (0,23 ns/pF) C_L
	15			50	100	ns	42 ns + (0,16 ns/pF) C_L
CPA \rightarrow OS_n	5			170	340	ns	143 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		70	140	ns	59 ns + (0,23 ns/pF) C_L
	15			50	100	ns	42 ns + (0,16 ns/pF) C_L
Output transition times							
HIGH to LOW	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
	10	t_{THL}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V _{DD} V	symbol	min.	typ.	max.	
3-state propagation delays						
Output disable times						
EO → O _n ;	5	tPHZ		30	60	ns
EOS → OS _n	10		25	50	ns	
HIGH	15		20	40	ns	
LOW	5	tPLZ		40	80	ns
	10		25	50	ns	
	15		20	40	ns	
Output enable times						
EO → O _n ;	5	tPZH		35	70	ns
EOS → OS _n	10		20	40	ns	
HIGH	15		15	30	ns	
LOW	5	tPZL		50	100	ns
	10		25	50	ns	
	15		15	30	ns	
Minimum clock pulse width; CPA, CPS	5	tWCPH	70	35		ns
HIGH	10		40	20		ns
	15		30	15		ns
Minimum reset pulse width; MR, MR _{sc}	5	tWMRH	90	45		ns
HIGH	10		60	30		ns
	15		40	20		ns
Recovery time for MR	5	tRMR	120	60		ns
	10		60	30		ns
	15		50	25		ns
Recovery time for MR _{sc}	5	tRMR	60	30		ns
	10		40	20		ns
	15		30	15		ns
Maximum clock pulse frequency CPA and CPS	5	f _{max}	2,5	5		MHz
	10		6	12		MHz
	15		8	16		MHz

	V _{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)*	5	1 100 f _i + Σ(f _o C _L) × V _{DD} ²	f _i = input freq. (MHz)
	10	4 800 f _i + Σ(f _o C _L) × V _{DD} ²	f _o = output freq. (MHz)
	15	12 000 f _i + Σ(f _o C _L) × V _{DD} ²	C _L = load cap. (pF) Σ(f _o C _L) = sum of outputs V _{DD} = supply voltage (V)

* C_{ext} = 0.

APPLICATION INFORMATION

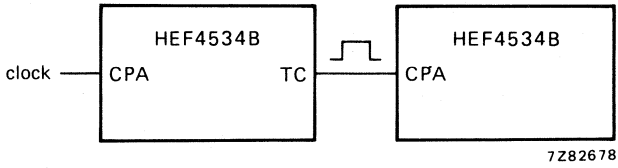


Fig. 9 Two HEF4534B ICs connected for cascade operation. TC is HIGH for a single clock period when all five BCD decads go to zero. TC also goes HIGH when MR is applied.

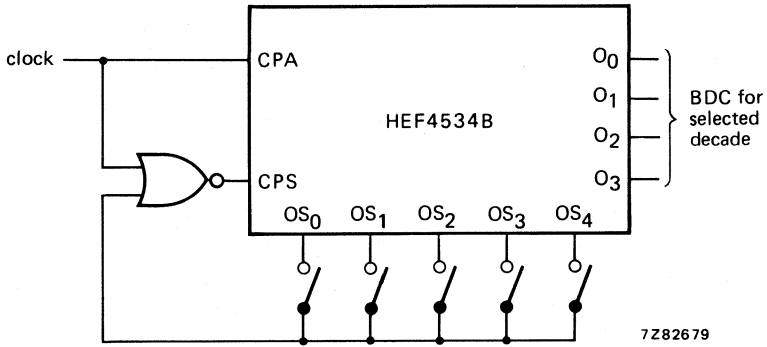


Fig. 10 Forcing a decade to the O_n outputs. When the O_n outputs of a given decade are required, this configuration will lock-up the selected decade within four clock cycles. The select line feed back may be hardwired or switched.

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

DUAL PRECISION MONOSTABLE MULTIVIBRATOR

The HEF4538B is a dual retriggerable-resettable monostable multivibrator. Each multivibrator has an active LOW trigger/retrigger input (\bar{I}_0), an active HIGH trigger/retrigger input (I_1), an overriding active LOW direct reset input (\bar{C}_D), an output (O) and its complement (\bar{O}), and two pins (C_{TC} , R_{TC}) for connecting the external timing components C_t and R_t .

The HEF4538B may be triggered by either the positive or the negative edges of the input pulse and will produce an accurate output pulse with a pulse width range of 10 μ s to infinity. The duration and accuracy of the output pulse are determined by the external timing components C_t and R_t . The output pulse width (T) is equal to $R_t \times C_t$. The linear design techniques in LOC MOS guarantee precise control of the output pulse width.

Schmitt-trigger action in the trigger inputs makes the circuit highly tolerant to slower rise and fall times.

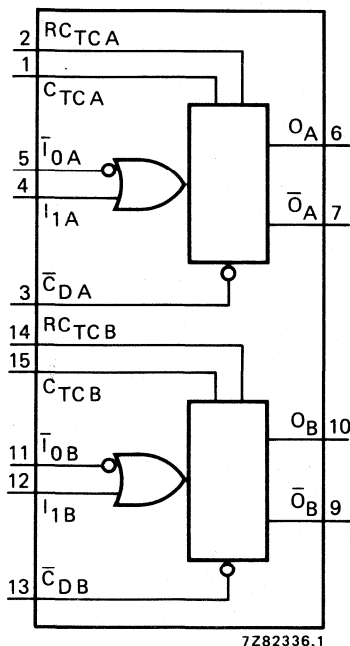


Fig. 1 Functional diagram.

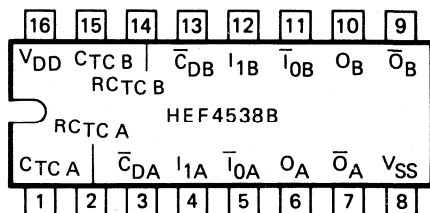


Fig. 2 Pinning diagram.

HEF4538BP: 16-lead DIL; plastic (SOT-38Z).
 HEF4538BD: 16-lead DIL; ceramic (SOT-74).
 HEF4538BT: 16-lead flat pack; plastic (SO-16; SOT-109A).

PINNING

- \bar{I}_0A, \bar{I}_0B input (HIGH to LOW triggered)
- I_1A, I_1B input (LOW to HIGH triggered)
- $\bar{C}_{DA}, \bar{C}_{DB}$ direct reset input (active LOW)
- O_A, O_B output
- \bar{O}_A, \bar{O}_B complementary output (active LOW)
- $C_{TC A}, C_{TC B}$ external capacitor connections
- $R_{TC A}, R_{TC B}$ external capacitor/resistor connections

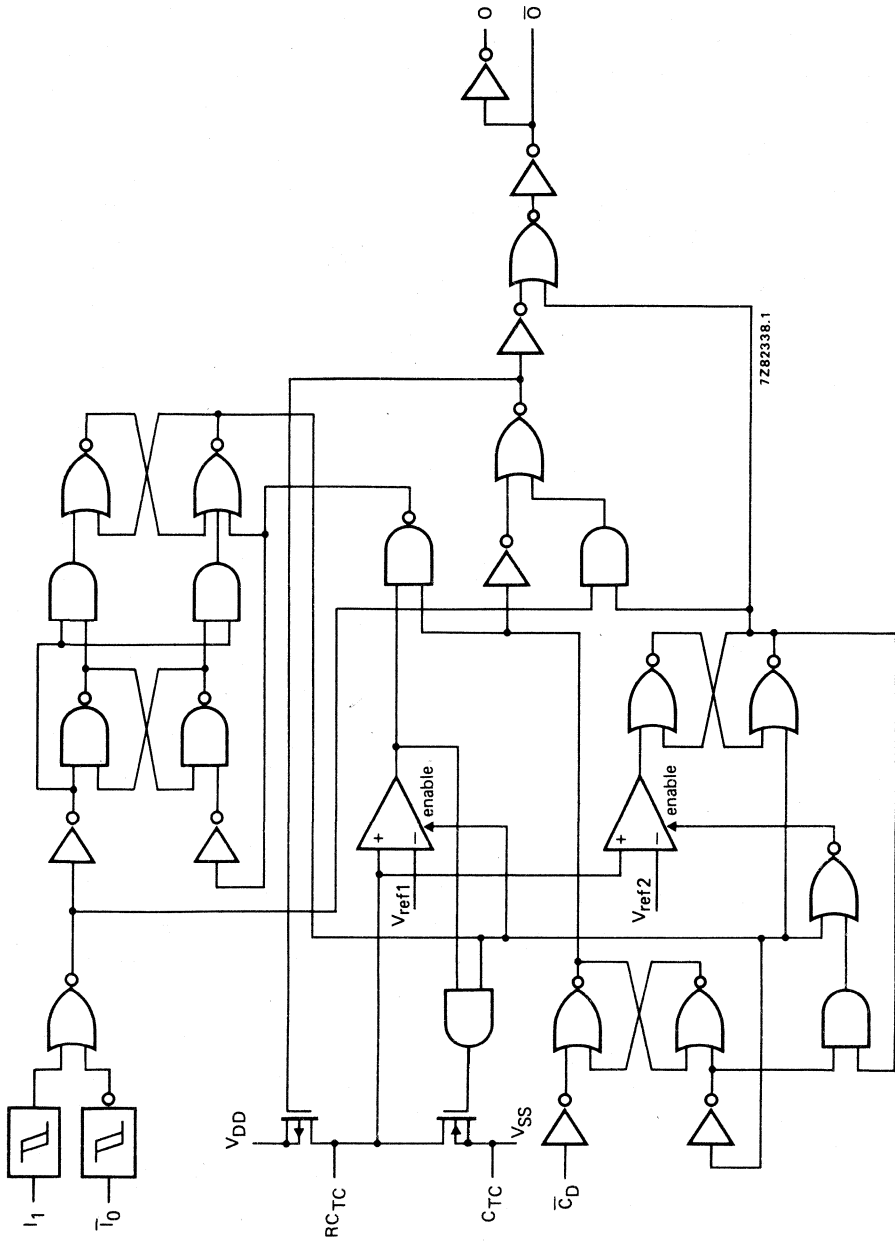
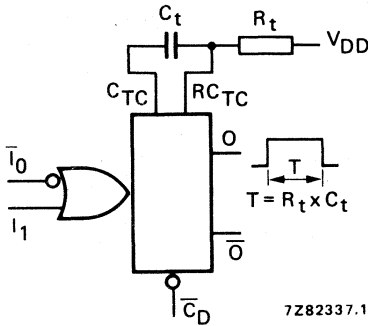


Fig. 3 Logic diagram.

FUNCTION TABLE

inputs			outputs	
\bar{I}_0	I_1	C_D	O	\bar{O}
\searrow	L	H		
H	\swarrow	H		
X	X	L	L	H

H = HIGH state (the more positive voltage)
 L = LOW state (the less positive voltage)
 X = state is immaterial
 \swarrow = positive-going transition
 \searrow = negative-going transition
 = positive output pulse
 = negative output pulse



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Fig. 4 Connection of the external timing components R_t and C_t .

DEVELOPMENT SAMPLE DATA

D.C. CHARACTERISTICS

$V_{SS} = 0\text{ V}$

	V_{DD} V	symbol	T_{amb} (°C)						
			-40		+25		+85		
			typ.	max.	typ.	max.	typ.	max.	
Supply current active state (see note)	5	I_D			35				μA
	10				80				μA
	15				125				μA
Input leakage current (pins 2 and 14)	15	$\pm I_{IN}$			300			1000	nA

Note

Only one monostable is switching: current present during output pulse (output O is HIGH).

A.C. CHARACTERISTICS

 $V_{SS} = 0 \text{ V}$; $T_{amb} = 25 \text{ }^\circ\text{C}$; $C_L = 50 \text{ pF}$; input transition times $\leq 20 \text{ ns}$

	V_{DD} V	symbol	min.	typ.	max.	typical extrapolation formula
Propagation delays $\bar{I}_0, I_1 \rightarrow 0$ HIGH to LOW	5	t_{PHL}		150	ns	$123 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
	10			70	ns	$59 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
	15			40	ns	$32 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
$\bar{I}_0, I_1 \rightarrow \bar{0}$ LOW to HIGH	5	t_{PLH}		150	ns	$123 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
	10			70	ns	$59 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
	15			40	ns	$32 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
$\bar{C}_D \rightarrow 0$ HIGH to LOW	5	t_{PHL}		150	ns	$123 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
	10			70	ns	$59 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
	15			40	ns	$32 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
$\bar{C}_D \rightarrow \bar{0}$ LOW to HIGH	5	t_{PLH}		150	ns	$123 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
	10			70	ns	$59 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
	15			40	ns	$32 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
Recovery times $\bar{C}_D \rightarrow \bar{I}_0, I_1$	5	t_{RCD}		0	ns	
	10			0	ns	
	15			0	ns	
$0, \bar{0} \rightarrow \bar{I}_0, I_1$	5	t_{RO}		0	ns	
	10			0	ns	
	15			0	ns	
Minimum \bar{I}_0 pulse width; LOW	5	t_{WI0L}		60	ns	
	10			30	ns	
	15			20	ns	
Minimum I_1 pulse width; HIGH	5	t_{WI1L}		60	ns	
	10			30	ns	
	15			20	ns	
Minimum \bar{C}_D pulse width; LOW	5	t_{WCDL}		40	ns	
	10			20	ns	
	15			15	ns	
Output 0 or $\bar{0}$ pulse width	5	t_{WO}		208	μs	$\left\{ \begin{array}{l} R_t = 100 \text{ k}\Omega \\ C_t = 0,002 \text{ }\mu\text{F} \end{array} \right.$
	10			208	μs	
	15			208	μs	
Output 0 or $\bar{0}$ pulse width	5	t_{WO}		10,4	ms	$\left\{ \begin{array}{l} R_t = 100 \text{ k}\Omega \\ C_t = 0,1 \text{ }\mu\text{F} \end{array} \right.$
	10			10,4	ms	
	15			10,4	ms	
Output 0 or $\bar{0}$ pulse width	5	t_{WO}		1,04	s	$\left\{ \begin{array}{l} R_t = 100 \text{ k}\Omega \\ C_t = 10 \text{ }\mu\text{F} \end{array} \right.$
	10			1,04	s	
	15			1,04	s	

A.C. CHARACTERISTICS

$V_{SS} = 0 \text{ V}$; $T_{amb} = 25 \text{ }^\circ\text{C}$; $C_L = 50 \text{ pF}$; input transition times $\leq 20 \text{ ns}$

	V_{DD} V	symbol	min.	typ.	max.	
Change in output O pulse width over temperature (T_{amb})	5	Δt_{WO}		$\pm 0,5$		%
	10			$\pm 0,5$		%
	15			$\pm 0,5$		%
Change in output O pulse width over V_{DD} range 5 to 15 V		Δt_{WO}		$\pm 1,5$		%
Pulse width variation between circuits in same package	5	Δt_{WO}		± 1		%
	10			± 1		%
	15			± 1		%
External timing resistor		R_t	5	—	*	$k\Omega$
External timing capacitor		C_t	2000	—	no limits	pF
Input capacitance (pin 2 or 14)		C_{IN}		15		pF

$\left\{ \begin{array}{l} R_t = 100 \text{ k}\Omega \\ C_t = 0,1 \text{ }\mu\text{F} \end{array} \right.$

DEVELOPMENT SAMPLE DATA

* The maximum permissible resistance R_t , which holds the specified accuracy of t_{WO} , depends on the leakage current of the capacitor C_t and the leakage of the HEF4538B.

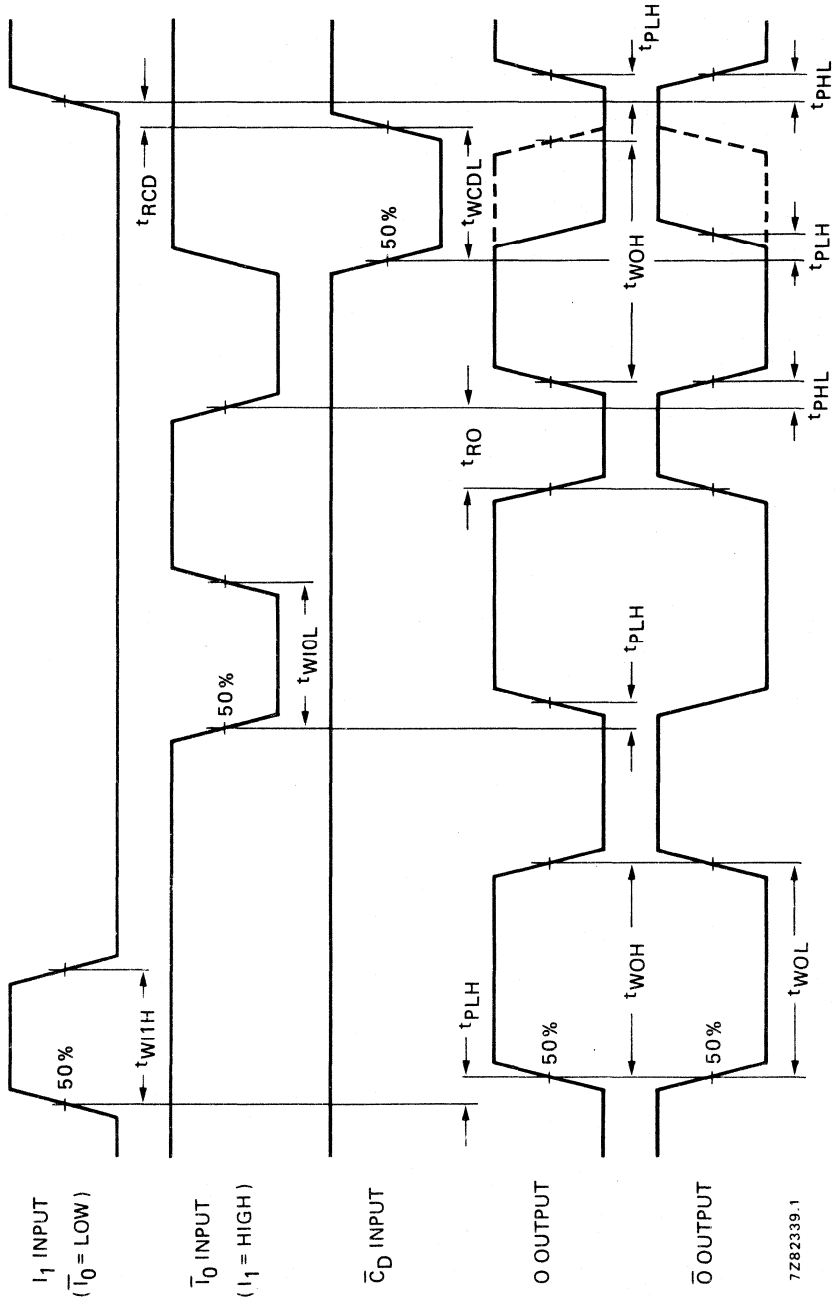
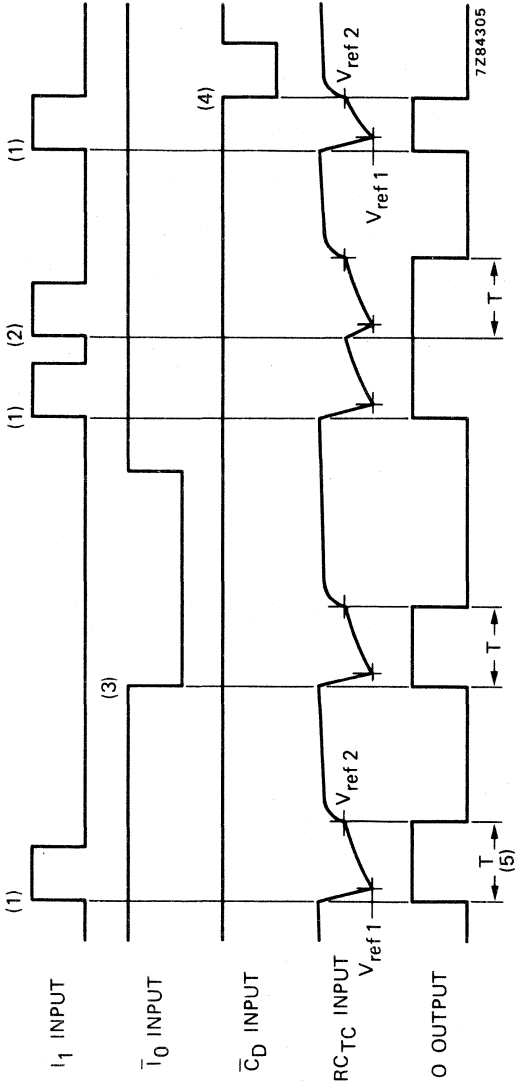


Fig. 5 Waveforms showing minimum \bar{I}_0 , I_1 , O and \bar{C}_D pulse widths, recovery times and propagation delays.

DEVELOPMENT SAMPLE DATA



- (1) Positive edge triggering.
- (2) Positive edge re-triggering (pulse lengthening).
- (3) Negative edge triggering.
- (4) Reset (pulse shortening).
- (5) $T = R_t \times C_t$.

Fig. 6 Timing diagram.

DUAL 4-INPUT MULTIPLEXER



The HEF4539B is a dual 4-input multiplexer with common select logic. Each multiplexer has four multiplexer inputs (I_0 to I_3), an active LOW enable input (\bar{E}) and a multiplexer output (O). When HIGH, \bar{E} forces O of the respective multiplexer LOW, independent of the select inputs (S_0 and S_1) and I_0 to I_3 . When \bar{E} is LOW, S_0 and S_1 determine which multiplexer input (I_0 to I_3) on each of the multiplexers is routed to the respective multiplexer output (O).

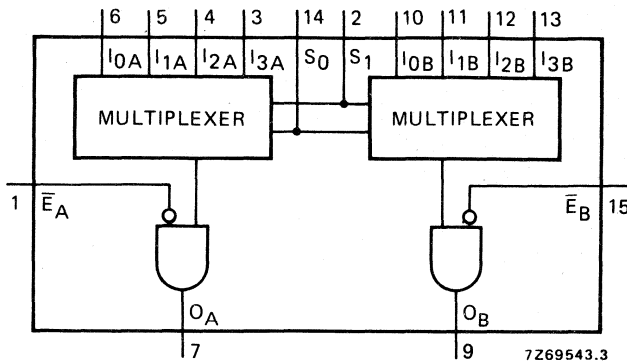


Fig. 1 Functional diagram.

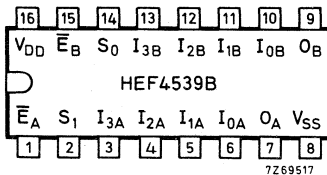


Fig. 2 Pinning diagram.

HEF4539BP: 16-lead DIL; plastic (SOT-38Z).
 HEF4539BD: 16-lead DIL; ceramic (SOT-74).
 HEF4539BT: 16-lead flat pack; plastic
 (SO-16; SOT-109A).

PINNING

I_{0A} , I_{1A} , I_{2A} , I_{3A} multiplexer inputs
 I_{0B} , I_{1B} , I_{2B} , I_{3B} multiplexer inputs
 S_0 , S_1 select inputs
 \bar{E}_A , \bar{E}_B enable inputs (active LOW)
 O_A , O_B multiplexer outputs

FAMILY DATA

I_{DD} LIMITS category MSI

} see Family Specifications

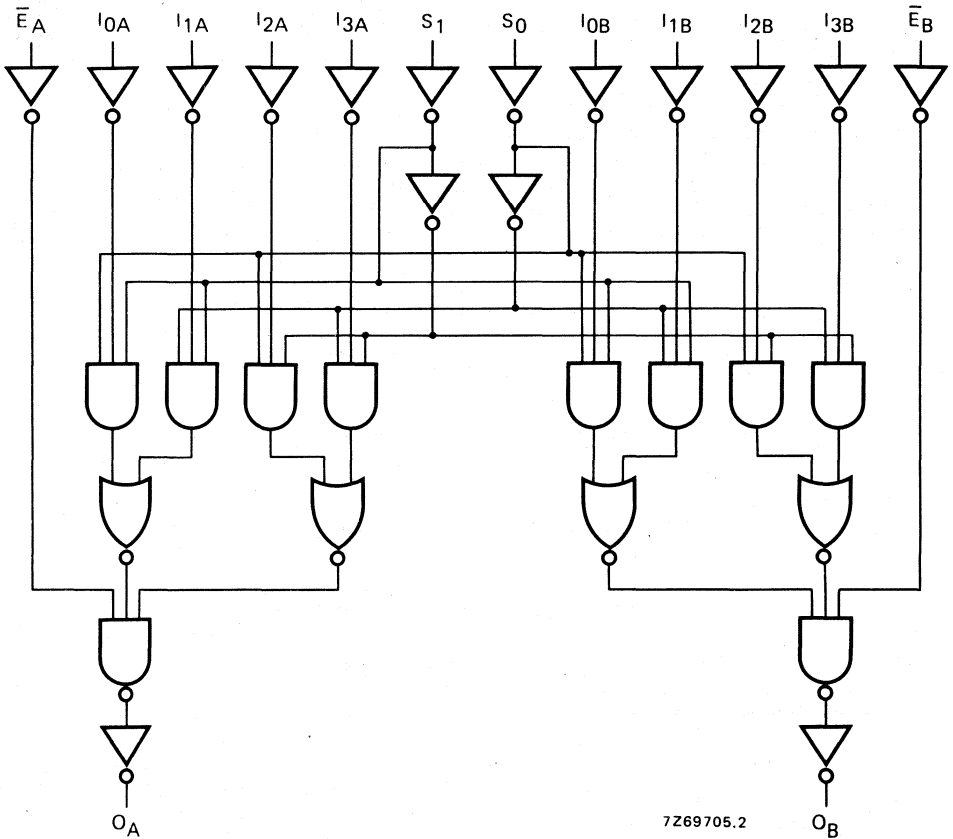


Fig. 3 Logic diagram.

FUNCTION TABLE

inputs			output
S ₀	S ₁	\bar{E}_n	O _n
X	X	H	L
L	L	L	I ₀
H	L	L	I ₁
L	H	L	I ₂
H	H	L	I ₃

H = HIGH state (the more positive voltage)
 L = LOW state (the less positive voltage)
 X = state is immaterial

A.C. CHARACTERISTICS

 $V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	symbol	min.	typ.	max.	typical extrapolation formula	
Propagation delays $I_n \rightarrow O_n$ HIGH to LOW	5	tPHL		120	240	ns	$93\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10		45	90	ns	$34\text{ ns} + (0,23\text{ ns/pF}) C_L$	
	15		30	60	ns	$22\text{ ns} + (0,16\text{ ns/pF}) C_L$	
LOW to HIGH	5	tPLH		120	245	ns	$93\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10		50	100	ns	$39\text{ ns} + (0,23\text{ ns/pF}) C_L$	
	15		35	65	ns	$27\text{ ns} + (0,16\text{ ns/pF}) C_L$	
$S_n \rightarrow O_n$ HIGH to LOW	5	tPHL		165	330	ns	$138\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10		65	125	ns	$54\text{ ns} + (0,23\text{ ns/pF}) C_L$	
	15		40	80	ns	$32\text{ ns} + (0,16\text{ ns/pF}) C_L$	
LOW to HIGH	5	tPLH		155	310	ns	$128\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10		60	120	ns	$49\text{ ns} + (0,23\text{ ns/pF}) C_L$	
	15		40	80	ns	$32\text{ ns} + (0,16\text{ ns/pF}) C_L$	
$E_n \rightarrow O_n$ HIGH to LOW	5	tPHL		100	200	ns	$73\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10		40	80	ns	$29\text{ ns} + (0,23\text{ ns/pF}) C_L$	
	15		30	55	ns	$22\text{ ns} + (0,16\text{ ns/pF}) C_L$	
LOW to HIGH	5	tPLH		100	200	ns	$73\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10		40	80	ns	$29\text{ ns} + (0,23\text{ ns/pF}) C_L$	
	15		30	55	ns	$22\text{ ns} + (0,16\text{ ns/pF}) C_L$	
Output transition times HIGH to LOW	5	tTHL		60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$
	10		30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$	
	15		20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$	
LOW to HIGH	5	tTLH		60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$
	10		30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$	
	15		20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$	

	V_{DD} V	typical formula for P (μW)	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
Dynamic power dissipation per package (P)	5	$700 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	10	$2900 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$8100 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

APPLICATION INFORMATION

Some examples of applications for the HEF4539B are:

- Data selectors.
- Data multiplexers.



PROGRAMMABLE TIMER

The HEF4541B is a programmable timer which consists of a 16-stage binary counter, an integrated oscillator to be used with external timing components, an automatic power-on reset and output control logic. The frequency of the oscillator is determined by the external components R_T and C_T within the frequency range 1 Hz to 100 kHz. This oscillator may be replaced by an external clock signal at input RS, the timer advances on the positive-going transition of RS. A LOW on the auto reset input (\overline{AR}) and a LOW on the master reset input (MR) enables the internal power-on reset. A HIGH level at input MR resets the counter independent of all other inputs.

A HIGH at input \overline{AR} turns off the power-on reset to provide a low quiescent power dissipation of the timer. The 16-stage counter divides the oscillator frequency by 2^8 , 2^{10} , 2^{13} or 2^{16} depending on the state of the address inputs (A_0 , A_1). The divided oscillator frequency is available at output O. The phase input (PH) features a complementary output signal. If the mode select input (MODE) is LOW or HIGH the timer can be used respectively as a single transition timer or 2^n frequency divider.

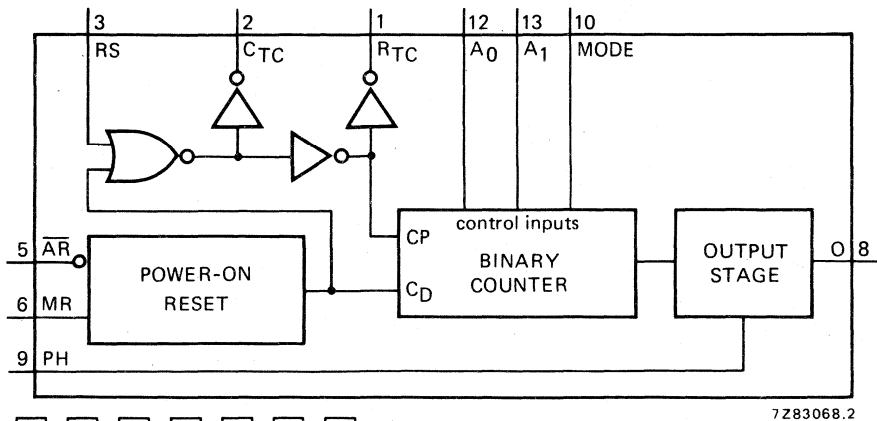


Fig. 1 Functional diagram.

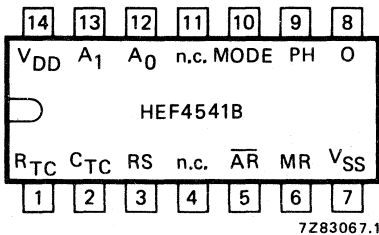


Fig. 2 Pinning diagram.

HEF4541BP: 14-lead DIL; plastic (SOT-27S, T, V).
 HEF4541BD: 14-lead DIL; ceramic (SOT-73).
 HEF4541BT: 14-lead flat pack; plastic (SO-14; SOT-108A).

FAMILY DATA

I_{DD} LIMITS category MSI

see Family Specifications

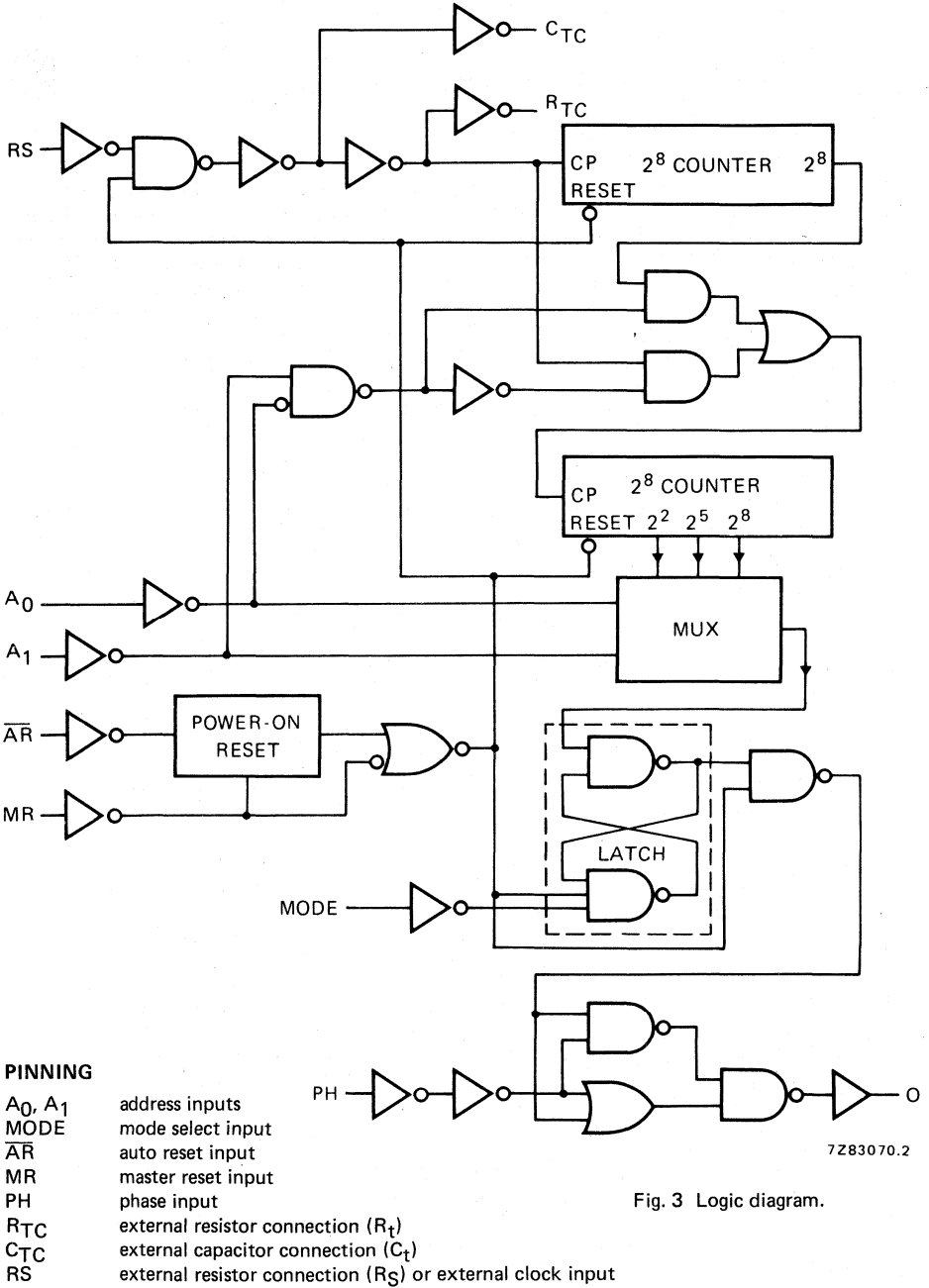


Fig. 3 Logic diagram.

FREQUENCY SELECTION TABLE

A ₀	A ₁	number of counter stages n	$\frac{f_{osc}}{f_{out}} = 2^n$
L	L	13	8 192
L	H	10	1 024
H	L	8	256
H	H	16	65 536

FUNCTION TABLE

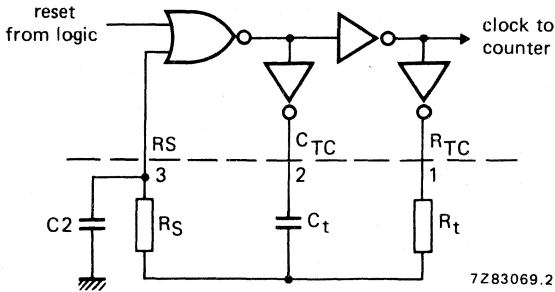
inputs				mode
\overline{AR}	MR	PH	MODE	
H	L	X	X	auto reset disabled
L	L	X	X	auto reset enabled
X	H	X	X	master reset active
X	L	X	H	normal operation selected
X	L	X	L	division to output
X	L	L	X	single-cycle mode* output initially LOW, after reset
X	L	H	X	output initially HIGH, after reset

H = HIGH state (the more positive voltage)
 L = LOW state (the less positive voltage)
 X = state is immaterial

* The timer is initialized on a reset pulse and the output changes state after 2^{n-1} counts and remains in that state (latched). Reset of this latch is obtained by master reset or by a LOW to HIGH transition on the MODE input.



RC oscillator



Typical formula for oscillator frequency:

$$f_{osc} = \frac{1}{2,3 \times R_t \times C_t}$$

Fig. 4 External component connection for RC oscillator; $R_S \approx 2R_t$.

Timing component limitations

The oscillator frequency is mainly determined by $R_t C_t$, provided $R_t \ll R_S$ and $R_S C_2 \ll R_t C_t$. The function of R_S is to minimize the influence of the forward voltage across the input protection diodes on the frequency. The stray capacitance C_2 should be kept as small as possible. In consideration of accuracy, C_t must be larger than the inherent stray capacitance. R_t must be larger than the LOCMOS 'ON' resistance in series with it, which typically is 500Ω at $V_{DD} = 5 \text{ V}$, 300Ω at $V_{DD} = 10 \text{ V}$ and 200Ω at $V_{DD} = 15 \text{ V}$.

The recommended values for these components to maintain agreement with the typical oscillation formula are:

- $C_t \geq 100 \text{ pF}$, up to any typical value,
- $10 \text{ k}\Omega \leq R_t \leq 1 \text{ M}\Omega$.

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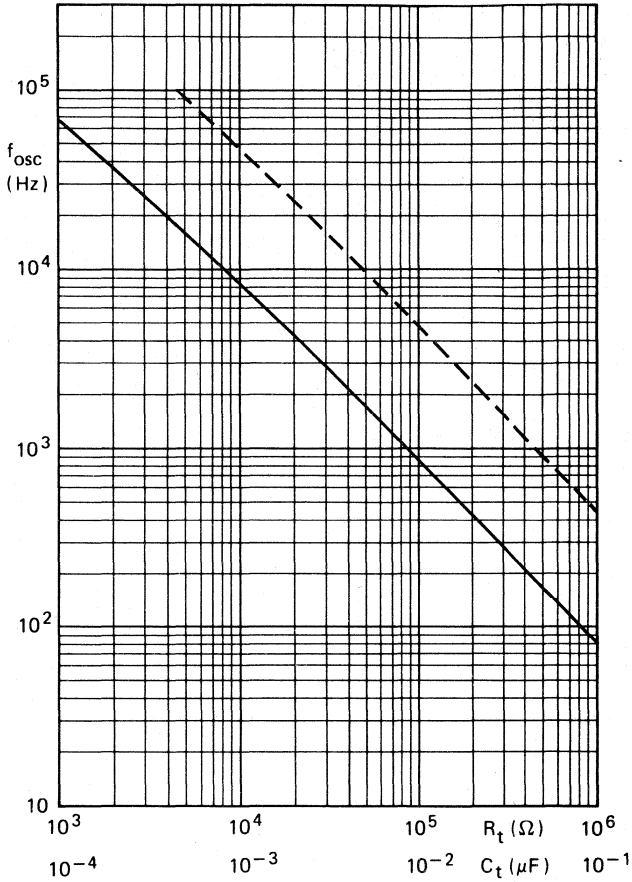


Fig. 5 RC oscillator frequency as a function of R_t and C_t at $V_{DD} = 5$ to 15 V; $T_{amb} = 25$ °C.

— C_t curve at $R_t = 56$ k Ω ; $R_S = 120$ k Ω .
 - - - R_t curve at $C_t = 1$ nF; $R_S = 2R_t$.

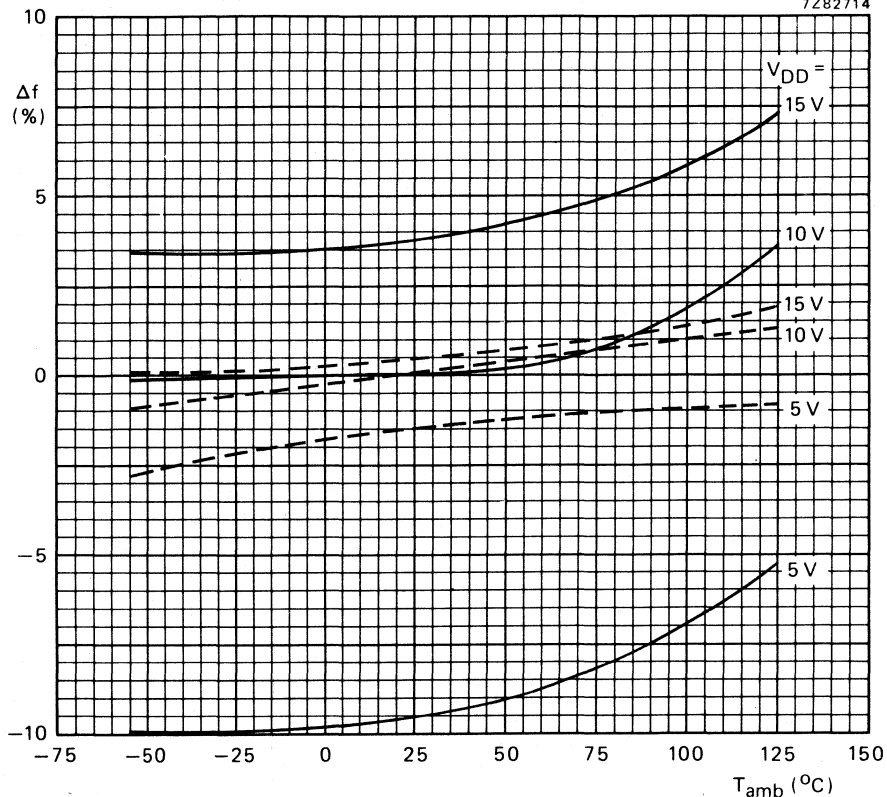


Fig. 6 Frequency deviation (Δf) as a function of ambient temperature; referenced at : f_{osc} at $T_{amb} = 25^\circ\text{C}$ and $V_{DD} = 10 \text{ V}$.

- $R_t = 56 \text{ k}\Omega$; $C_t = 1 \text{ nF}$; $R_S = 0$.
- - - $R_t = 56 \text{ k}\Omega$; $C_t = 1 \text{ nF}$; $R_S = 120 \text{ k}\Omega$.

D.C. CHARACTERISTICS

V_{SS} = 0 V

	V _{DD} V	V _{OL} V	V _{OH} V	symbol	T _{amb} (°C)							
					-40		+25		+85			
					min.	max.	min.	typ.	max.	min.	max.	
Supply current power-on reset enabled (note)	5			I _D	—	80	—	20	80	—	230	
	10				—	750	—	250	600	—	700	
	15				—	1600	—	500	1300	—	1500	
Supply voltage for automatic reset initialization (note)				V _{DD}	—	—	8,5	5	—	—	—	
Output current HIGH; C _{TC} , R _{TC}	5		4,6	-I _{OH}	0,5	—	0,4	—	—	0,3	—	
	10		9,5		1,4	—	1,2	—	—	0,95	—	
	15		13,5		4,8	—	4,0	—	—	3,2	—	
Output current LOW; C _{TC} , R _{TC}	5		2,5	-I _{OH}	1,4	—	1,2	—	—	0,95	—	
	10	0,4			I _{OL}	0,33	—	0,27	—	—	0,20	—
	15	1,5				1,00	—	0,85	—	—	0,68	—
				3,20		—	2,70	—	—	2,30	—	

Note

All inputs at 0 V or V_{DD}, except input \overline{AR} = input MR = 0 V (power-on reset active).

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ≤ 20 ns

	V _{DD} V	typical formula for P (μW)*
Dynamic power dissipation per package (P)	5	1 300 f _i + f _o C _L V _{DD} ²
	10	5 300 f _i + f _o C _L V _{DD} ²
	15	12 000 f _i + f _o C _L V _{DD} ²
Total power dissipation when using the on-chip oscillator (P)	5	1 300 f _{osc} + f _o C _L V _{DD} ² + 2C _t V _{DD} ² f _{osc} + 10 V _{DD}
	10	5 300 f _{osc} + f _o C _L V _{DD} ² + 2C _t V _{DD} ² f _{osc} + 100 V _{DD}
	15	12 000 f _{osc} + f _o C _L V _{DD} ² + 2C _t V _{DD} ² f _{osc} + 400 V _{DD}

* where:

- f_i = input frequency (MHz)
- f_o = output frequency (MHz)
- C_L = load capacitance (pF)
- V_{DD} = supply voltage (V)
- C_t = timing capacitance (pF)
- f_{osc} = oscillator frequency (MHz)

A.C. CHARACTERISTICS

 $V_{SS} = 0 \text{ V}$; $T_{amb} = 25 \text{ }^\circ\text{C}$; $C_L = 50 \text{ pF}$; input transition times $\leq 20 \text{ ns}$

	V_{DD} V	symbol	min.	typ.	max.	typical extrapolation formula
Propagation delays						
RS \rightarrow 0						
2^8 selected	5			375	750 ns	$348 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
HIGH to LOW	10	t _{PHL}		150	300 ns	$139 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
LOW to HIGH	15	t _{PLH}		110	220 ns	$102 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
RS \rightarrow 0						
2^{10} selected	5			425	850 ns	$398 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
HIGH to LOW	10	t _{PHL}		165	330 ns	$154 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
LOW to HIGH	15	t _{PLH}		120	240 ns	$112 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
RS \rightarrow 0						
2^{13} selected	5			510	1020 ns	$483 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
HIGH to LOW	10	t _{PHL}		190	380 ns	$179 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
LOW to HIGH	15	t _{PLH}		135	270 ns	$127 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
RS \rightarrow 0						
2^{16} selected	5			575	1150 ns	$548 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
HIGH to LOW	10	t _{PHL}		210	420 ns	$199 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
LOW to HIGH	15	t _{PLH}		150	300 ns	$142 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
Minimum clock	5		60	30	ns	
pulse width; LOW	10	t _{WRSL}	30	15	ns	
	15		24	12	ns	
Minimum reset	5		60	30	ns	
pulse width; HIGH	10	t _{WMRH}	30	15	ns	
	15		24	12	ns	
Maximum clock	5		8	16	MHz	
pulse frequency	10	f _{max}	15	30	MHz	
	15		18	36	MHz	
Oscillator frequency	5			90	kHz	} $R_t = 5 \text{ k}\Omega$ $C_t = 1 \text{ nF}$ $R_S = 10 \text{ k}\Omega$
	10	f _{osc}		90	kHz	
	15			90	kHz	
Oscillator frequency	5			8	kHz	} $R_t = 56 \text{ k}\Omega$ $C_t = 1 \text{ nF}$ $R_S = 120 \text{ k}\Omega$
	10	f _{osc}		8	kHz	
	15			8	kHz	

BCD TO 7-SEGMENT LATCH/DECODER/DRIVER



The HEF4543B is a BCD to 7-segment latch/decoder/driver for liquid crystal and LED displays. It has four address inputs (D_A to D_D), an active HIGH latch disable input (LD), an active HIGH blanking input (BI), an active HIGH phase input (PH) and seven buffered segment outputs (O_a to O_g).

The circuit provides the function of a 4-bit storage latch and an 8-4-2-1 BCD to 7-segment decoder/driver. It can invert the logic levels of the output combination. The phase (PH), blanking (BI) and latch disable (LD) inputs are used to reverse the function table phase, blank the display and store a BCD code, respectively.

For liquid crystal displays a square-wave is applied to PH and the electrical common back-plane of the display. The outputs of the device are directly connected to the segments of the liquid crystal.

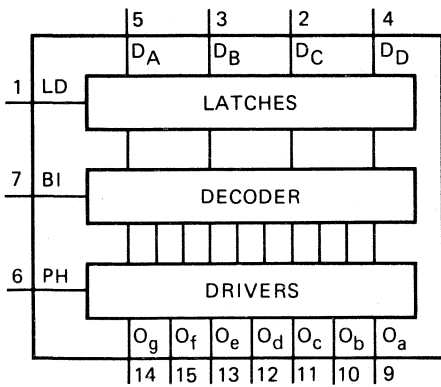
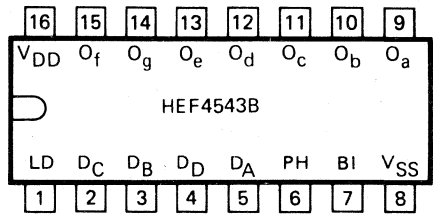


Fig. 1 Functional diagram. 7Z72880.2



7Z72881.1

Fig. 2 Pinning diagram.

- HEF4543BP: 16-lead DIL; plastic (SOT-38Z).
- HEF4543BD: 16-lead DIL; ceramic (SOT-74).
- HEF4543BT: 16-lead flat pack; plastic (SO-16; SOT-109A).

PINNING

- D_A to D_D address (data) inputs
- PH phase input (active HIGH)
- BI blanking input (active HIGH)
- LD latch disable input (active HIGH)
- O_a to O_g segment outputs

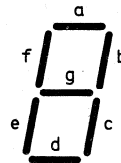
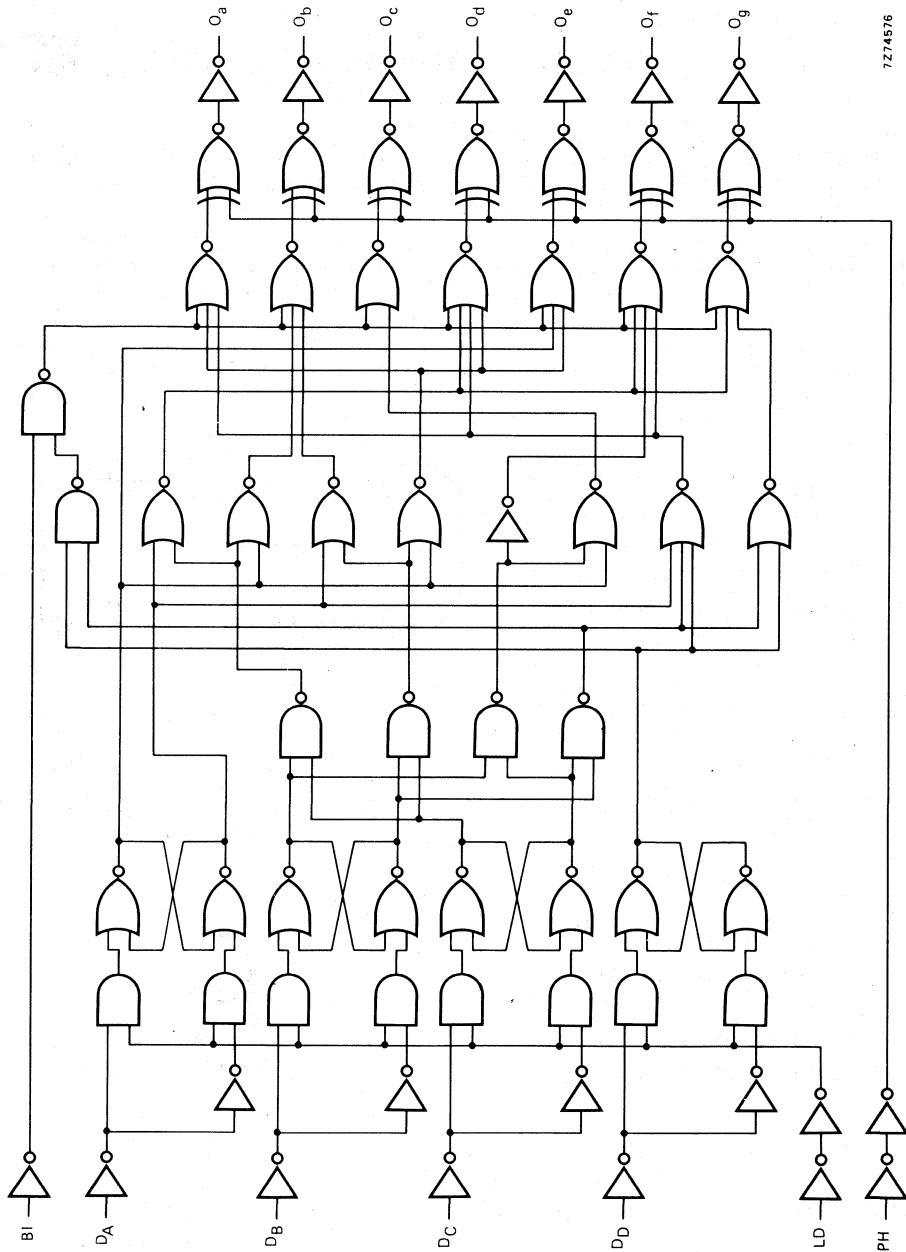


Fig. 3 Segment designation.

FAMILY DATA

I_{DD} LIMITS category MSI

see Family Specifications



7274576

Fig. 4 Logic diagram.

FUNCTION TABLE

inputs							outputs							
LD	BI	PH *	D _D	D _C	D _B	D _A	O _a	O _b	O _c	O _d	O _e	O _f	O _g	display
X	H	L	X	X	X	X	L	L	L	L	L	L	L	blank
H	L	L	L	L	L	L	H	H	H	H	H	H	L	0
H	L	L	L	L	L	H	L	H	H	L	L	L	L	1
H	L	L	L	L	H	L	H	H	L	H	H	L	H	2
H	L	L	L	L	H	H	H	H	H	H	L	L	H	3
H	L	L	L	H	L	L	L	H	H	L	L	H	H	4
H	L	L	L	H	L	H	H	L	H	L	L	H	H	5
H	L	L	L	H	H	L	H	L	H	H	H	H	H	6
H	L	L	L	H	H	H	H	H	H	L	L	L	L	7
H	L	L	H	L	L	L	H	H	H	H	H	H	H	8
H	L	L	H	L	L	H	H	H	H	L	L	H	H	9
H	L	L	H	L	H	L	L	L	L	L	L	L	L	blank
H	L	L	H	L	H	H	L	L	L	L	L	L	L	blank
H	L	L	H	H	L	L	L	L	L	L	L	L	L	blank
H	L	L	H	H	L	H	L	L	L	L	L	L	L	blank
H	L	L	H	H	H	L	L	L	L	L	L	L	L	blank
H	L	L	H	H	H	H	L	L	L	L	L	L	L	blank
L	L	L	X	X	X	X				**				**
as above		H	as above				inverse of above							as above

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

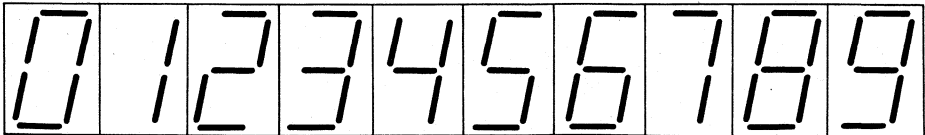
X = state is immaterial

* For liquid crystal displays, apply a square-wave to PH.

For common cathode LED displays, select PH = LOW.

For common anode LED displays, select PH = HIGH.

** Depends upon the BCD-code previously applied when LD = HIGH.



7Z72882

Fig. 5 Display.

A.C. CHARACTERISTICS

 $V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	symbol	min.	typ.	max.	typical extrapolation formula					
Propagation delays	5	$D_n \rightarrow O_n$ HIGH to LOW	180	360	ns	$153\text{ ns} + (0,55\text{ ns/pF}) C_L$					
							10	75	150	ns	$64\text{ ns} + (0,23\text{ ns/pF}) C_L$
	5	180	360	ns	$153\text{ ns} + (0,55\text{ ns/pF}) C_L$						
						10	75	150	ns	$64\text{ ns} + (0,23\text{ ns/pF}) C_L$	
											15
	5	170	340	ns	$143\text{ ns} + (0,55\text{ ns/pF}) C_L$						
						10	80	160	ns	$69\text{ ns} + (0,23\text{ ns/pF}) C_L$	
											15
	5	190	380	ns	$163\text{ ns} + (0,55\text{ ns/pF}) C_L$						
						10	80	160	ns	$69\text{ ns} + (0,23\text{ ns/pF}) C_L$	
											15
	5	145	290	ns	$118\text{ ns} + (0,55\text{ ns/pF}) C_L$						
						10	65	130	ns	$54\text{ ns} + (0,23\text{ ns/pF}) C_L$	
											15
	5	125	250	ns	$98\text{ ns} + (0,55\text{ ns/pF}) C_L$						
						10	55	110	ns	$54\text{ ns} + (0,23\text{ ns/pF}) C_L$	
											15
5	60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$							
					10	30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$		
										15	20
5	60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$							
					10	30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$		
										15	20
5	60	30	ns								
					10	30	15	ns			
										15	20
5	40	20	ns								
					10	20	5	ns			
										15	15
5	0	-15	ns								
					10	15	0	ns			
										15	20

	V_{DD} V	typical formula for P (μW)	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
Dynamic power dissipation per package (P)	5	$2\,200 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	10	$10\,400 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$33\,000 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

APPLICATION INFORMATION

Some examples of applications for the HEF4543B are:

- Driving LCD displays.
- Driving LED displays.
- Driving fluorescent displays
- Driving incandescent displays.
- Driving gas discharge displays.

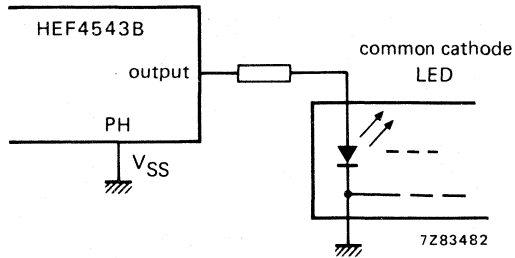


Fig. 6 Connection to common cathode LED display readout.

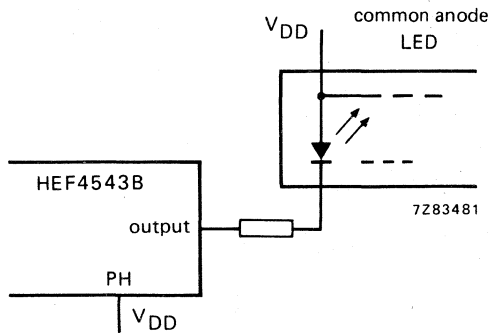


Fig. 7 Connection to common anode LED display readout.

Note to Figs 6 and 7: bipolar transistors may be added for gain where $V_{DD} \leq 10\text{ V}$ or $I_{out} \geq 10\text{ mA}$.

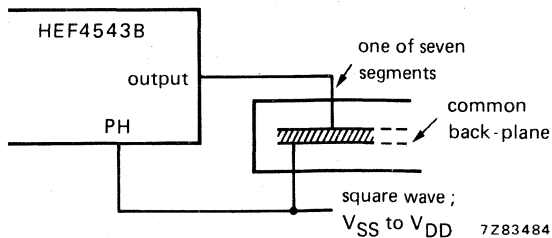


Fig. 8 Connection to liquid crystal (LCD) display readout.

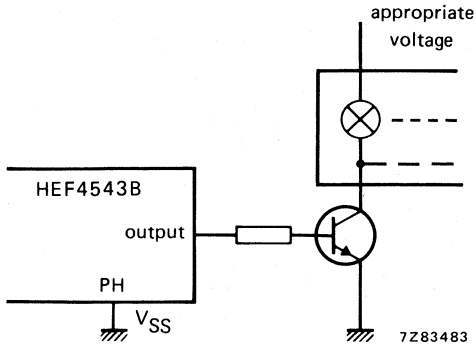


Fig. 9 Connection to incandescent display readout.

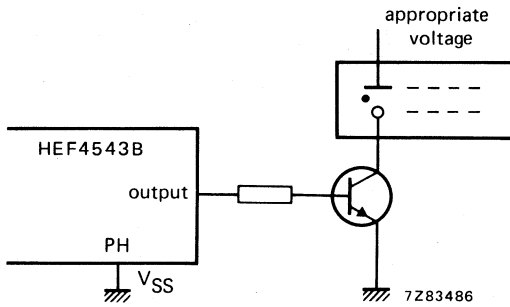


Fig. 10 Connection to gas discharge display readout.

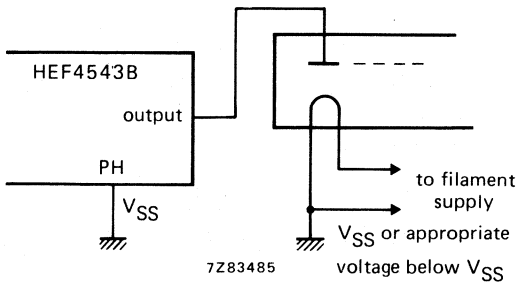


Fig. 11 Connection to fluorescent display readout.

DUAL 1-OF-4 DECODER/DEMULTIPLEXER



The HEF4555B is a dual 1-of-4 decoder/demultiplexer. Each has two address inputs (A_0 and A_1), an active LOW enable input (\bar{E}) and four mutually exclusive outputs which are active HIGH (O_0 to O_3). When used as a decoder, \bar{E} when HIGH, forces O_0 to O_3 LOW. When used as a demultiplexer, the appropriate output is selected by the information on A_0 and A_1 with \bar{E} as data input. All unselected outputs are LOW.

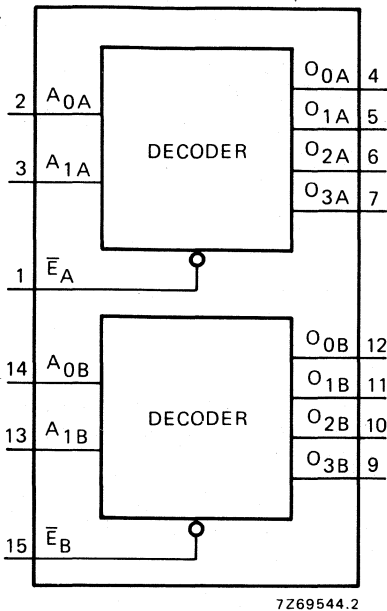


Fig. 1 Functional diagram.



Fig. 2 Pinning diagram.

- HEF4555BP: 16-lead DIL; plastic (SOT-38Z).
- HEF4555BD: 16-lead DIL; ceramic (SOT-74).
- HEF4555BT: 16-lead flat pack; plastic (SO-16; SOT-109A).

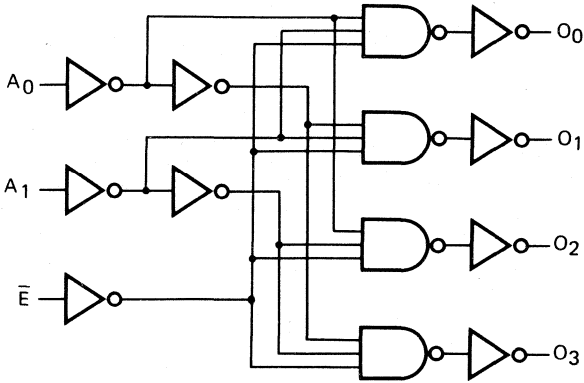
PINNING

- \bar{E} enable inputs (active LOW)
- A_0 and A_1 address inputs
- O_0 to O_3 outputs (active HIGH)

FAMILY DATA

I_{DD} LIMITS category MSI

} see Family Specifications



7Z69728.1

Fig. 3 Logic diagram (one decoder/multiplexer).

TRUTH TABLE

inputs			outputs			
\bar{E}	A ₀	A ₁	O ₀	O ₁	O ₂	O ₃
L	L	L	H	L	L	L
L	H	L	L	H	L	L
L	L	H	L	L	H	L
L	H	H	L	L	L	H
H	X	X	L	L	L	L

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

A.C. CHARACTERISTICS

 $V_{SS} = 0 \text{ V}$; $T_{amb} = 25 \text{ }^\circ\text{C}$; $C_L = 50 \text{ pF}$; input transition times $\leq 20 \text{ ns}$

	V_{DD} V	symbol	min.	typ.	max.	typical extrapolation formula	
Propagation delays $A_n \rightarrow O_n$ HIGH to LOW	5	t_{PHL}	115	230	ns	$88 \text{ ns} + (0,55 \text{ ns/pF}) C_L$	
	10		45	90	ns	$34 \text{ ns} + (0,23 \text{ ns/pF}) C_L$	
	15		30	65	ns	$22 \text{ ns} + (0,16 \text{ ns/pF}) C_L$	
	LOW to HIGH	5	t_{PLH}	140	280	ns	$113 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
		10		55	105	ns	$44 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
		15		40	75	ns	$32 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
$\bar{E}_n \rightarrow O_n$ HIGH to LOW	5	t_{PHL}	125	250	ns	$98 \text{ ns} + (0,55 \text{ ns/pF}) C_L$	
	10		50	95	ns	$39 \text{ ns} + (0,23 \text{ ns/pF}) C_L$	
	15		30	65	ns	$22 \text{ ns} + (0,16 \text{ ns/pF}) C_L$	
	LOW to HIGH	5	t_{PLH}	150	295	ns	$123 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
		10		55	110	ns	$44 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
		15		40	75	ns	$32 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
Output transition times HIGH to LOW	5	t_{THL}	60	120	ns	$10 \text{ ns} + (1,0 \text{ ns/pF}) C_L$	
	10		30	60	ns	$9 \text{ ns} + (0,42 \text{ ns/pF}) C_L$	
	15		20	40	ns	$6 \text{ ns} + (0,28 \text{ ns/pF}) C_L$	
	LOW to HIGH	5	t_{TLH}	60	120	ns	$10 \text{ ns} + (1,0 \text{ ns/pF}) C_L$
		10		30	60	ns	$9 \text{ ns} + (0,42 \text{ ns/pF}) C_L$
		15		20	40	ns	$6 \text{ ns} + (0,28 \text{ ns/pF}) C_L$

	V_{DD} V	typical formula for P (μW)	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
Dynamic power dissipation per package (P)	5	$4500 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	10	$18\,800 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$45\,700 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

APPLICATION INFORMATION

Some examples of applications for the HEF4555B are:

- Code conversion.
- Address decoding.
- Demultiplexing: when using the enable input as data input.

DUAL 1-OF-4 DECODER/DEMULTIPLEXER



The HEF4556B is a dual 1-of-4 decoder/demultiplexer. Each has two address inputs (A_0 and A_1), an active LOW enable input (\bar{E}) and four mutually exclusive outputs which are active LOW (\bar{O}_0 to \bar{O}_3). When used as a decoder, \bar{E} when HIGH, forces \bar{O}_0 to \bar{O}_3 HIGH. When used as a demultiplexer, the appropriate output is selected by the information on A_0 and A_1 with \bar{E} as data input. All unselected outputs are HIGH.

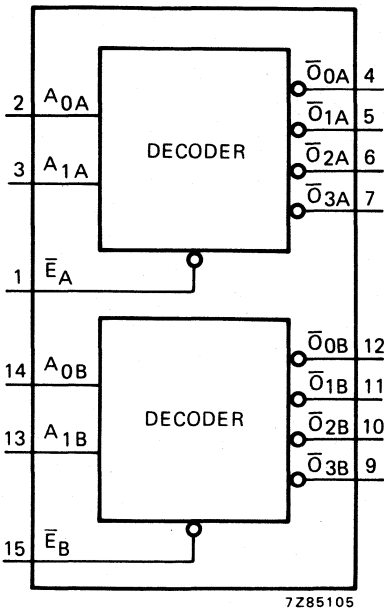


Fig. 1 Functional diagram.



Fig. 2 Pinning diagram.

- HEF4556BP: 16-lead DIL; plastic (SOT-38Z).
- HEF4556BD: 16-lead DIL; ceramic (SOT-74).
- HEF4556BT: 16-lead flat pack; plastic (SO-16; SOT-109A).

PINNING

- \bar{E} enable inputs (active LOW)
- A_0 and A_1 address inputs
- \bar{O}_0 to \bar{O}_3 outputs (active LOW)

FAMILY DATA

I_{DD} LIMITS category MSI

} see Family Specifications

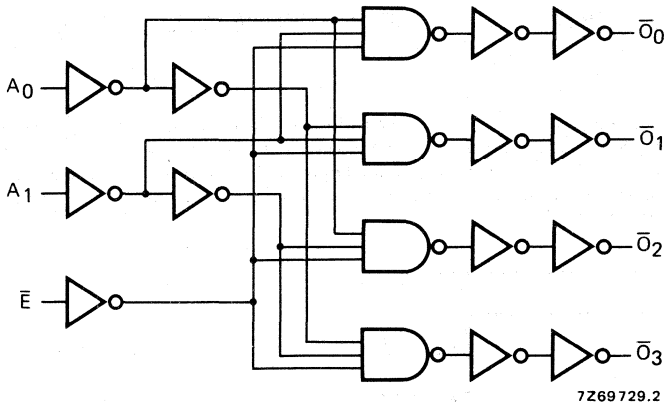


Fig. 3 Logic diagram (one decoder/multiplexer).

TRUTH TABLE

inputs			outputs			
\bar{E}	A_0	A_1	\bar{O}_0	\bar{O}_1	\bar{O}_2	\bar{O}_3
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L
H	X	X	H	H	H	H

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

A.C. CHARACTERISTICS

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	symbol	min.	typ.	max.	typical extrapolation formula		
Propagation delays $A_n \rightarrow \bar{O}_n$ HIGH to LOW	5	tPHL		130	255	ns	$103\text{ ns} + (0,55\text{ ns/pF}) C_L$	
	10		50	100	ns	$39\text{ ns} + (0,23\text{ ns/pF}) C_L$		
	15		35	65	ns	$27\text{ ns} + (0,16\text{ ns/pF}) C_L$		
	LOW to HIGH	5	tPLH		105	210	ns	$78\text{ ns} + (0,55\text{ ns/pF}) C_L$
		10		40	85	ns	$29\text{ ns} + (0,23\text{ ns/pF}) C_L$	
		15		30	60	ns	$22\text{ ns} + (0,16\text{ ns/pF}) C_L$	
$\bar{E}_n \rightarrow \bar{O}_n$ HIGH to LOW	5	tPHL		120	240	ns	$93\text{ ns} + (0,55\text{ ns/pF}) C_L$	
	10		45	90	ns	$34\text{ ns} + (0,23\text{ ns/pF}) C_L$		
	15		30	60	ns	$22\text{ ns} + (0,16\text{ ns/pF}) C_L$		
	LOW to HIGH	5	tPLH		105	205	ns	$78\text{ ns} + (0,55\text{ ns/pF}) C_L$
		10		40	80	ns	$29\text{ ns} + (0,23\text{ ns/pF}) C_L$	
		15		30	60	ns	$22\text{ ns} + (0,16\text{ ns/pF}) C_L$	
Output transition times	5	tTHL		60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$	
			HIGH to LOW	10	30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$
				15	20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$
	LOW to HIGH	5	tTLH		60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$
		10		30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$	
		15		20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$	

	V_{DD} V	typical formula for P (μW)	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
Dynamic power dissipation per package (P)	5	$4400 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	10	$18\ 000 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$43\ 300 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

APPLICATION INFORMATION

Some examples of applications for the HEF4556B are:

- Code conversion.
- Address decoding.
- Demultiplexing: when using the enable input as data input.

1-to-64 BIT VARIABLE LENGTH SHIFT REGISTER



The HEF4557B is a static clocked serial shift register whose length may be programmed to be any number of bits between 1 and 64. The number of bits selected is equal to the sum of the subscripts of the enabled length control inputs ($L_1, L_2, L_4, L_8, L_{16}$ and L_{32}) plus one. Serial data may be selected from the D_A or D_B data inputs with the A/\bar{B} select input. This feature is useful for recirculation purposes. Information on D_A or D_B is shifted into the first register position and all the data in the register is shifted one position to the right on the LOW to HIGH transition of CP_0 while \overline{CP}_1 is LOW or on the HIGH to LOW transition of \overline{CP}_1 while CP_0 is HIGH. A HIGH on master reset (MR) resets the register and forces O to LOW and \bar{O} to HIGH, independent of the other inputs.

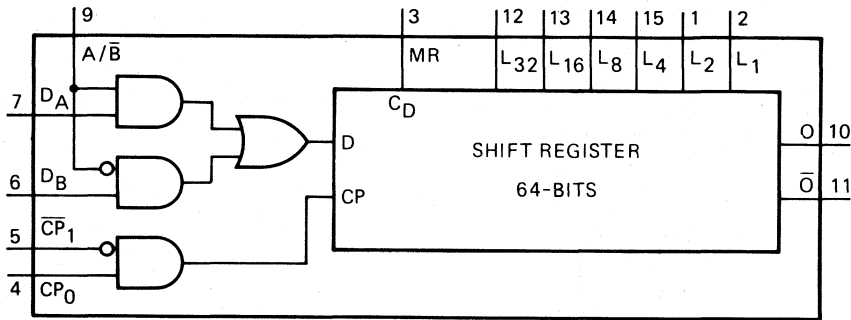


Fig. 1 Functional diagram.

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PINNING

- D_A, D_B data inputs
- A/\bar{B} select data input
- CP_0 clock input
- \overline{CP}_1 clock enable input
- MR asynchronous master reset
- L_1 to L_{32} bit-length control inputs
- O, \bar{O} buffered outputs

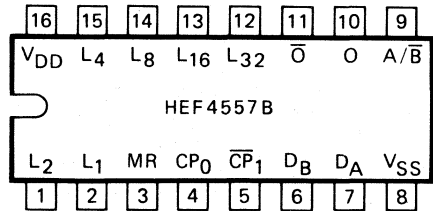


Fig. 2 Pinning diagram.

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- HEF4557BP: 16-lead DIL; plastic (SOT-38Z).
- HEF4557BD: 16-lead DIL; ceramic (SOT-74).
- HEF4557BT: 16-lead flat pack; plastic (SO-16; SOT-109A).

FAMILY DATA

I_{DD} LIMITS category LSI

} see Family Specifications

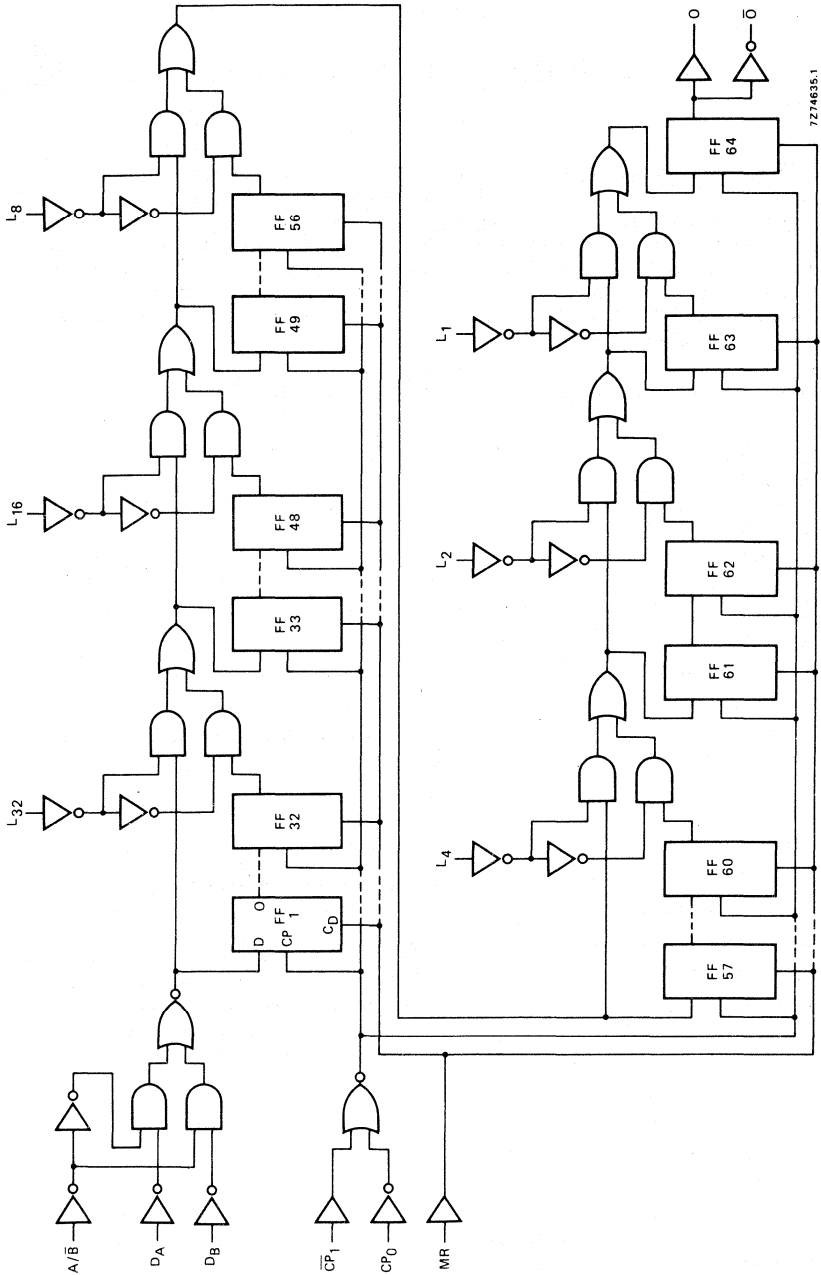


Fig. 3 Logic diagram.

FUNCTION TABLE

inputs						output
MR	A/ \bar{B}	D _A	D _B	CP ₀	$\overline{CP_1}$	O *
L	L	D ₁	D ₂	/	L	D ₂
L	H	D ₁	D ₂	/	L	D ₁
L	L	D ₁	D ₂	H	\	D ₂
L	H	D ₁	D ₂	H	\	D ₁
H	X	X	X	X	X	L

H = HIGH state (the more positive voltage)
 L = LOW state (the less positive voltage)
 X = state is immaterial
 / = positive-going transition
 \ = negative-going transition
 D_n = either HIGH or LOW

* The moment D_n appears at O depends on the bit-length shown in the table below.

BIT-LENGTH SELECT FUNCTION TABLE

L ₃₂	L ₁₆	L ₈	L ₄	L ₂	L ₁	register length
L	L	L	L	L	L	1-bit
L	L	L	L	L	H	2-bits
L	L	L	L	L	H	3-bits
L	L	L	L	H	H	4-bits
L	L	L	H	L	L	5-bits
L	L	L	H	L	H	6-bits
L	L	L	H	H	L	7-bits
L	L	L	H	H	H	8-bits
↓	↓	↓	↓	↓	↓	↓
L	H	H	H	H	H	32-bits
H	L	L	L	L	L	33-bits
H	L	L	L	L	H	34-bits
↓	↓	↓	↓	↓	↓	↓
H	H	H	H	L	L	61-bits
H	H	H	H	L	H	62-bits
H	H	H	H	H	L	63-bits
H	H	H	H	H	H	64-bits

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ≤ 20 ns

	V _{DD} V	typical formula for P (μW)	where f _i = input freq. (MHz) f _o = output freq. (MHz) C _L = load capacitance (pF) Σ(f _o C _L) = sum of outputs V _{DD} = supply voltage (V)
Dynamic power dissipation per package (P)	5	3 500 f _i + Σ(f _o C _L) × V _{DD} ²	
	10	15 000 f _i + Σ(f _o C _L) × V _{DD} ²	
	15	37 000 f _i + Σ(f _o C _L) × V _{DD} ²	

A.C. CHARACTERISTICS

$V_{SS} = 0$ V; $T_{amb} = 25$ °C; $C_L = 50$ pF; input transition times ≤ 20 ns

	V_{DD} V	symbol	typ.	max.		typical extrapolation formula
Propagation delays $CP_0, CP_1 \rightarrow O, \bar{O}$ HIGH to LOW	5		240	480	ns	$213 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
	10	t_{PHL}	90	180	ns	$79 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
	15		65	130	ns	$57 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
LOW to HIGH	5		240	480	ns	$213 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
	10	t_{PLH}	90	180	ns	$79 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
	15		65	130	ns	$57 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
MR \rightarrow O HIGH to LOW	5		170	340	ns	$243 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
	10	t_{PHL}	80	160	ns	$69 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
	15		60	120	ns	$52 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
MR \rightarrow \bar{O} LOW to HIGH	5		140	280	ns	$113 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
	10	t_{PLH}	70	140	ns	$59 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
	15		55	110	ns	$47 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
Output transition times HIGH to LOW	5		60	120	ns	$10 \text{ ns} + (1,0 \text{ ns/pF}) C_L$
	10	t_{THL}	30	60	ns	$9 \text{ ns} + (0,42 \text{ ns/pF}) C_L$
	15		20	40	ns	$6 \text{ ns} + (0,28 \text{ ns/pF}) C_L$
LOW to HIGH	5		60	120	ns	$10 \text{ ns} + (1,0 \text{ ns/pF}) C_L$
	10	t_{TLH}	30	60	ns	$9 \text{ ns} + (0,42 \text{ ns/pF}) C_L$
	15		20	40	ns	$6 \text{ ns} + (0,28 \text{ ns/pF}) C_L$

Interpolation table (see note next page)

length control inputs						minimum number of bits selected	set-up, hold, recovery times
L_1	L_2	L_4	L_8	L_{16}	L_{32}		
L	L	L	L	L	L	1	specified
H	L	L	L	L	L	2	
X	H	L	L	L	L	3	
X	X	H	L	L	L	5	six equal steps
X	X	X	H	L	L	9	
X	X	X	X	H	L	17	
X	X	X	X	X	H	33	specified

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

X = state is immaterial

A.C. CHARACTERISTICS

 $V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$; see also waveforms Fig. 4

	V_{DD} V	symbol	min.	typ.		
Minimum clock pulse width; LOW for $\overline{CP_0}$ or HIGH for $\overline{CP_1}$	5	t_{WCPL}	180	90	ns	
	10	or	60	30	ns	
	15	t_{WCPH}	40	20	ns	
Minimum reset pulse width; HIGH	5	t_{WMRH}	150	75	ns	
	10		70	35	ns	
	15		50	25	ns	
Set-up times $D_A, D_B, A/\overline{B} \rightarrow CP_0,$ $\overline{CP_1}$ L_1 to $L_{32} = \text{LOW}$	5	t_{su}	360	180	ns	
	10		140	70	ns	
	15		90	45	ns	
	$L_{32} = \text{HIGH}$	5	t_{su}	40	-20	ns
		10		35	-10	ns
		15		30	-5	ns
Hold times $D_A, D_B, A/\overline{B} \rightarrow CP_0,$ $\overline{CP_1}$ L_1 to $L_{32} = \text{LOW}$	5	t_{hold}	-40	-110	ns	
	10		-10	-45	ns	
	15		0	-30	ns	
	$L_{32} = \text{HIGH}$	5	t_{hold}	90	30	ns
		10		60	20	ns
		15		50	15	ns
Recovery times for MR L_1 to $L_{32} = \text{LOW}$	5	t_{RMR}	500	250	ns	
	10		250	125	ns	
	15		150	75	ns	
	$L_{32} = \text{HIGH}$	5	t_{RMR}	110	50	ns
		10		70	30	ns
		15		60	25	ns
Minimum clock pulse frequency	5	f_{max}	2,5	5	MHz	
	10		7	14	MHz	
	15		10	20	MHz	

see note

Note

The set-up, hold and recovery times vary with the minimum number of bits selected. For other values as specified one may interpolate as shown in the table (see previous page).

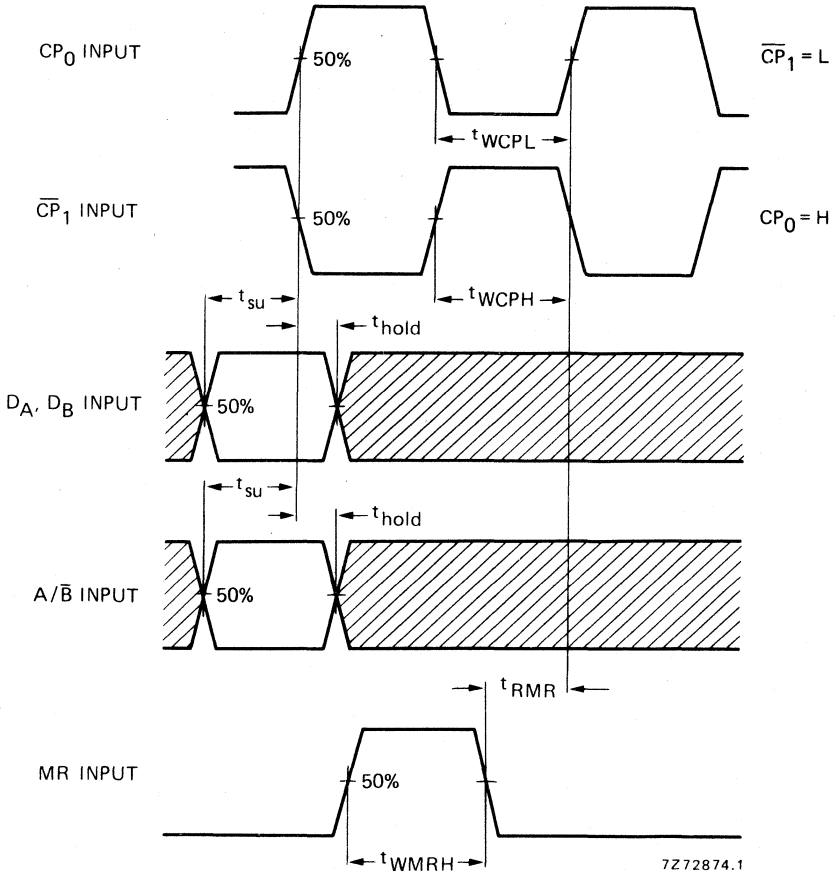


Fig. 4 Waveforms showing recovery time for MR and minimum CP₀, \overline{CP}_1 and MR pulse widths, set-up and hold times for D_A, D_B and A/ \overline{B} to CP₀ and \overline{CP}_1 . Set-up and hold times are shown as positive values but may be specified as negative values.



4-BIT MAGNITUDE COMPARATOR

The HEF4585B is a 4-bit magnitude comparator which compares two 4-bit words (A and B), whether they are 'less than', 'equal to', or 'greater than'. Each word has four parallel inputs (A_0 to A_3 and B_0 to B_3); A_3 and B_3 being the most significant inputs. Three outputs are provided; A greater than B ($O_{A > B}$), A less than B ($O_{A < B}$) and A equal to B ($O_{A = B}$). Three expander inputs ($I_{A > B}$, $I_{A < B}$ and $I_{A = B}$) allow cascading of the devices without external gates.

For proper compare operation the expander inputs to the least significant position must be connected as follows: $I_{A = B} = I_{A > B} = \text{HIGH}$, $I_{A < B} = \text{LOW}$. For words greater than 4-bits, units can be cascaded by connecting outputs $O_{A < B}$ and $O_{A = B}$ to the corresponding inputs of the next significant comparator (input $I_{A > B}$ is connected to a HIGH).

Operation is not restricted to binary codes, the devices will work with any monotonic code. The function table describes the operation of the device under all possible logic conditions.

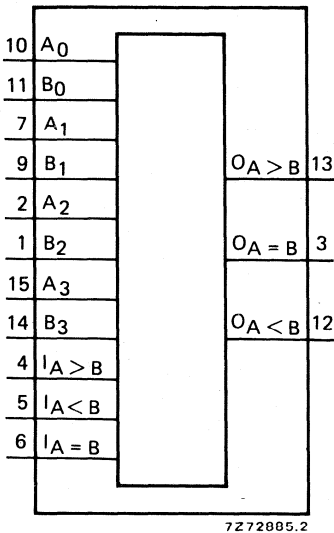


Fig. 1 Functional diagram.

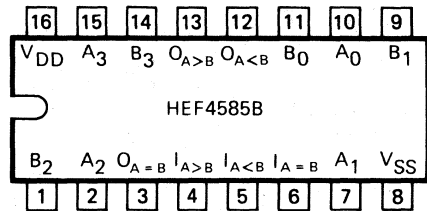


Fig. 2 Pinning diagram.

HEF4585BP: 16-lead DIL; plastic (SOT-38Z).
HEF4585BD: 16-lead DIL; ceramic (SOT-74).
HEF4585BT: 16-lead flat-pack; plastic (SO-16; SOT-109A).

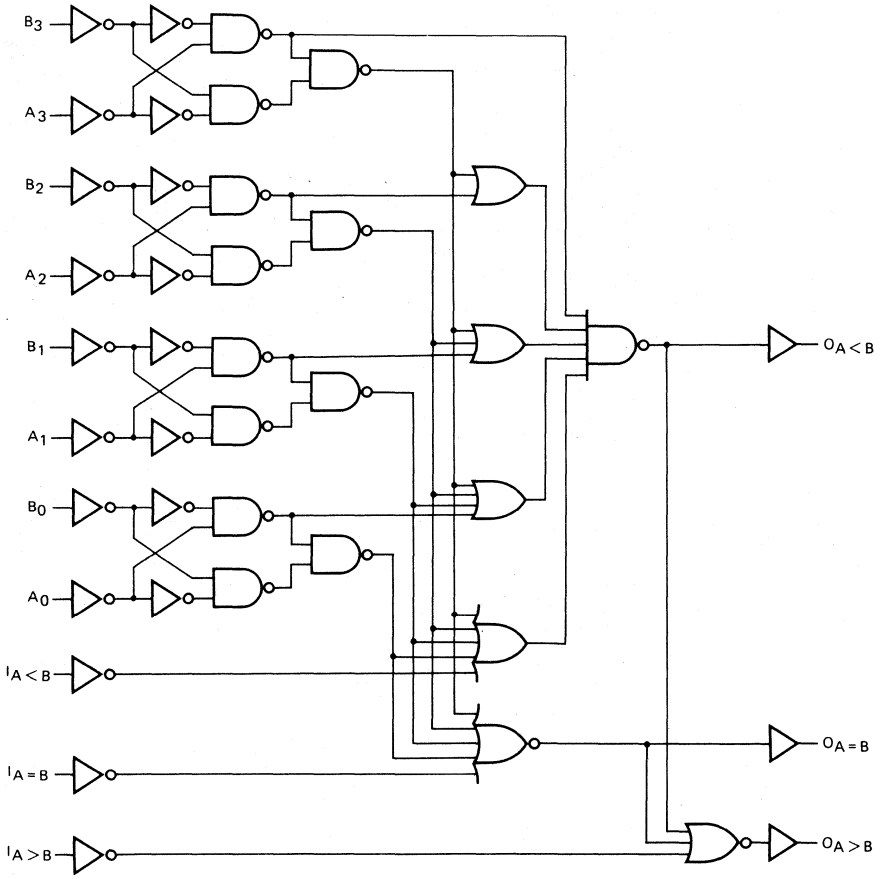
PINNING

A_0 to A_3 word A parallel inputs
 B_0 to B_3 word B parallel inputs
 $I_{A > B}$, $I_{A < B}$, $I_{A = B}$ expander inputs
 $O_{A > B}$ A greater than B output
 $O_{A < B}$ A less than B output
 $O_{A = B}$ A equal to B output

FAMILY DATA

I_{DD} LIMITS category MSI

} see Family Specifications



7274596.1

Fig. 3 Logic diagram.

FUNCTION TABLE

comparing inputs				cascading inputs			outputs		
A ₃ , B ₃	A ₂ , B ₂	A ₁ , B ₁	A ₀ , B ₀	I _{A > B}	I _{A < B}	I _{A = B}	O _{A > B}	O _{A < B}	O _{A = B}
A ₃ > B ₃	X	X	X	H	X	X	H	L	L
A ₃ < B ₃	X	X	X	X	X	X	L	H	L
A ₃ = B ₃	A ₂ > B ₂	X	X	H	X	X	H	L	L
A ₃ = B ₃	A ₂ < B ₂	X	X	X	X	X	L	H	L
A ₃ = B ₃	A ₂ = B ₂	A ₁ > B ₁	X	H	X	X	H	L	L
A ₃ = B ₃	A ₂ = B ₂	A ₁ < B ₁	X	X	X	X	L	H	L
A ₃ = B ₃	A ₂ = B ₂	A ₁ = B ₁	A ₀ > B ₀	H	X	X	H	L	L
A ₃ = B ₃	A ₂ = B ₂	A ₁ = B ₁	A ₀ < B ₀	X	X	X	L	H	L
A ₃ = B ₃	A ₂ = B ₂	A ₁ = B ₁	A ₀ = B ₀	X	L	H	L	L	H
A ₃ = B ₃	A ₂ = B ₂	A ₁ = B ₁	A ₀ = B ₀	H	L	L	H	L	L
A ₃ = B ₃	A ₂ = B ₂	A ₁ = B ₁	A ₀ = B ₀	X	H	L	L	H	L
A ₃ = B ₃	A ₂ = B ₂	A ₁ = B ₁	A ₀ = B ₀	X	H	H	L	H	H
A ₃ = B ₃	A ₂ = B ₂	A ₁ = B ₁	A ₀ = B ₀	L	L	L	L	L	L

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

X = state is immaterial

The upper 11 lines describe the normal operation under all conditions that will occur in a single device or in a serial expansion scheme.

The lower 2 lines describe the operation under abnormal conditions on the cascading inputs. These conditions occur when the parallel expansion technique is used.

A.C. CHARACTERISTICS

 $V_{SS} = 0 \text{ V}$; $T_{amb} = 25 \text{ }^\circ\text{C}$; $C_L = 50 \text{ pF}$; input transition times $\leq 20 \text{ ns}$

	V_{DD} V	symbol	min.	typ.	max.	typical extrapolation formula
Propagation delays $A_n, B_n \rightarrow O_n$ HIGH to LOW	5	tPHL		160	320 ns	$133 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
	10		65	130 ns	$54 \text{ ns} + (0,23 \text{ ns/pF}) C_L$	
	15		45	90 ns	$37 \text{ ns} + (0,16 \text{ ns/pF}) C_L$	
LOW to HIGH	5	tPLH		150	300 ns	$123 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
	10		60	120 ns	$49 \text{ ns} + (0,23 \text{ ns/pF}) C_L$	
	15		45	90 ns	$37 \text{ ns} + (0,16 \text{ ns/pF}) C_L$	
$I_n \rightarrow O_n$ HIGH to LOW	5	tPHL		110	220 ns	$83 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
	10		45	90 ns	$34 \text{ ns} + (0,23 \text{ ns/pF}) C_L$	
	15		30	60 ns	$22 \text{ ns} + (0,16 \text{ ns/pF}) C_L$	
LOW to HIGH	5	tPLH		120	240 ns	$93 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
	10		50	100 ns	$39 \text{ ns} + (0,23 \text{ ns/pF}) C_L$	
	15		35	70 ns	$27 \text{ ns} + (0,16 \text{ ns/pF}) C_L$	
Output transition times HIGH to LOW	5	tTHL		60	120 ns	$10 \text{ ns} + (1,0 \text{ ns/pF}) C_L$
	10		30	60 ns	$9 \text{ ns} + (0,42 \text{ ns/pF}) C_L$	
	15		20	40 ns	$6 \text{ ns} + (0,28 \text{ ns/pF}) C_L$	
LOW to HIGH	5	tTLH		60	120 ns	$10 \text{ ns} + (1,0 \text{ ns/pF}) C_L$
	10		30	60 ns	$9 \text{ ns} + (0,42 \text{ ns/pF}) C_L$	
	15		20	40 ns	$6 \text{ ns} + (0,28 \text{ ns/pF}) C_L$	

	V_{DD} V	typical formula for P (μW)	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
Dynamic power dissipation per package (P)	5	$1250 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	10	$5500 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$15000 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

APPLICATION INFORMATION

Some examples of applications for the HEF4585B are:

- Process controllers.
- Servo-motor control.

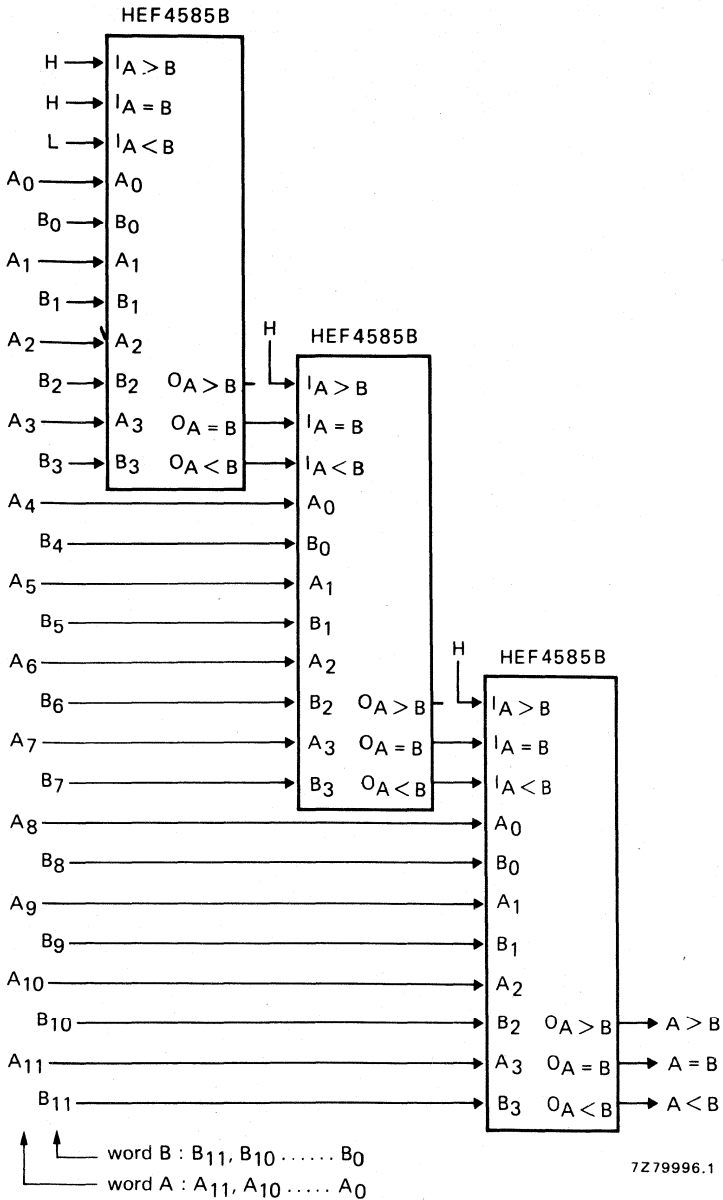


Fig. 4 Example of cascading comparators.

256-BIT, 1-BIT PER WORD RANDOM ACCESS MEMORIES



The HEF4720B and HEF4720V are 256-bit, 1-bit per word random access memories with 3-state outputs. The memories are fully decoded and completely static.

Recommended supply voltage range for HEF4720B is 3 to 15 V and for HEF4720V is 4,5 to 12,5 V; minimum stand-by voltage for both types is 3 V.

The use of LOC MOS gives the added advantage of very low stand-by power. The circuits can be directly interfaced with standard bipolar devices (TTL) without using special interface circuits. The memory operates from a single power supply. The separate chip select input (\overline{CS}) allows simple memory expansion when the outputs are wire-ORed. If \overline{CS} is HIGH, the outputs are floating and no new information can be written into the memory. The signal at \overline{O} has the same polarity as the data input D, while the signal at O is the complement of the signal at \overline{O} . The write control W must be HIGH for writing into the memory.

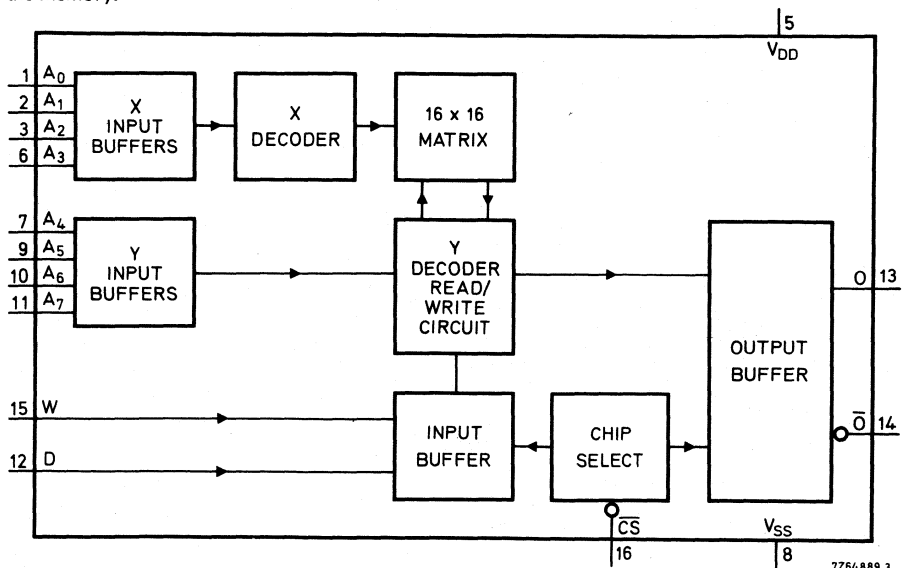


Fig. 1 Block diagram.

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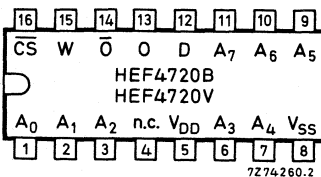


Fig. 2 Pinning diagram.

7274260.2

HEF4720BP; HEF4720VP: 16-lead DIL; plastic (SOT-38Z).

HEF4720BD; HEF4720VD: 16-lead DIL; ceramic (SOT-74).

FAMILY DATA: see Family Specifications.

I_{DD} LIMITS: see next page.

FUNCTION TABLE

\overline{CS}	W	O	\overline{O}	mode
L	H	data written into memory	complement of data written into memory	write
L	L	data written into memory	complement of data written into memory	read
H	X	Z	Z	inhibit

H = HIGH state (the more positive voltage) X = state is immaterial
L = LOW state (the less positive voltage) Z = high impedance OFF-state

PINNING

\overline{CS} chip select input (active LOW)
W write enable input
D data input
A₀ to A₇ address inputs
O 3-state output (active HIGH)
 \overline{O} 3-state output (active LOW)

SUPPLY VOLTAGE

	rating	recommended operating	stand-by min.
HEF4720B	-0,5 to 18	3,0 to 15,0	3 V
HEF4720V	-0,5 to 18	4,5 to 12,5	3 V

The values given at V_{DD} = 15 V in the following d.c. and a.c. characteristics, are not applicable to the HEF4720V, because of its lower supply voltage range.

D.C. CHARACTERISTICS

V_{SS} = 0 V

	V _{DD} V	V _{OL} V	symbol	T _{amb} (°C)					
				-40		+25		+85	
				min.	max.	min.	max.	min.	max.
Output current LOW	4,75	0,4	I _{OL}	2,4		2		1,6	mA
	10	0,5		4,8		4		3,2	mA
	15	1,5		10,0		10		7,5	mA
Quiescent device current	5		I _{DD}		25		25		200 μA
	10				50		50		400 μA
	15				100		100		800 μA
Input leakage current HEF4720V HEF4720B	10		±I _{IN}		0,3		0,3		1 μA
	15				0,3		0,3		1 μA

A.C. CHARACTERISTICS

	V _{DD} V	symbol	min.	typ.	max.	
Output capacitance	5	C _O		5	pF	
	10		5	pF		
	15		5	pF		

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V _{DD} V	symbol	min.	typ.	max.	typical extrapolation formula	
Read cycle							
Read access time	5	t _{ACC}		320	580	ns	292 ns + (0,55 ns/pF) C _L
	10		130	220	ns	118 ns + (0,23 ns/pF) C _L	
	15		100	160	ns	92 ns + (0,16 ns/pF) C _L	
Chip select to output time	5	t _{CO}			180	ns	
	10				70	ns	
	15				50	ns	
Address hold time	5	t _{OA}	0			ns	
	10		0			ns	
	15		0			ns	
Output hold time with respect to address input	5	t _{VAL1}	60	170		ns	142 ns + (0,55 ns/pF) C _L
	10		20	50		ns	38 ns + (0,23 ns/pF) C _L
	15		15	40		ns	32 ns + (0,16 ns/pF) C _L
Output hold time with respect to chip select input	5	t _{COH}			130	ns	
	10				70	ns	
	15				60	ns	
Output floating time with respect to chip select input	5	t _{COF}	0			ns	
	10		0			ns	
	15		0			ns	
Read cycle time	5	t _{RC}	580			ns	
	10		220			ns	
	15		160			ns	
Output transition times LOW to HIGH	5	t _{TLH}		60	120	ns	10 ns + (1,0 ns/pF) C _L
	10			30	60	ns	9 ns + (0,42 ns/pF) C _L
	15			20	40	ns	6 ns + (0,28 ns/pF) C _L
HIGH to LOW	5	t _{THL}		40	80	ns	14 ns + (0,52 ns/pF) C _L
	10			22	40	ns	11 ns + (0,22 ns/pF) C _L
	15			15	30	ns	7 ns + (0,16 ns/pF) C _L

A.C. CHARACTERISTICS

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	symbol	min.	typ.	max.
Write cycle					
Write cycle time	5	t_{WC}	580		ns
	10		220		ns
	15		160		ns
Address to write set-up time	5	t_{AW}	110		ns
	10		50		ns
	15		50		ns
Write pulse width	5	t_{WP}	370	10 000	ns
	10		130	10 000	ns
	15		80	10 000	ns
Write recovery time	5	t_{WR}	100		ns
	10		40		ns
	15		30		ns
Data set-up time	5	t_{DW}	250		ns
	10		100		ns
	15		80		ns
Data hold time	5	t_{DH}	100		ns
	10		30		ns
	15		20		ns
Chip select set-up time with respect to write pulse	5	t_{CSW}	370		ns
	10		130		ns
	15		80		ns
Chip select hold time with respect to write pulse	5	t_{CSH}	0		ns
	10		0		ns
	15		0		ns
Chip select lead time over write pulse to prevent writing	5	t_{CSL}	0		ns
	10		0		ns
	15		0		ns
Read-modify-write cycle					
Read enable hold time	5	t_{RH}	0		ns
	10		0		ns
	15		0		ns
Output hold time with respect to write pulse	5	t_{VAL2}	60		ns
	10		20		ns
	15		15		ns
Read-modify-write cycle time	5	t_{RWC}	1050		ns
	10		390		ns
	15		270		ns

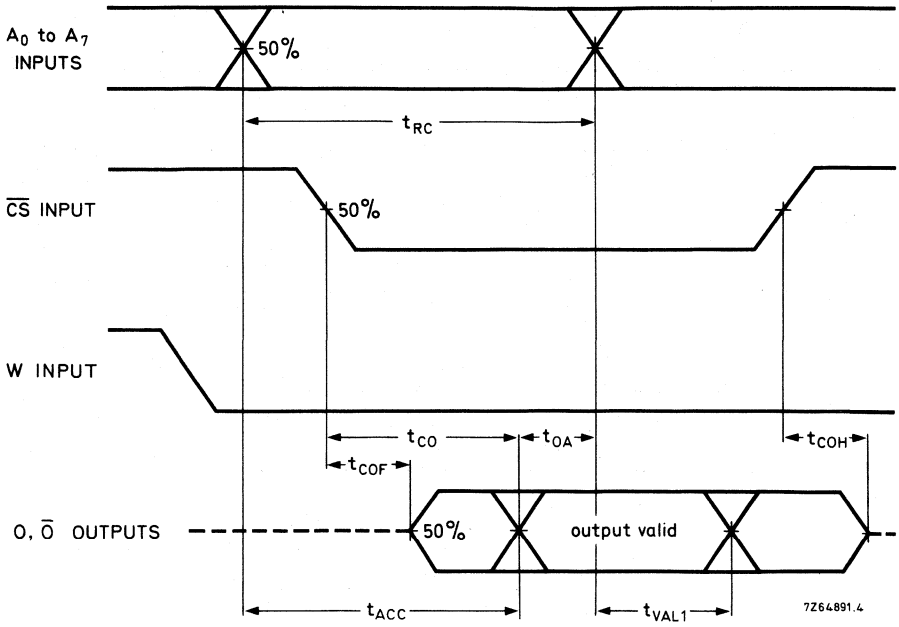


Fig. 3 Read cycle timing diagram.

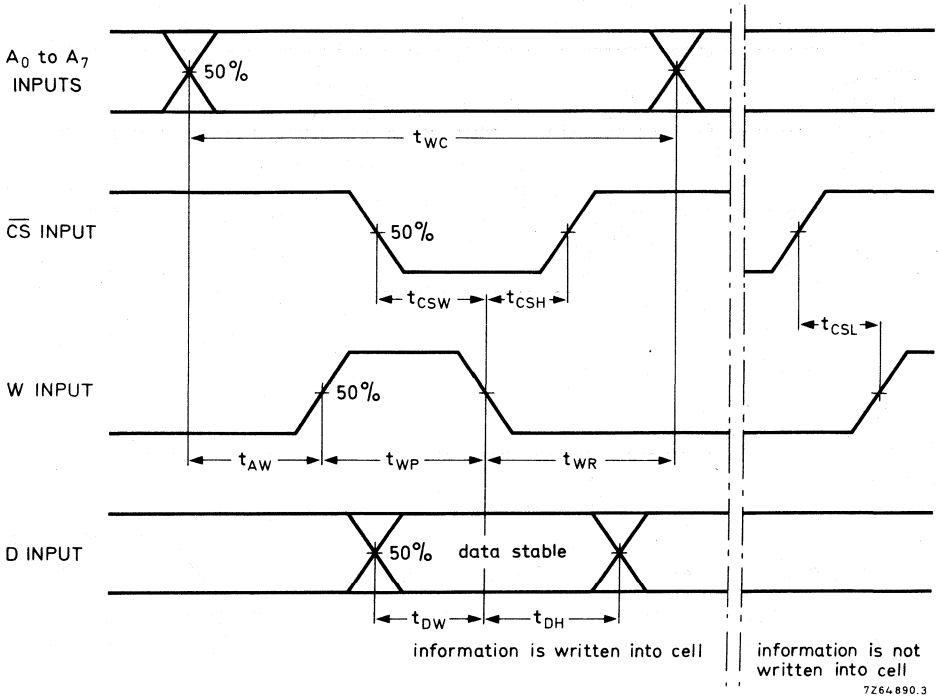


Fig. 4 Write cycle timing diagram.

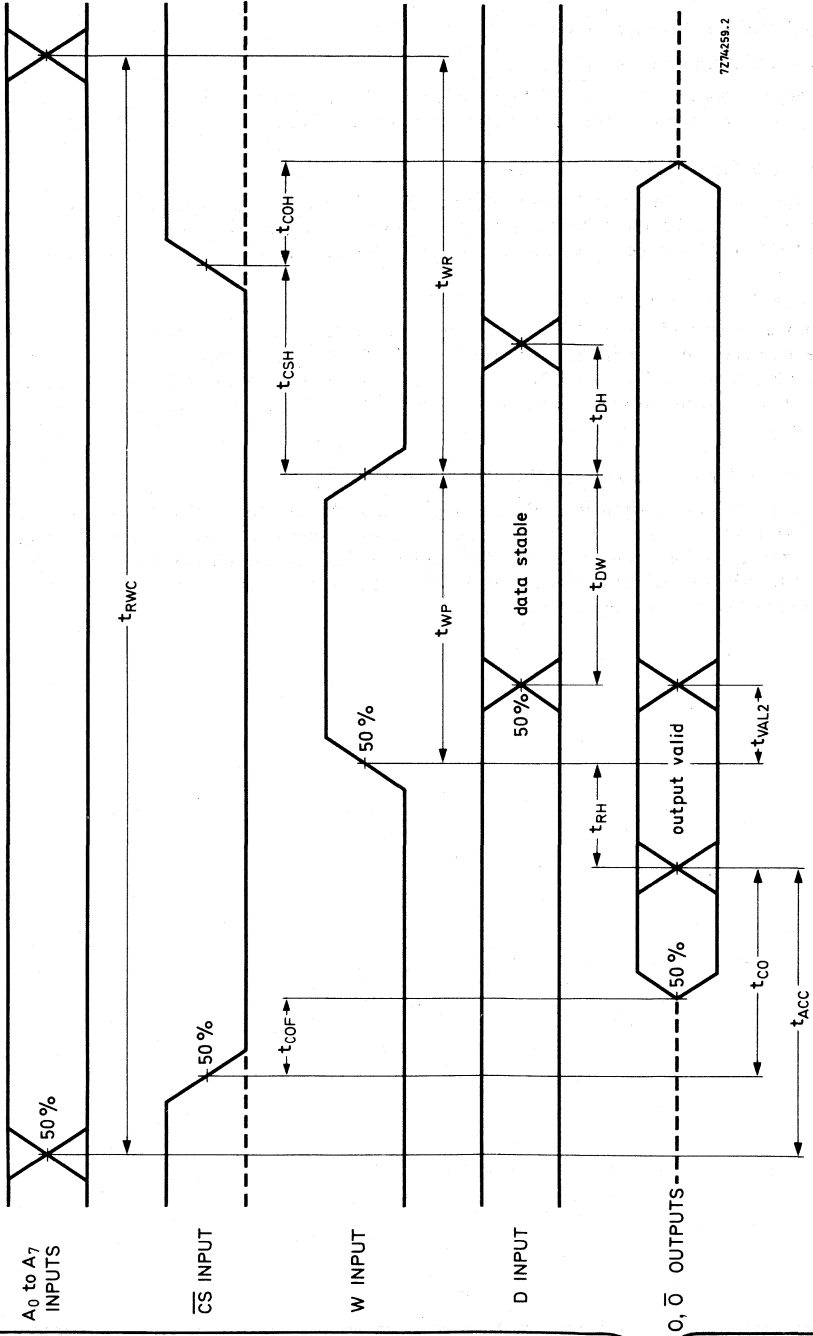


Fig. 5 Read-modify-write cycle timing diagram.

APPLICATION INFORMATION

Extension of memory capacity

The memory capacity of the HEF4720B; V is 256 bits (or 256 words of 1 bit). The capacity of a system can be extended in various ways by the connection of further HEF4720B; V ICs.

Extending the word length

By connecting a number of HEF4720B; V ICs as shown in Fig. 6, the word length (i.e. bits per word) is multiplied by that number. That is, each device stores 1 bit per word but the total number of words remains 256. For example, if four devices are used in this way, 256 four-binary-bit words can be stored.

Extending the number of words

If a number of HEF4720B; V ICs are connected as shown in Fig. 7, the words available are multiplied by that number, but the word length remains 1 bit. Notice that in this case additional addresses are used in conjunction with the \overline{CS} input. In the case shown in Fig. 7 (4 x HEF4720B; V in parallel), the addresses and data inputs are loaded with four inputs (= 20 pF), the \overline{CS} inputs are loaded with one input each.

Extending both the word length and number of words

Figure 8 shows how a combination of the extensions described above can be used to obtain both greater word length and additional words. It is clear that the capacitive load of the driving circuits puts a limit to the free choice of the interface. In Fig. 8, each address is loaded with 16 inputs, i.e. $16 \times 5 = 80$ pF: each \overline{CS} inverter is loaded with 8 inputs, i.e. $8 \times 5 = 40$ pF. The data inverters in this case are loaded with only two inputs each.

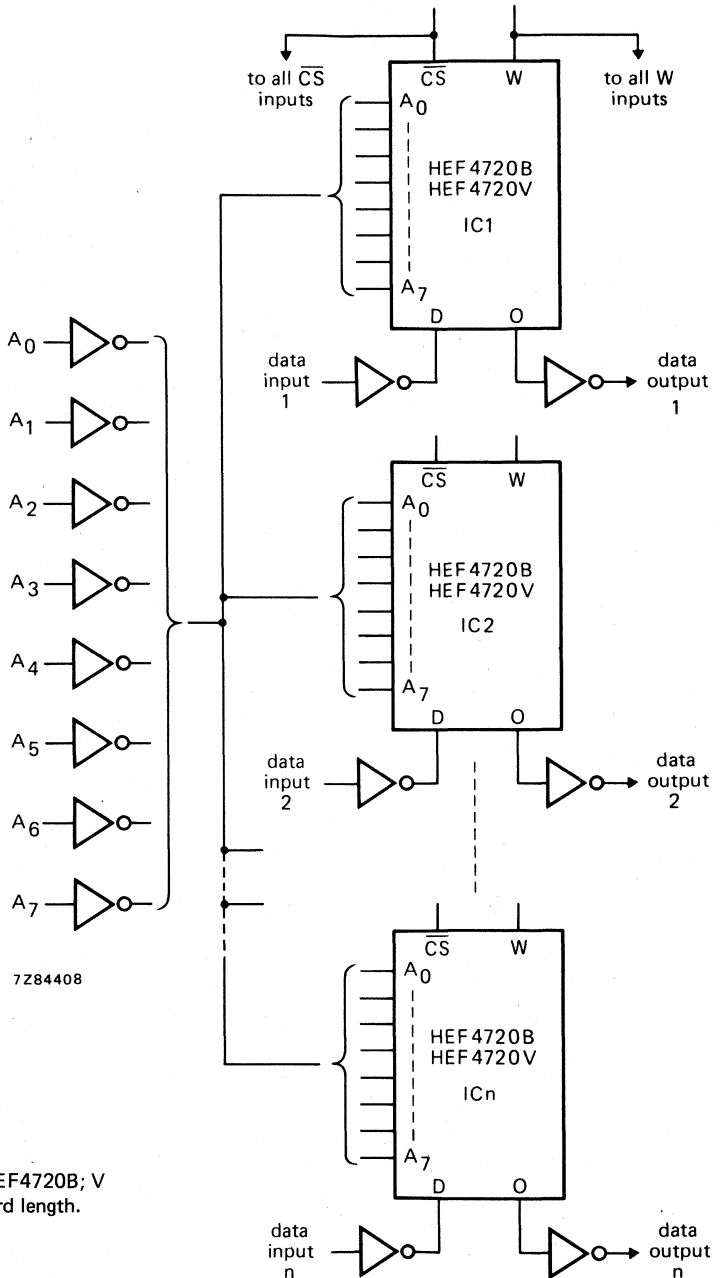


Fig. 6 Using extra HEF4720B; V ICs to extend the word length.

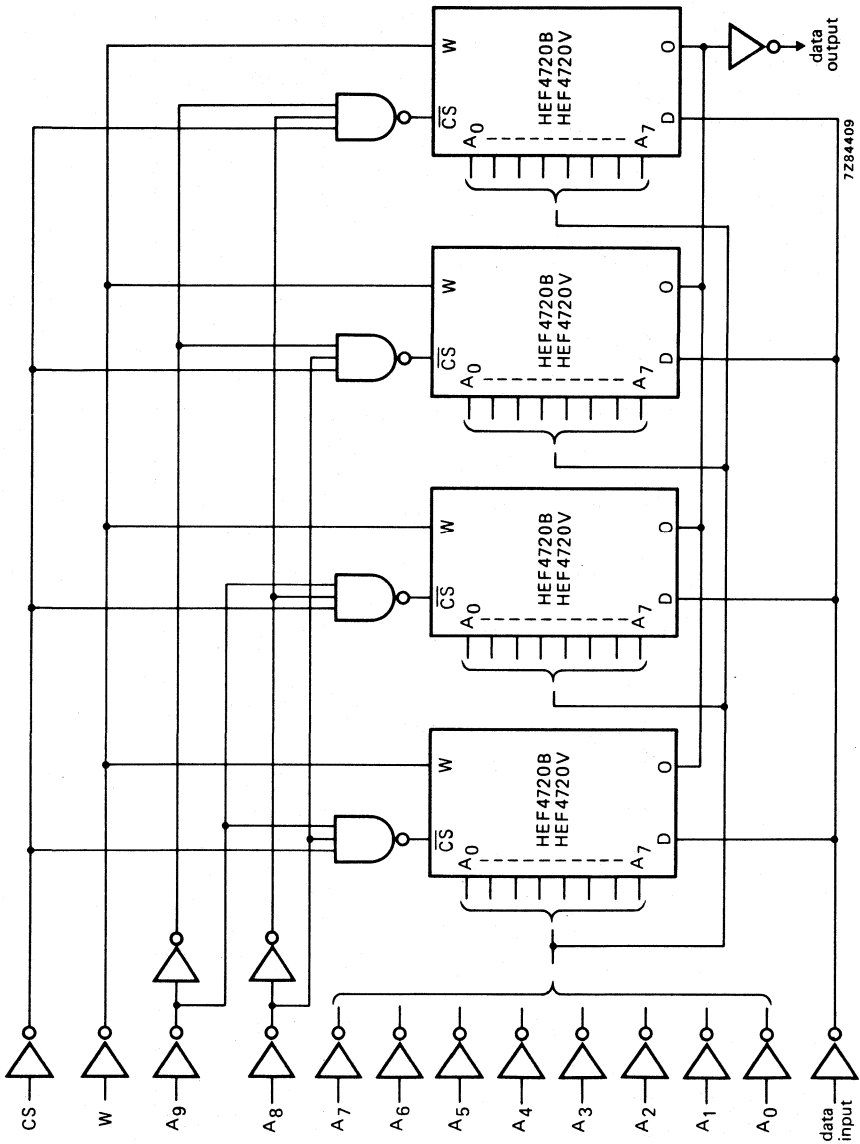
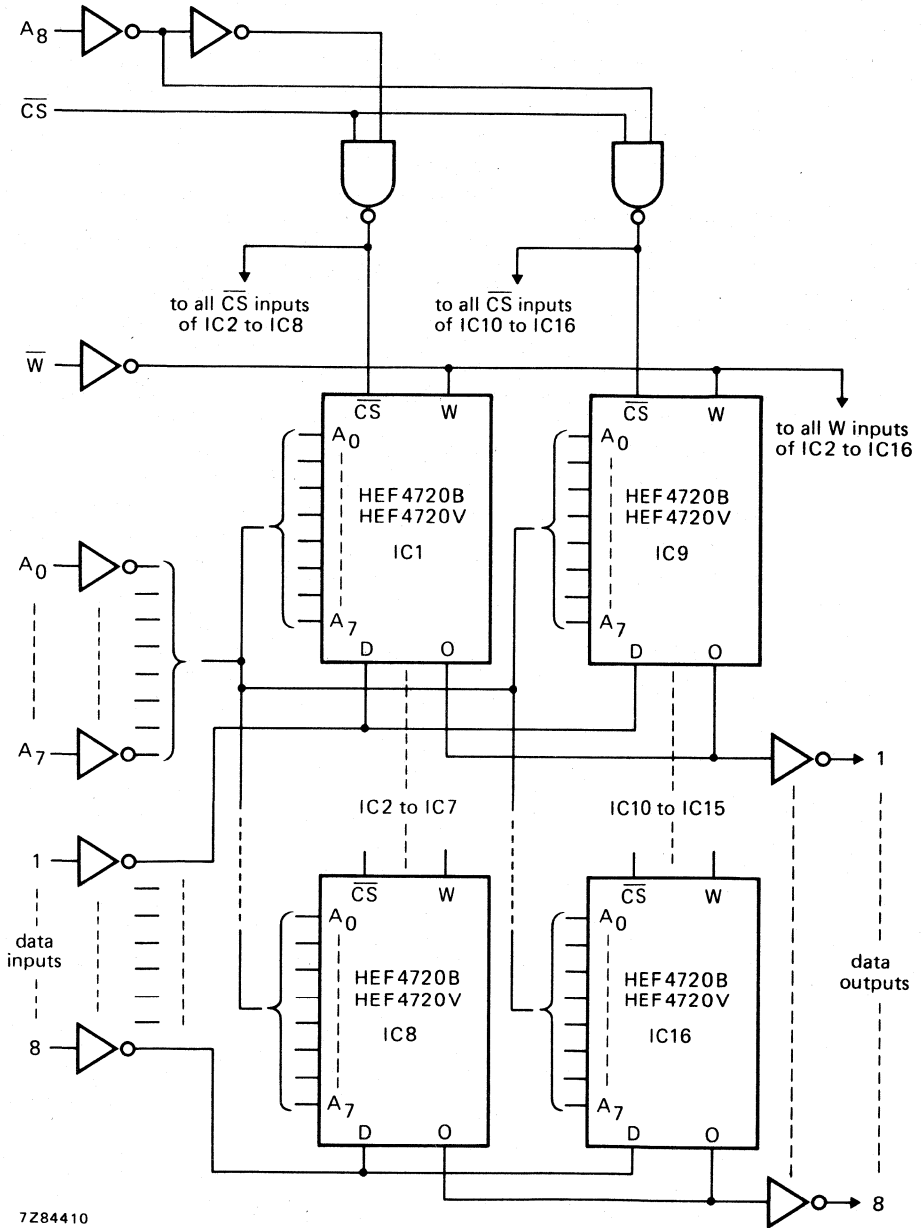


Fig. 7 Using extra HEF4720B; V ICs to obtain more words.



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Fig. 8 Using extra HEF4720B; V ICs to obtain more words and greater word length.

APPLICATION INFORMATION (continued)

Memory retention

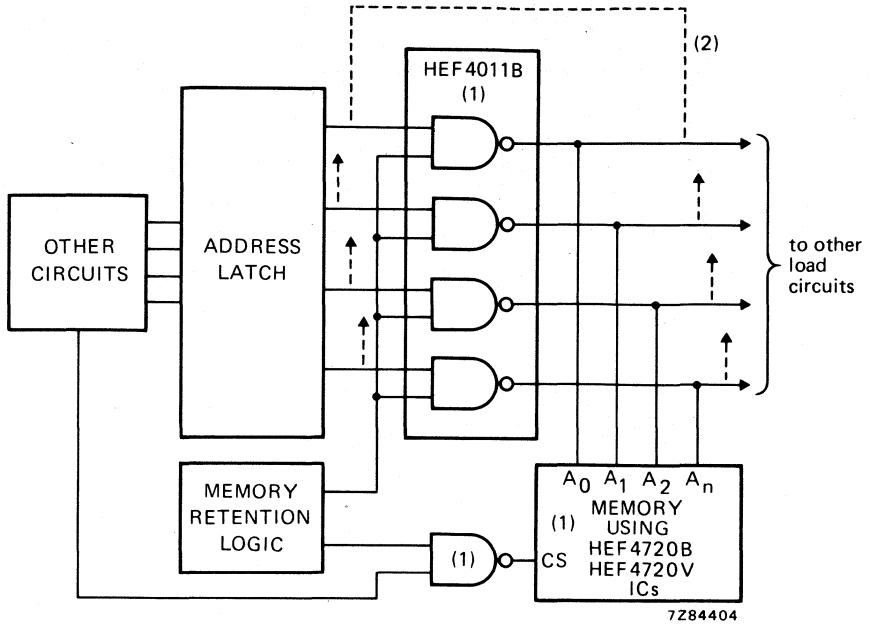
It is sometimes necessary to ensure that the information stored in the memory cannot be erased inadvertently. This can be arranged by adding detection circuits, by measures in the timing, and by the addition of a battery. With the HEF4720B; V, memory retention is very easily obtained because its current drain in the stand-by condition is almost zero. The wide supply voltage range makes it possible to keep the memory active by means of a simple battery, thereby preventing information loss.

In designing the memory retention circuits, two aspects should be kept in mind. The memory retention will not function in an optimum way if the battery voltage is low or if the voltage transitions at the address input are too slow. The first of these is usually the result of using too simple a battery back-up circuit, e.g. a battery charged via a diode from the TTL supply voltage. In this case, the LOCMOS supply voltage falls below the safe operating voltage. Special arrangements should be made to overcome this.

Slow address transitions (the second cause of memory loss) are due to a long RC-time in the power system. When the power is switched on or off, the 5 V line changes between 0 and 5 V in milliseconds to seconds so producing a correspondingly long transition time in the various logic outputs. This creates problems in the proper operation of the HEF4720B; V, with loss of memory as a possible result. This can be prevented by ensuring that input rise and fall times do not exceed 10 μ s.

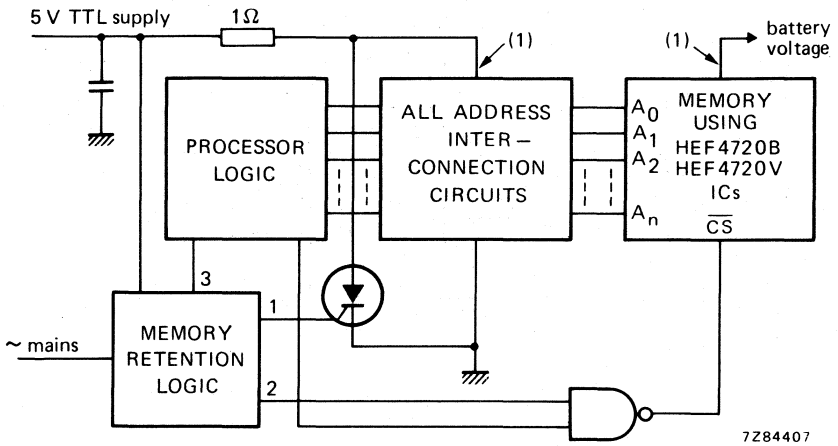
Three possibilities for controlling the rise and fall times at the HEF4720B; V interface are given here:

1. LOCMOS gates can be connected between the address latch and the HEF4720B; V (Fig. 9). In the event of a low voltage, or mains supply failure, the gates can be blocked by a signal from the memory retention logic thus isolating the HEF4720B; V from the address and \overline{CS} inputs.
2. The interface power supply can be separated from the TTL power supply by means of a low-value resistor (Fig. 10); a thyristor is connected from the interface power supply to earth. The system is arranged so that, upon switching off or failure of the interface supply, the thyristor turns on thus ensuring a rapid fall of the supply voltage.
3. The best solution is to select the interface circuits from the LOCMOS family and to feed all these circuits from the battery (Fig. 11). These stages then remain active when the TTL 5 V supply fails. The interface circuits are mostly only active on a clock pulse, have the possibility of being inactive on a gate level, or can be forced into one position.

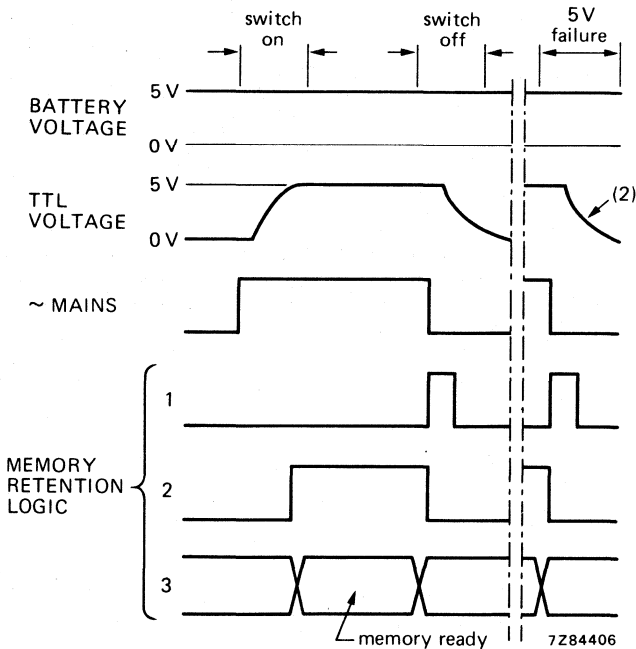


- (1) These devices have a battery supply.
- (2) Alternative connection.

Fig. 9 Use of battery-operated LCMOS gates to isolate the memory in case of power supply failure. Devices marked (1) are connected to the battery. The HEF4011B can sink about 0,7 mA: if the load is greater than this, only the memory should be connected, other loads being connected to the address latch as shown by the dashed-line connections.



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(1) Leads should be so arranged to prevent cross-talk; thyristor connections must be short.

(2) Slope $> 500 \text{ mV}/\mu\text{s}$ in the vicinity of the threshold.

Fig. 10 Using a thyristor to ensure a rapid fall of interface supply at switch-off or supply failure.

8-BIT ADDRESSABLE LATCH



The HEF4724B is an 8-bit addressable latch with three address inputs (A_0 to A_2), a data input (D), an active LOW enable input (\bar{E}), an active HIGH clear input (CL), and eight parallel latch outputs (O_0 to O_7).

When \bar{E} and CL are HIGH, all outputs (O_0 to O_7) are LOW. Eight-channel demultiplexing or active HIGH 1-of-8 decoding with output enable operation occurs when CL is HIGH and \bar{E} is LOW. When CL and \bar{E} are LOW, the selected output (O_0 to O_7 ; determined by A_0 to A_2) follows D . When \bar{E} goes HIGH, the contents of the latch are stored. When operating in the addressable latch mode ($\bar{E} = CL = LOW$), changing more than one bit of A_0 to A_2 could impose a transient wrong address. Therefore, this should only be done while in the memory mode ($\bar{E} = HIGH, CL = LOW$).

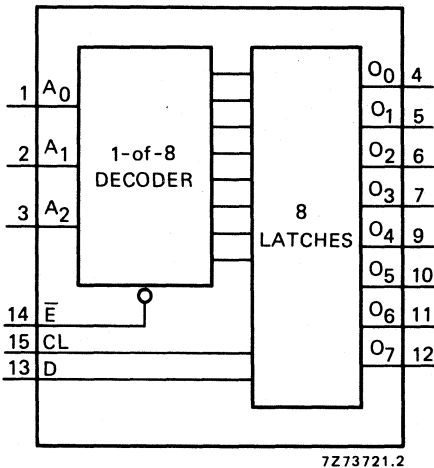


Fig. 1 Functional diagram.

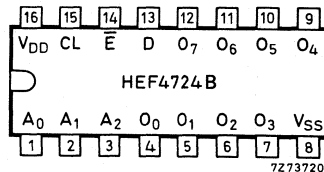


Fig. 2 Pinning diagram.

HEF4724BP : 16-lead DIL; plastic (SOT-38Z).

HEF4724BD : 16-lead DIL; ceramic (SOT-74).

HEF4724BT : 16-lead flat pack;
plastic (SO-16; SOT-109A).

PINNING

A_0 to A_2	address inputs
D	data input
\bar{E}	enable input (active LOW)
CL	clear input (active HIGH)
O_0 to O_7	parallel latch outputs

FAMILY DATA

see Family Specifications

I_{DD} LIMITS category MSI

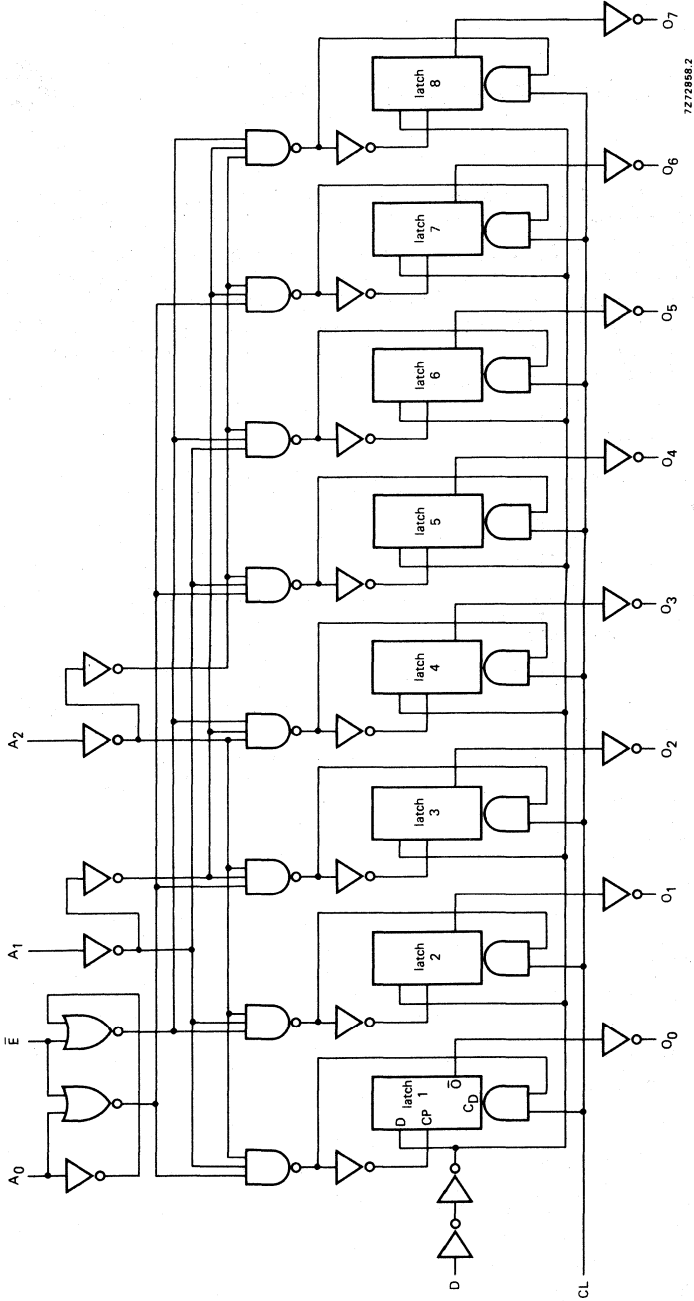


Fig. 3 Logic diagram.

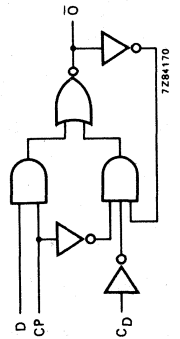


Fig. 4 Logic diagram (one latch).

MODE SELECTION

\bar{E}	CL	mode
L	L	addressable latch
H	L	memory
L	H	active HIGH 8-channel demultiplexer
H	H	clear

FUNCTION TABLE

CL	\bar{E}	D	A ₀	A ₁	A ₂	O ₀	O ₁	O ₂	O ₃	O ₄	O ₅	O ₆	O ₇	mode
H	H	X	X	X	X	L	L	L	L	L	L	L	L	clear
H	L	D ₁	L	L	L	D ₁	L	L	L	L	L	L	L	demultiplexer; unaddressed latch is cleared
H	L	D ₁	H	L	L	L	D ₁	L	L	L	L	L	L	
H	L	D ₁	L	H	L	L	L	D ₁	L	L	L	L	L	
H	L	D ₁	H	H	L	L	L	L	D ₁	L	L	L	L	
H	L	D ₁	L	L	H	L	L	L	L	D ₁	L	L	L	
H	L	D ₁	H	L	H	L	L	L	L	L	D ₁	L	L	
H	L	D ₁	L	H	H	L	L	L	L	L	L	D ₁	L	
H	L	D ₁	H	H	H	L	L	L	L	L	L	L	D ₁	
L	H	X	X	X	X	O _{n-1}	O _{n-1}	O _{n-1}	O _{n-1}	O _{n-1}	O _{n-1}	O _{n-1}	O _{n-1}	memory
L	L	D ₁	L	L	L	D ₁	O _{n-1}	O _{n-1}	O _{n-1}	O _{n-1}	O _{n-1}	O _{n-1}	O _{n-1}	addressable latch; unaddressed latch holds previous state
L	L	D ₁	H	L	L	O _{n-1}	D ₁	O _{n-1}	O _{n-1}	O _{n-1}	O _{n-1}	O _{n-1}	O _{n-1}	
L	L	D ₁	L	H	L	O _{n-1}	O _{n-1}	D ₁	O _{n-1}	O _{n-1}	O _{n-1}	O _{n-1}	O _{n-1}	
L	L	D ₁	H	H	L	O _{n-1}	O _{n-1}	O _{n-1}	D ₁	O _{n-1}	O _{n-1}	O _{n-1}	O _{n-1}	
L	L	D ₁	L	L	H	O _{n-1}	O _{n-1}	O _{n-1}	O _{n-1}	D ₁	O _{n-1}	O _{n-1}	O _{n-1}	
L	L	D ₁	H	L	H	O _{n-1}	O _{n-1}	O _{n-1}	O _{n-1}	O _{n-1}	D ₁	O _{n-1}	O _{n-1}	
L	L	D ₁	L	H	H	O _{n-1}	O _{n-1}	O _{n-1}	O _{n-1}	O _{n-1}	O _{n-1}	D ₁	O _{n-1}	
L	L	D ₁	H	H	H	O _{n-1}	O _{n-1}	O _{n-1}	O _{n-1}	O _{n-1}	O _{n-1}	O _{n-1}	D ₁	

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

X = state is immaterial

O_{n-1} = state before the positive transition of \bar{E}

D₁ = either HIGH or LOW

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ≤ 20 ns

	V _{DD} V	typical formula for P (μW)	where f _i = input freq. (MHz) f _o = output freq. (MHz) C _L = load capacitance (pF) Σ(f _o C _L) = sum of outputs V _{DD} = supply voltage (V)
Dynamic power dissipation per package (P)	5	700 f _i + Σ(f _o C _L) × V _{DD} ²	
	10	3700 f _i + Σ(f _o C _L) × V _{DD} ²	
	15	10800 f _i + Σ(f _o C _L) × V _{DD} ²	

A.C. CHARACTERISTICS

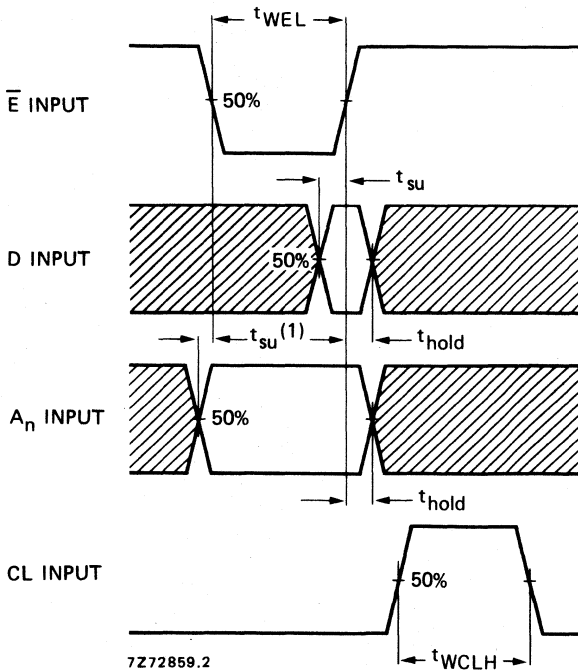
 $V_{SS} = 0 \text{ V}$; $T_{amb} = 25 \text{ }^\circ\text{C}$; $C_L = 50 \text{ pF}$; input transition times $\leq 20 \text{ ns}$

	V_{DD} V	symbol	min.	typ.	max.	typical extrapolation formula	
Propagation delays							
$\bar{E} \rightarrow O_n$	5			115	230	ns	$88 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
HIGH to LOW	10	t_{PHL}		50	95	ns	$39 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
	15			35	70	ns	$27 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
	5			95	195	ns	$68 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
LOW to HIGH	10	t_{PLH}		40	80	ns	$29 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
	15			30	55	ns	$22 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
$D \rightarrow O_n$	5			95	190	ns	$68 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
HIGH to LOW	10	t_{PHL}		35	75	ns	$24 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
	15			25	55	ns	$17 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
	5			85	170	ns	$58 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
LOW to HIGH	10	t_{PLH}		35	75	ns	$24 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
	15			25	55	ns	$17 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
$A_n \rightarrow O_n$	5			110	225	ns	$83 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
HIGH to LOW	10	t_{PHL}		45	95	ns	$34 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
	15			35	70	ns	$27 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
	5			95	190	ns	$68 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
LOW to HIGH	10	t_{PLH}		40	80	ns	$29 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
	15			30	55	ns	$22 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
$CL \rightarrow O_n$	5			85	165	ns	$58 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
HIGH to LOW	10	t_{PHL}		35	70	ns	$24 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
	15			25	50	ns	$17 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
Set-up times							
$D \rightarrow \bar{E}$	5		40	20		ns	see also waveforms Fig. 5
	10	t_{su}	15	5		ns	
	15		10	0		ns	
	5		40	20		ns	
$A_n \rightarrow \bar{E}$	10	t_{su}	20	10		ns	
	15		15	5		ns	
Hold times							
$D \rightarrow \bar{E}$	5		20	0		ns	
	10	t_{hold}	15	5		ns	
	15		15	5		ns	
	5		50	25		ns	
$A_n \rightarrow \bar{E}$	10	t_{hold}	20	10		ns	
	15		15	5		ns	
Minimum \bar{E} pulse width; LOW	5		75	35		ns	
	10	t_{WEL}	30	15		ns	
	15		20	10		ns	
Minimum CL pulse width; HIGH	5		70	35		ns	
	10	t_{WCLH}	30	15		ns	
	15		20	10		ns	

A.C. CHARACTERISTICS

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^\circ\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	symbol	min.	typ.	max.	typical extrapolation formula	
Output transition times HIGH to LOW	5	t_{THL}		60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$
	10		30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$	
	15		20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$	
LOW to HIGH	5	t_{TLH}		60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$
	10		30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$	
	15		20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$	



(1) The address to enable set-up time is the time before the HIGH to LOW enable transition that the address must be stable so that the correct latch is addressed and the other latches are not affected.

Fig. 5 Waveforms showing minimum \bar{E} and CL pulse widths, set-up times, hold times. Set-up and hold times are shown as positive values but may be specified as negative values.

QUADRUPLE 64-BIT STATIC SHIFT REGISTER

The HEF4731B and HEF4731V are quadruple 64-bit static shift registers each with separate serial data inputs (D_A to D_D), clock inputs (\overline{CP}_A to \overline{CP}_D) and data outputs (O_{63A} to O_{63D}) from the 64th register position.

Recommended supply voltage range for HEF4731B is 3 to 15 V and for HEF4731V is 4.5 to 12.5 V.

Data are shifted to the next stage on the negative-going transitions of the clock. Low impedance outputs are provided for direct interface to TTL.

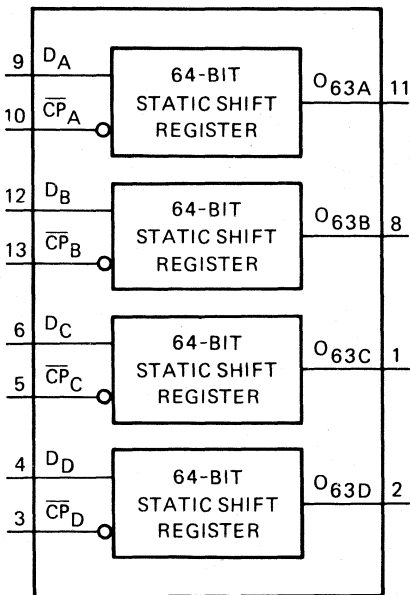


Fig. 1 Functional diagram. 7274633.1

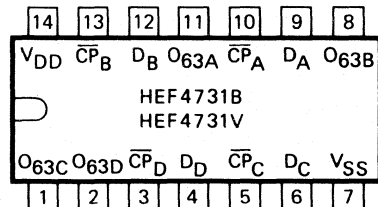


Fig. 2 Pinning diagram. 7274631

HEF4731BP; HEF4731VP : 14-lead DIL; plastic (SOT-27S, T, V).
HEF4731BD; HEF4731VD : 14-lead DIL; ceramic (SOT-73).

FAMILY DATA

I_{DD} LIMITS category LSI

see Family Specifications

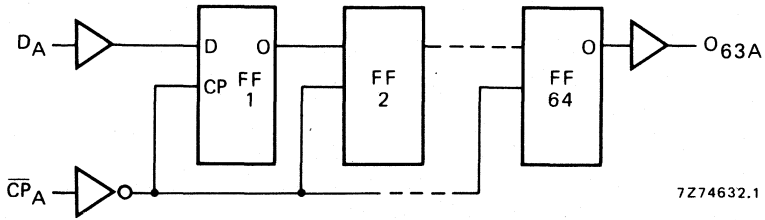


Fig. 3 Logic diagram (one of 64-bits shift register).

The values given at $V_{DD} = 15\text{ V}$ in the following d.c. and a.c. characteristics, are not applicable to the HEF4731V, because of its reduced supply voltage range.

D.C. CHARACTERISTICS

$V_{SS} = 0\text{ V}$; $V_I = V_{SS}$ or V_{DD}

	V_{DD} V	V_{OL} V	V_{OH} V	symbol	T_{amb} (°C)					
					-40		+25		+85	
					min.	max.	min.	max.	min.	max.
Output (source) current HIGH	5		2,5	$-I_{OH}$	3	2,5	2,0			mA
	5		4,6		1	0,85	0,65			mA
	10		9,5		3	2,5	2,0			mA
	15		13,5		10	8,5	6,5			mA
Output (sink) current LOW	4,75	0,4		I_{OL}	2,3	2,0	1,6			mA
	10	0,5			6,0	5,0	4,0			mA
	15	1,5			20,0	18,0	14,0			mA

A.C. CHARACTERISTICS

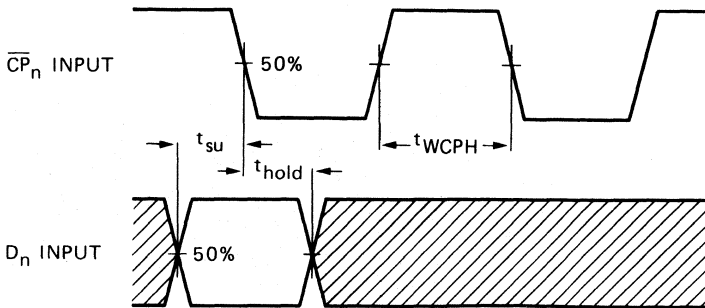
$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ °C}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	typical formula for P (μW)	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
Dynamic power dissipation per package (P)	5	$13\,000 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	10	$55\,000 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$140\,000 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

A.C. CHARACTERISTICS

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^\circ\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	symbol	min.	typ.	max.	typical extrapolation formula	
Propagation delays $\overline{CP} \rightarrow O_{63}$ HIGH to LOW	5			145	290	ns	$132\text{ ns} + (0,26\text{ ns/pF}) C_L$
	10	t_{PHL}		55	110	ns	$47\text{ ns} + (0,16\text{ ns/pF}) C_L$
	15			40	80	ns	$34\text{ ns} + (0,11\text{ ns/pF}) C_L$
5			160	320	ns	$138\text{ ns} + (0,45\text{ ns/pF}) C_L$	
LOW to HIGH	10	t_{PLH}		65	130	ns	$56\text{ ns} + (0,19\text{ ns/pF}) C_L$
	15			45	90	ns	$39\text{ ns} + (0,13\text{ ns/pF}) C_L$
	5			30	60	ns	$10\text{ ns} + (0,40\text{ ns/pF}) C_L$
Transition times O_{63} HIGH to LOW	10	t_{THL}		12	24	ns	$3\text{ ns} + (0,18\text{ ns/pF}) C_L$
	15			10	20	ns	$3\text{ ns} + (0,13\text{ ns/pF}) C_L$
	5			40	80	ns	$8\text{ ns} + (0,65\text{ ns/pF}) C_L$
LOW to HIGH	10	t_{TLH}		20	40	ns	$5\text{ ns} + (0,30\text{ ns/pF}) C_L$
	15			15	30	ns	$5\text{ ns} + (0,20\text{ ns/pF}) C_L$
	5			160	80	ns	
Minimum clock pulse width; HIGH	10	t_{WCPH}		60	30	ns	} see also waveforms Fig. 4
	15			40	20	ns	
	5			25	-5	ns	
Set-up time $D \rightarrow \overline{CP}$	10	t_{su}		15	-5	ns	} see also waveforms Fig. 4
	15			15	-5	ns	
	5			50	20	ns	
Hold time $D \rightarrow \overline{CP}$	10	t_{hold}		30	10	ns	} see also waveforms Fig. 4
	15			20	5	ns	
	5			3	6	MHz	
Maximum clock pulse frequency	10	f_{max}		8	16	MHz	
	15			12	25	MHz	



7274634

Fig. 4 Waveforms showing minimum clock pulse width, set-up and hold times for D to \overline{CP} . Set-up and hold times are shown as positive values but may be specified as negative values.

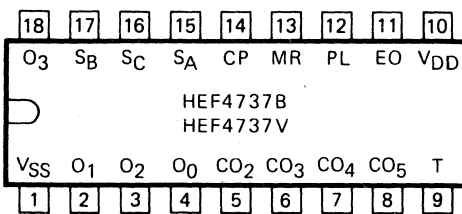
QUADRUPLE STATIC DECADE COUNTERS

The HEF4737B and HEF4737V are static quadruple decade counters for frequencies from 0 to 10 MHz. The counters are supplied with an extra overload flip-flop giving a total count capability of 19 999. The counter has the following inputs and outputs: a count input (CP), an asynchronous reset input (MR), an asynchronous preset input (PL), a transfer input (T), an output enable input (EO) (which controls the BCD outputs), the digit select inputs (S_A, S_B, S_C) (which perform selection of the contents of the latches to the 3-state BCD outputs (O_0 to O_3)), and the carry outputs (CO_2 to CO_5) (which give the carry signals of the decades except from the first decade).

The complementary MOS structure gives the devices very low stand-by and operating dissipation. Operating from a single supply voltage all outputs can drive one standard TTL input without interface circuitry under all specified operating conditions.

The BCD digit outputs are LOCMOS 3-state outputs. The high impedance off-state feature allows common bussing of the outputs. The counters are supplied with asynchronous reset and preset to 19 999 facilities making them suitable for counter and time base applications. All carry signals are available except from the first decade.

Recommended supply voltage range for HEF4737B is 3 to 15 V and for HEF4737V is 4,5 to 12,5 V.



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PINNING

CP	count input
MR	asynchronous reset input
PL	asynchronous preset input
T	transfer input
S_A, S_B, S_C	digit select inputs
EO	output enable input
O_0 to O_3	BCD outputs
CO_2 to CO_5	carry outputs

Fig. 1 Pinning diagram.

SUPPLY VOLTAGE

	rating	recommended operating
HEF4737B	-0,5 to 18	3,0 to 15,0 V
HEF4737V	-0,5 to 18	4,5 to 12,5 V

HEF4737BP; HEF4737VP: 18-lead DIL; plastic (SOT-102A).

HEF4737BD; HEF4737VD: 18-lead DIL; ceramic (SOT-133).

FAMILY DATA

I_{DD} LIMITS category LSI

see Family Specifications

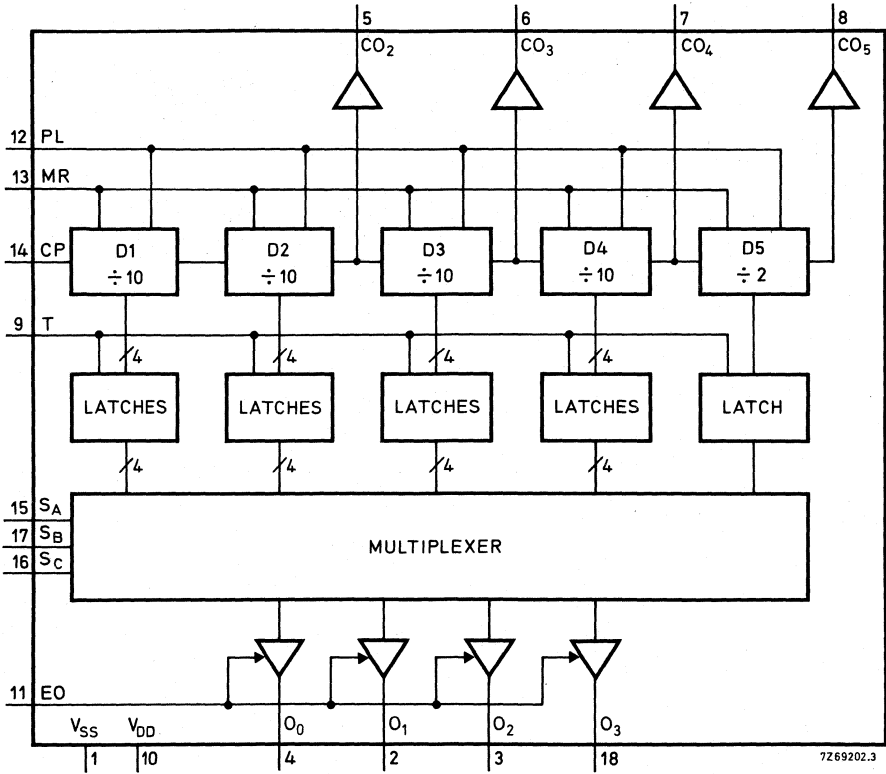


Fig. 2 Block diagram.

FUNCTIONAL DESCRIPTION

Input signals

Count input (CP)

The signal to be counted is applied to this input. When PL and MR are LOW the contents of the counter increments by one at a LOW to HIGH transition of CP.

Reset input (MR)

This is an asynchronous reset. A HIGH level applied to this input will reset the counter to zero independent of the level at the count input and preset input.

Preset input (PL)

This is an asynchronous preset. When MR is LOW a HIGH at the PL input will preset the counter to 19 999 independent of the level at the count input.

Transfer input (T)

A HIGH level applied to this input allows the information held by the counter to pass to the latches.



Output enable input (EO)

A HIGH level at this input enables the BCD outputs and information can be read out of the latches using the multiplexer. A LOW level at this input disables the BCD outputs making them floating (high impedance off-state).

Digit select inputs (S_A, S_B, S_C)

S _A	S _B	S _C	
L	L	L	selects D1 (LSD)
H	L	L	selects D2
L	H	L	selects D3
H	H	L	selects D4
X	X	H	selects D5 (MSD)

When D5 is selected, the contents of D5 is available at O₀ and O₁, O₂ and O₃ are LOW.

LSD = least significant divider
MSD = most significant divider

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

X = state is immaterial

Output signals

The carry outputs are active LOW outputs.

Carry output CO₂

When the contents of the first two decades of the counter are both 9 then the CO₂ output becomes LOW. It remains LOW until the next LOW to HIGH transition of the count input, i.e. until the contents of the first two decades are zero. CO₂ is LOW when the contents of the counter are: 00 099, 00 199, 02 299 etc.

Carry output CO₃

When the contents of the first three decades of the counter are all 9 then the CO₃ output becomes LOW. It remains LOW until the next LOW to HIGH transition of the count input, i.e. until the contents of the first three decades are zero. CO₃ is LOW when the contents of the counter are 00 999, 01 999, 02 999 etc.

Carry output CO₄

When the contents of the first four decades of the counter are all 9 then the CO₄ output becomes LOW. It remains LOW until the next LOW to HIGH transition of the count input, i.e. until the contents of the first four decades are zero. CO₄ is LOW when the contents of the counter are 09 999 and 19 999.

The carry signals CO₂, CO₃ and CO₄ are suppressed while the preset is active. A HIGH to the preset input sets the counter to 19 999 but the carry signals remain HIGH until preset input returns to LOW, then the carry outputs will also become LOW.

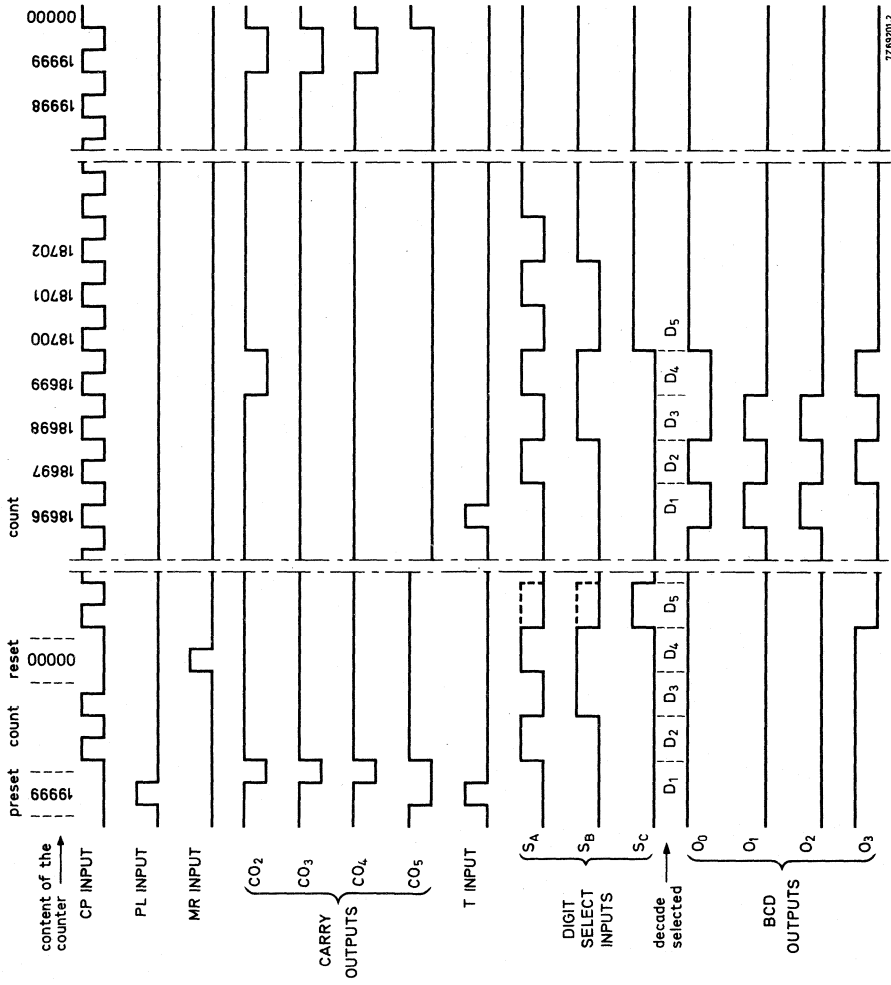
Carry output CO₅

When the content of the counter is 10 000 the CO₅ output becomes LOW. It returns to HIGH when the content of the counter is zero.

Digit outputs (O₀ to O₃)

The digit outputs give the contents of the selected latch. The output is in the form of BCD, positive logic.





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Fig. 3 Timing diagram.



The values given at $V_{DD} = 15\text{ V}$ in the following d.c. and a.c. characteristics, are not applicable to the HEF4737V, because of its reduced supply voltage range.

D.C. CHARACTERISTICS $V_{SS} = 0\text{ V}$

	V_{DD} V	V_{OH} V	V_{OL} V	symbol	T_{amb} (°C)						
					-40		+25		+85		
					min.	max.	min.	max.	min.	max.	
Input leakage current at $V_I = 0$ or V_{DD}	10			$\pm I_{IN}$	-	-	-	0,3	-	1	μA
	15				-	-	-	0,3	-	1	μA
Output (sink) current LOW	4,75		0,4	I_{OL}	1,6	-	1,6	-	1,4	-	mA
	10		0,5		2,5	-	2,3	-	1,7	-	mA
	15		1,5		7,0	-	6,0	-	4,0	-	mA
Output (source) current HIGH	5	4,6		$-I_{OH}$	0,96	-	0,80	-	0,65	-	mA
	10	9,5			2,4	-	2,0	-	1,6	-	mA
	15	13,5			7,0	-	6,0	-	4,5	-	mA
Output (source) current HIGH	5	2,5		$-I_{OH}$	3,0	-	2,5	-	2,0	-	mA
3-state output leakage current $V_O = 0$ or V_{DD}	10			$\pm I_{OZ}$	-	1,6	-	1,6	-	12	μA
	15				-	1,6	-	1,6	-	12	μA

A.C. CHARACTERISTICS

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^\circ\text{C}$; $C_L = 15\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	symbol				typical extrapolation formula		
			min.	typ.	max.			
Propagation delays CP \rightarrow O_n (D1 selected)	5	tPHL		320	640	ns	308 ns + (0,24 ns/pF) C_L	
	10		120	240	ns	125 ns + (0,10 ns/pF) C_L		
	15	90	180	ns	86 ns + (0,07 ns/pF) C_L			
	HIGH to LOW	5	tPLH		320	640	ns	296 ns + (0,48 ns/pF) C_L
		10		120	240	ns	110 ns + (0,20 ns/pF) C_L	
		15		90	180	ns	82 ns + (0,15 ns/pF) C_L	
CP \rightarrow O_n (D5 selected)	5	tPHL		620	1240	ns	608 ns + (0,24 ns/pF) C_L	
	10		330	660	ns	325 ns + (0,10 ns/pF) C_L		
	15	250	500	ns	246 ns + (0,07 ns/pF) C_L			
	HIGH to LOW	5	tPLH		620	1240	ns	596 ns + (0,48 ns/pF) C_L
		10		330	660	ns	320 ns + (0,20 ns/pF) C_L	
		15		250	500	ns	242 ns + (0,15 ns/pF) C_L	
CP \rightarrow CO_2	5	tPHL		220	440	ns	208 ns + (0,24 ns/pF) C_L	
	10		110	220	ns	105 ns + (0,10 ns/pF) C_L		
	15	85	170	ns	81 ns + (0,07 ns/pF) C_L			
	HIGH to LOW	5	tPLH		220	440	ns	196 ns + (0,48 ns/pF) C_L
		10		110	220	ns	100 ns + (0,20 ns/pF) C_L	
		15		85	170	ns	77 ns + (0,15 ns/pF) C_L	

A.C. CHARACTERISTICS (continued)

 $V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $C_L = 15\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	symbol	min.	typ.	max.	typical extrapolation formula	
Propagation delays							
CP \rightarrow CO ₅	5			350	700	ns	338 ns + (0,24 ns/pF) C _L
HIGH to LOW	10	t _{PHL}		160	320	ns	155 ns + (0,10 ns/pF) C _L
	15			120	240	ns	116 ns + (0,07 ns/pF) C _L
LOW to HIGH	5			350	700	ns	326 ns + (0,48 ns/pF) C _L
	10	t _{PLH}		160	320	ns	150 ns + (0,20 ns/pF) C _L
	15			120	240	ns	112 ns + (0,15 ns/pF) C _L
S _n \rightarrow O _n	5			200	400	ns	188 ns + (0,24 ns/pF) C _L
HIGH to LOW	10	t _{PHL}		80	160	ns	75 ns + (0,10 ns/pF) C _L
	15			55	110	ns	51 ns + (0,07 ns/pF) C _L
LOW to HIGH	5			200	400	ns	176 ns + (0,48 ns/pF) C _L
	10	t _{PLH}		80	160	ns	70 ns + (0,20 ns/pF) C _L
	15			55	110	ns	47 ns + (0,15 ns/pF) C _L
T \rightarrow O _n	5			220	440	ns	208 ns + (0,24 ns/pF) C _L
HIGH to LOW	10	t _{PHL}		90	180	ns	85 ns + (0,10 ns/pF) C _L
	15			60	120	ns	56 ns + (0,07 ns/pF) C _L
LOW to HIGH	5			220	440	ns	196 ns + (0,48 ns/pF) C _L
	10	t _{PLH}		90	180	ns	80 ns + (0,20 ns/pF) C _L
	15			60	120	ns	52 ns + (0,15 ns/pF) C _L
MR \rightarrow O _n	5			490	980	ns	478 ns + (0,24 ns/pF) C _L
HIGH to LOW	10	t _{PHL}		200	400	ns	195 ns + (0,10 ns/pF) C _L
	15			60	120	ns	56 ns + (0,07 ns/pF) C _L
PL \rightarrow O _n	5			260	520	ns	236 ns + (0,48 ns/pF) C _L
LOW to HIGH	10	t _{PLH}		110	220	ns	100 ns + (0,20 ns/pF) C _L
	15			85	170	ns	77 ns + (0,15 ns/pF) C _L
MR \rightarrow CO _n	5			350	700	ns	326 ns + (0,48 ns/pF) C _L
LOW to HIGH	10	t _{PLH}		160	320	ns	150 ns + (0,20 ns/pF) C _L
	15			120	240	ns	112 ns + (0,15 ns/pF) C _L
PL \rightarrow CO _n	5			350	700	ns	338 ns + (0,24 ns/pF) C _L
HIGH to LOW	10	t _{PHL}		160	320	ns	155 ns + (0,10 ns/pF) C _L
	15			120	240	ns	116 ns + (0,07 ns/pF) C _L
Output transition times; any output	5			35	70	ns	15 ns + (0,40 ns/pF) C _L
HIGH to LOW	10	t _{THL}		18	36	ns	9 ns + (0,18 ns/pF) C _L
	15			15	30	ns	8 ns + (0,13 ns/pF) C _L
LOW to HIGH	5			50	100	ns	15 ns + (0,70 ns/pF) C _L
	10	t _{TLH}		30	60	ns	13 ns + (0,33 ns/pF) C _L
	15			25	50	ns	13 ns + (0,23 ns/pF) C _L

	V _{DD} V	symbol	min.	typ.	max.
3-state propagation delays					
Output disable times					
EO → O _n	5			60	120 ns
HIGH	10	t _{PHZ}	35	70	ns
	15		25	50	ns
LOW	5		60	120	ns
	10	t _{PLZ}	35	70	ns
	15		25	50	ns
Output enable times					
EO → O _n	5		90	180	ns
HIGH	10	t _{PZH}	40	80	ns
	15		30	60	ns
LOW	5		90	180	ns
	10	t _{PZL}	40	80	ns
	15		30	60	ns
Minimum CP pulse width; LOW	5		160	80	ns
	10	t _{WCPL}	60	30	ns
	15		50	25	ns
Minimum MR pulse width; HIGH	5		100	50	ns
	10	t _{WMRH}	50	25	ns
	15		40	20	ns
Minimum PL pulse width; HIGH	5		120	60	ns
	10	t _{WPLH}	60	30	ns
	15		50	25	ns
Minimum T pulse width; HIGH	5		100	50	ns
	10	t _{WTH}	40	20	ns
	15		36	18	ns
Maximum clock pulse frequency	5		3	6	MHz
	10	f _{max}	8	16	MHz
	15		10	20	MHz

	V _{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	950 f _i + Σ(f _o C _L) × V _{DD} ²	f _i = input freq. (MHz)
	10	4 200 f _i + Σ(f _o C _L) × V _{DD} ²	f _o = output freq. (MHz)
	15	11 200 f _i + Σ(f _o C _L) × V _{DD} ²	C _L = load cap. (pF)
			Σ(f _o C _L) = sum of outputs
			V _{DD} = supply voltage (V)

DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

HEF4738V

LSI

IEC/IEEE BUS INTERFACE

The HEF4738V is an implementation of the IEC-bus as described in IEC report 66 CO 22 (interface system for programmable measuring apparatus) as well as in IEEE standard 488-1975 (standard digital interface for programmable instrumentation).

Together with bus-drivers, level converters and multiplexers it is suitable for connecting electronic programmable and non-programmable equipment to an IEC/IEEE interface bus.

All inputs have standard HE4000B family levels.

In the circuit the following standard interface functions are incorporated:

- Complete source handshake (subset SH1)
- Complete acceptor handshake (subset AH1)
- Basic talker with serial poll and talk-only mode (when It = LOW, subset T1; It = HIGH, subset T5)
- Basic listener with listen-only mode (when It = LOW, subset L1; It = HIGH, subset L3)
- Complete service request (subset SR1)
- Complete remote local (subset RL1)
- Remote parallel poll configuration (subset PP1)
- Complete device clear (subset DC1)
- Complete device trigger (subset DT1)
- Some controller facilities

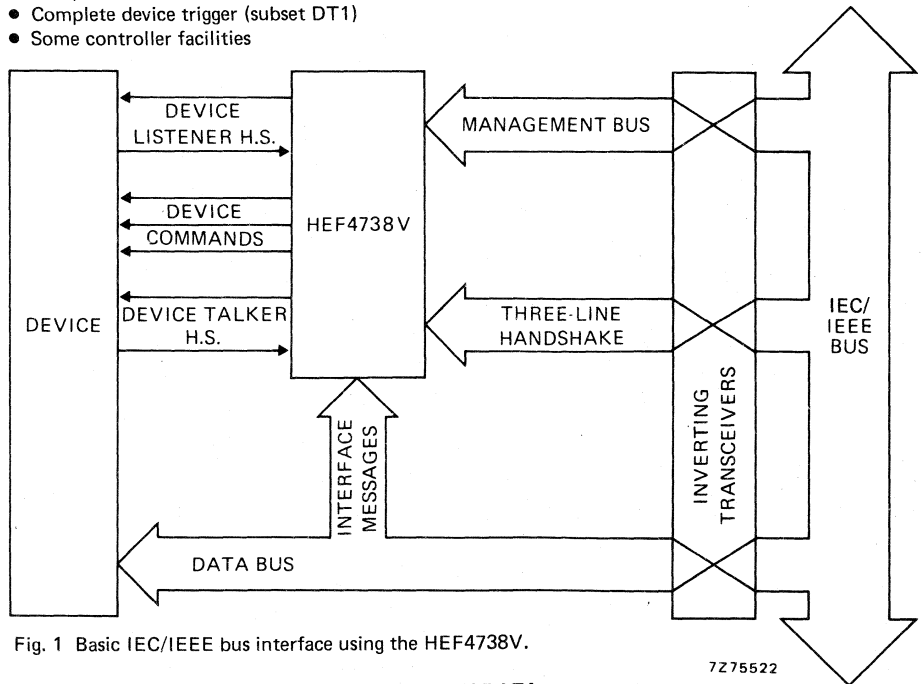


Fig. 1 Basic IEC/IEEE bus interface using the HEF4738V.

SUPPLY VOLTAGE

rating	recommended operating
-0,5 to 18	4,5 to 12,5 V

FAMILY DATA

I_{DD} LIMITS category LSI

see Family Specifications

7275522

GENERAL DESCRIPTION

The inputs IRFD, IDAC, $\overline{\text{IDAV}}$, $\overline{\text{IFC}}$, $\overline{\text{IREN}}$, $\overline{\text{IATN}}$, $\overline{\text{IDY}}$ and IDIO1 to IDIO7 must be connected via an inverting TTL to LOC MOS level converter to the respective bus lines: NRFD, NDAC, DAV, IFC, REN, ATN, IDY and DIO1 to DIO7.

The outputs ORFD, ODAC, $\overline{\text{ODAV}}$ and $\overline{\text{OSRQ}}$ can drive one standard TTL load and are suitable for driving NRFD, NDAC, DAV and SRQ via an inverting bus-driver circuit.

The parallel poll outputs OP1, OP2, OP3 and OPP can also drive one standard TTL load. Outputs OP1, OP2 and OP3 are connected to flip-flops, which store the attendant bits P1, P2 and P3 of the last PPE message. OP1, OP2 and OP3 have to be decoded externally and multiplexed to the DIO-lines when OPP is LOW.

All other output stages are standard HE4000B family.

Most of the functions in the IEC/IEEE interface IC are realized with synchronous sequential logic, which is driven from the clock input CP. HIGH to LOW transitions are used to synchronize input signals and LOW to HIGH transitions trigger the internal flip-flops. In order to meet the IEC/IEEE timing specifications, the maximum clock frequency is 2 MHz. The maximum data transfer is then 200 kbytes/second.

Input $\overline{\text{Irdy}}$ (not ready for next message) and output Odvd (data valid device) are intended for a two-wire handshake procedure between the acceptor function in the IC and the data input of the device (instrument to be connected to the interface system). The procedure is made so, that if the device reacts fast enough, the handshake procedure can be omitted by interconnecting Odvd and $\overline{\text{Irdy}}$. The conditions to be fulfilled by the device are:

- The device must be able to accept a data byte within one clock period after dvd goes HIGH under all conditions.
- The device must be ready to process a data byte within two clock periods plus the minimum settling time of the talker devices under all conditions.

Input $\overline{\text{Inba}}$ (not new byte available) and output Odcd (don't change data) are intended for a two-wire handshake procedure with the source function in the IC and the data output of the device (instrument). The procedure is so made that if the device reacts fast enough the handshake procedure can be omitted by interconnecting Odcd and $\overline{\text{Inba}}$. The conditions to be fulfilled by the device are:

- The device must be able to set a new data byte on the bus within one clock period after dcd goes LOW under all conditions.
- The device must be able to have the next data byte available within seven clock periods under all conditions.

Input lsr and output Ored should be connected to an external parallel-in/serial-out (when Ored is HIGH parallel-in, when LOW serial-out) shift register, which must be connected to the clock CP and must trigger on the LOW to HIGH transitions. The data on the parallel inputs of this external shift register are loaded in parallel and shifted-out via input lsr into an internal shift register. The eleven serial input signals are in the order of shifting: A5, A4, A3, A2, A1, ton, lon, lt, rsv, rtl and ist. Signals A5, A4, A3, A2 and A1 represent the device talker and listener address. When signal lt (either listener or talker) is HIGH, a listener addressing sets the talker to the idle state and a talker addressing sets the listener to the idle state (subset T5 and L3). With lt LOW, the device can be addressed to be a listener and a talker. Because of the serial input procedure, all these input signals arrive in the interface functions of the IC between 16 and 32 clock cycles.

The signals ton, lon, rsv, rtl and ist are standard IEC/IEEE inputs.

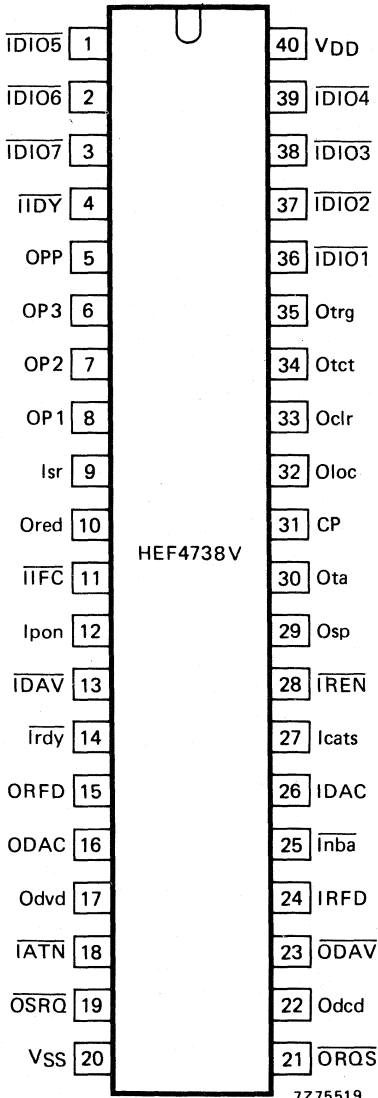
The output Oclr or Otrg is HIGH if DCAS (device clear active state) or DTAS (device trigger active state) respectively is active.

The output Oloc is HIGH when LOCS (local state) or LWLS (local with lock-out state) is active.

Output $\overline{\text{OSRQ}}$ is HIGH when the rsv signal is read from the external shift register and the SRQS (request service state) is active. After this request has been answered by a serial poll, $\overline{\text{ORQS}}$ is HIGH in the APRS (affirmative poll response state). The inverted signal on $\overline{\text{ORQS}}$ must be multiplexed to bus-line DIO7, together with the status byte of the other DIO lines, when output Osp is HIGH in the SPAS (serial poll active state).

Input *Icats* and output *Otct* are intended for use of this IC in a controller. When *Icats* is HIGH, the source handshake function will exit SIDS and SIWS and enter respectively SGNS and SWNS. Output *Otct* is HIGH if the *tct* message is sent over the interface and the ACDS state is active. A HIGH on input *Ipon* sets each function to its initial state. This level can be set to LOW after the IC has received 32 clock pulses at stabilized supply voltage.

DEVELOPMENT SAMPLE DATA



Input pins

- 1,2,3,36, 37,38,39 } = IDIO1 to 7: input DIO
- 4 = IIDY input IDY not
- *9 = Isr input shift register
- 11 = IIFC input IFC not
- 12 = Ipon input pon
- 13 = IDAV input DAV not
- 14 = Irdy input rdy not
- 18 = IATN input ATN not
- 24 = IRFD input RFD
- 25 = Inba input nba not
- 26 = IDAC input DAC
- 27 = Icats input cats
- 28 = IREN input REN not
- 31 = CP clock pulse input

Output pins

- 5 = OPP output PP
- 8,7,6 = OP1 to OP3 output P1 to P3
- 10 = Ored output red
- 15 = ORFD output RFD
- 16 = ODAC output DAC
- 17 = Odvd output dvd
- 19 = OSRQ output SRQ not
- 21 = ORQS output RQS not
- 22 = Odcd output dcd
- 23 = ODAV output DAV not
- 29 = Osp output sp
- 30 = Ota output ta
- 32 = Oloc output loc
- 33 = Oclr output clr
- 34 = Otct output tct
- 35 = Otrg output trg

Supply pins

- 20 = VSS: more negative supply line
- 40 = VDD: more positive supply line

* Isr is serial input for signals A5, A4, A3, A2, A1, ton, lon, lt, rsv, rtl and ist.

Fig. 2. Pinning diagram; for abbreviations see following list.
HEF4738VP: 40-lead DIL; plastic (SOT-129).

7275519

LIST OF USED ABBREVIATIONS

A1 to A5	address	SIWS	source idle wait state
ACDS	acceptor data state	sp	serial poll
APRS	affirmative poll response state	SPAS	serial poll active state
ATN	attention	SPD	serial poll disable
AVD	address valid	SPE	serial poll enable
cats	controller active or transfer state	sr	shift register
clr	device clear	SRQ	service request
CVD	command valid	SRQS	request service state
DAC	data accepted	SWNS	source wait for new cycle state
DAV	data valid	ta	talker active
DCAS	device clear active state	tct	talk control
dcd	don't change data	ton	talk only
DCL	device clear	trg	trigger
DIO	data input output	UNL	unlisten
DTAS	device trigger active state		
dvd	data valid device		
EOI	end of output/identify		
GTL	go to local		
IDY	identify		
IFC	interface clear		
ist	individual status		
LLO	local lock-out		
loc	local		
LOCS	local state		
lon	listen only		
lt	listener or talker function		
LWLS	local with lock-out state		
MLA	my listen address		
MTA	my talk address		
nba	new byte available		
NRFD	not ready for data		
NDAC	not data accepted		
OTA	other talk address		
P1 to P3	parallel response messages		
PCA	parallel poll configure accepted		
pon	power on		
PP	parallel poll message enable		
PPC	parallel poll configure		
PPD	parallel poll disable		
PPE	parallel poll enable		
PPU	parallel poll unconfigure		
rdy	ready for next message		
red	ready for next shift cycle		
REN	remote enable		
RFD	ready for data		
RQS	requested service		
rsv	request for service		
rtl	return to local		
SDC	selected device clear		
SGNS	source generate state		
SIDS	source idle state		

DEVELOPMENT SAMPLE DATA

D.C. CHARACTERISTICS

V_{SS} = 0 V

	V _{DD} V	V _{OL} V	V _{OH} V	symbol	T _{amb} (°C)			
					-40 min.	+25 max.	+85 min.	+85 max.
Output current HIGH; see note	5		2,5	-I _{OH}	3	2,5	2,0	mA
	5		4,6		1	0,85	0,65	mA
	10		9,5		3	2,5	2,0	mA
Output current LOW; see note	4,75	0,4		I _{OL}	2,7	2,3	1,8	mA
	10	0,5			9,5	8,0	6,3	mA
Quiescent device current	5			I _{DD}	50	50	375	μA
	10				100	100	750	μA

Note

Output currents for pins: 5 = OPP, 6 = OP3, 7 = OP2, 8 = OP1, 15 = ORFD, 16 = ODAC, 19 = \overline{OSRQ} , 23 = ODAV. These pins can drive one standard TTL load.

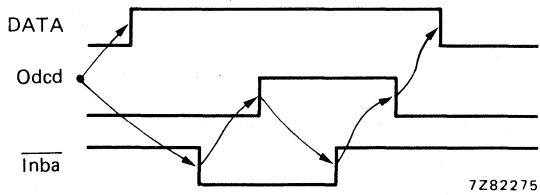


Fig. 4 Waveforms showing data exchange in talker function.

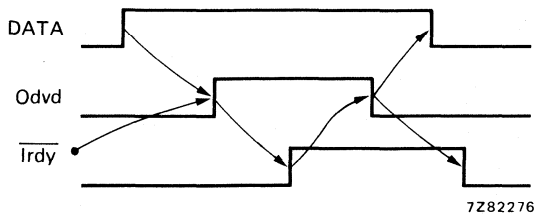
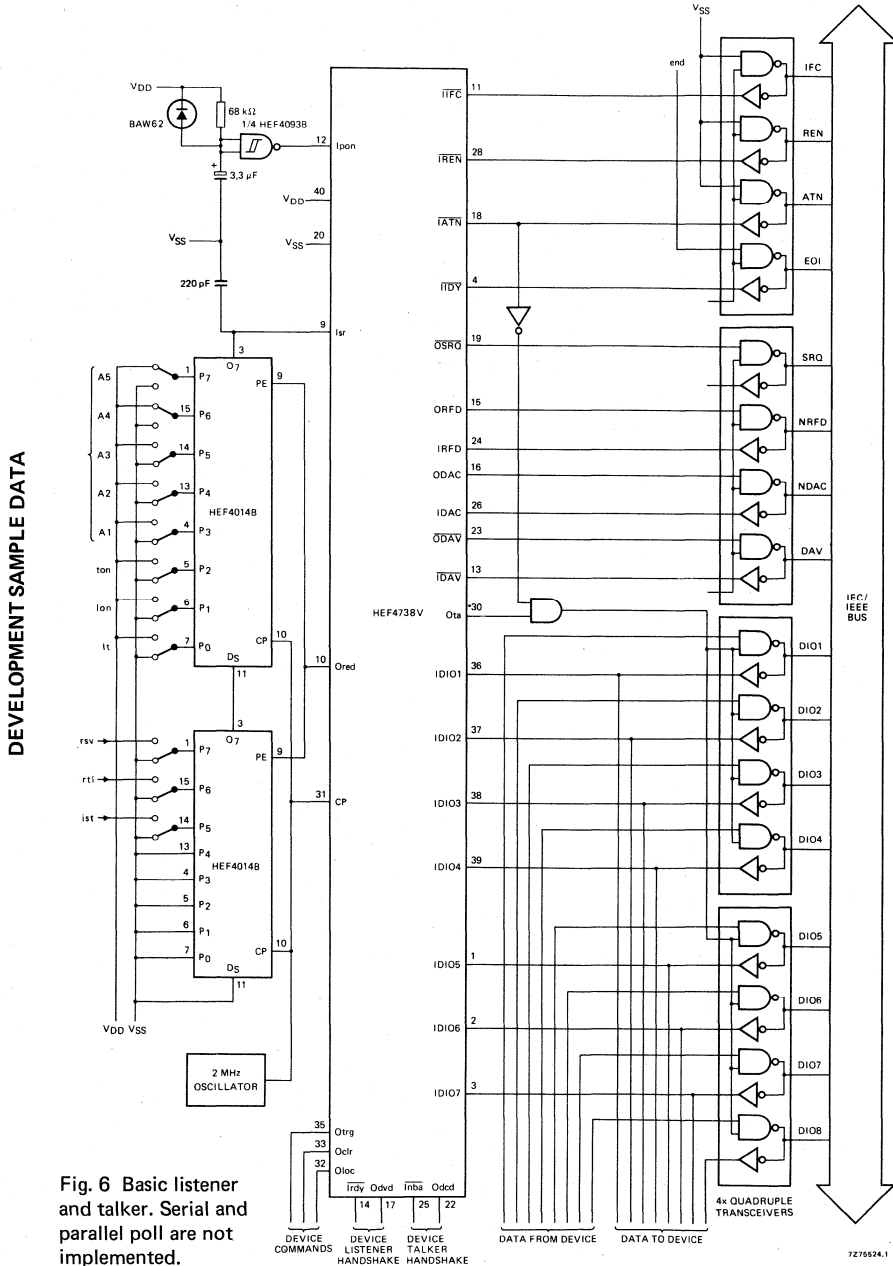


Fig. 5 Waveforms showing data exchange in listener function.

APPLICATION INFORMATION



DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

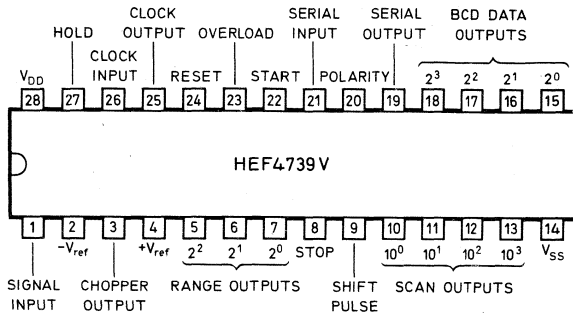
HEF4739V

LSI

DIGITAL VOLTMETER CIRCUIT

The HEF4739V is intended for use in dual polarity digital voltmeters where the delta-modulation principle is used for analogue to digital conversion. The device contains all the digital logic of the voltmeter including the facility for automatic range selection. Each output can drive one TTL input under all specified conditions.

Recommended operating supply voltage range is 4,5 to 12,5 V (−0,5 to + 18 V as a rating).



7272116.3

Fig. 1 Pinning diagram.

HEF4739VP: 28-lead DIL; plastic (SOT-117).

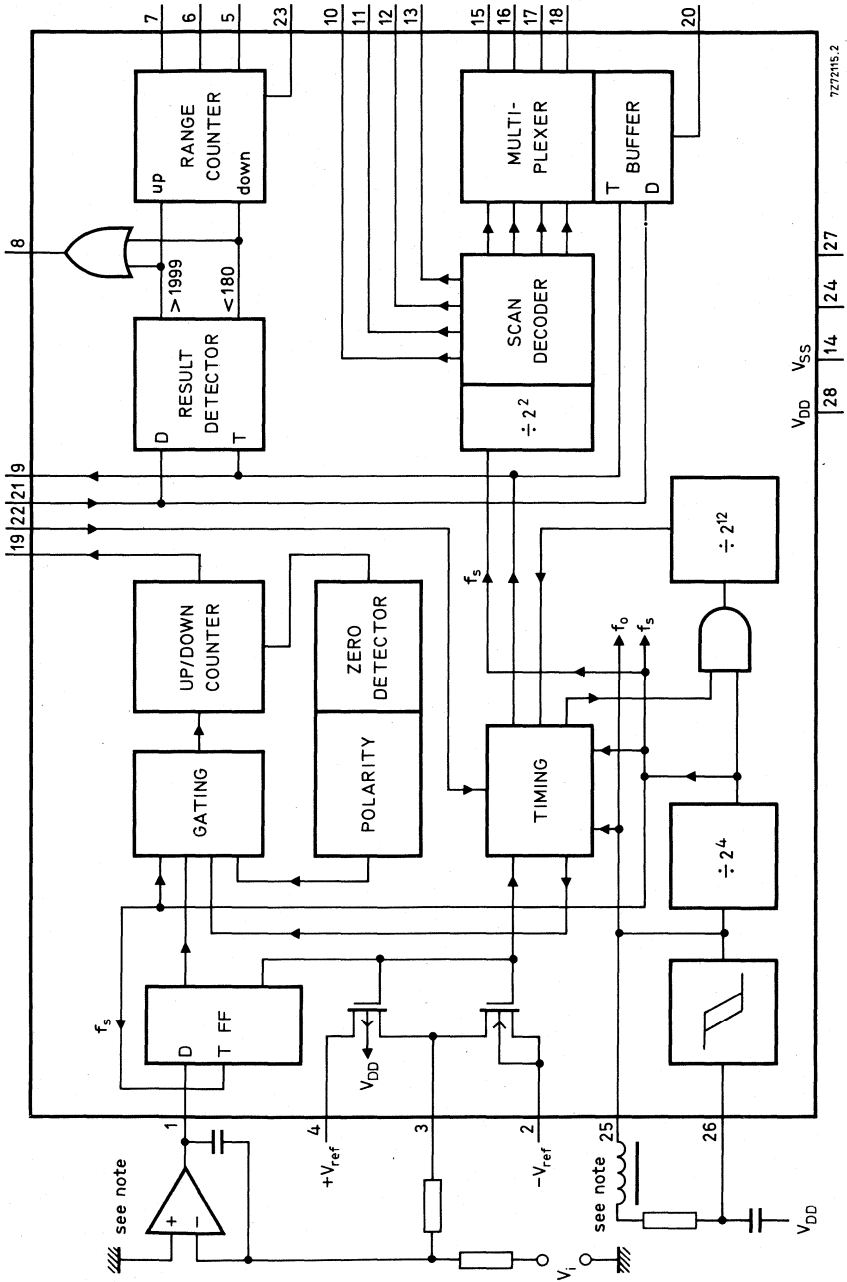
PINNING

- | | |
|--------------------------|-------------------------------|
| 1. Signal input | 15. 2^0 ; BCD data output |
| 2. $-V_{ref}$ | 16. 2^1 ; BCD data output |
| 3. Chopper output | 17. 2^2 ; BCD data output |
| 4. $+V_{ref}$ | 18. 2^3 ; BCD data output |
| 5. 2^2 ; range output | 19. Serial output |
| 6. 2^1 ; range output | 20. Polarity output |
| 7. 2^0 ; range output | 21. Serial input |
| 8. Stop output | 22. Start input |
| 9. Shift pulse output | 23. Overload output |
| 10. 10^0 ; scan output | 24. Reset input |
| 11. 10^1 ; scan output | 25. Clock output |
| 12. 10^2 ; scan output | 26. Clock input |
| 13. 10^3 ; scan output | 27. Data hold input |
| 14. V_{SS} (ground) | 28. V_{DD} (supply voltage) |

FAMILY DATA

see Family Specifications

I_{DD} LIMITS category LSI



Note: system earth not connected to VSS.

Fig. 2 Block diagram.

7272HS.2

FUNCTIONAL DESCRIPTION

Signal input (pin 1)

To be connected with output of an integrator.
 HIGH: chopper output connected with $+V_{ref}$
 LOW : chopper output connected with $-V_{ref}$

Chopper output (pin 3)

To be connected with input of an integrator.
 When signal input is HIGH: chopper output is connected with $+V_{ref}$
 When signal input is LOW : chopper output is connected with $-V_{ref}$

Reference inputs

$+V_{ref}$ has to be connected to the positive reference voltage of the system and $-V_{ref}$ to the negative reference voltage.

Polarity output

This output is HIGH if the signal input is more frequently HIGH than LOW.

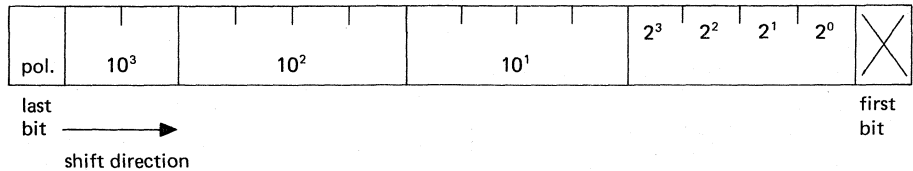
Clock input/clock output

The clock frequency is determined by external components. The clock input can be used as an input if an external clock is applied. The clock frequency (f_0) is 16 times the sample frequency (f_s) and the measuring time is 65 536 clock pulses.

Serial input/serial output/shift pulse output

The serial input and serial output pins should be externally connected together. Between two measurements a train of 16 pulses appear at the shift pulse output. This pulse train is used internally to shift the information from the up/down counter to the buffer. The serial output is the output of the up/down counter and serial input is the input to the buffer.

The 16-bit serial information is as follows:



From these 16 bits the first bit should be neglected and the last bit gives the polarity.

Start input/stop output

The built-in automatic ranging circuit will select a higher range if the result is greater than 1999 and a lower range if the result is less than 180. A change in range will be indicated by a LOW on the stop output. In order to allow the external ranging circuitry to respond to a change in range the next measuring period will be delayed until the start input has been HIGH for at least 16 clock pulses.

Range outputs/overload output

The range outputs present in binary form the state of the range selector. The overload output becomes HIGH when the measuring result is greater than 1999 independent of the selected range.

DEVELOPMENT SAMPLE DATA



FUNCTIONAL DESCRIPTION (continued)

BCD data outputs

These outputs show the contents of the selected digit of the buffer register in BCD code.

Scan outputs

These outputs show at each moment which digit of the buffer has been selected. The selected output is HIGH: scan sequence $10^3 - 10^2 - 10^1 - 10^0$. The scan pulses are separated by one clock pulse (interdigit blanking).

Reset input/data hold input (see function table below)

When the reset input has been LOW for at least 32 clock pulses the circuit is completely reset. The ranging is then in the lowest position and the 10^3 digit is selected. After reset the next measuring period starts. When having data hold mode the last measuring result is maintained.

FUNCTION TABLE

reset	hold	function
L	L	test mode *
L	H	reset
H	L	data hold
H	H	normal operation

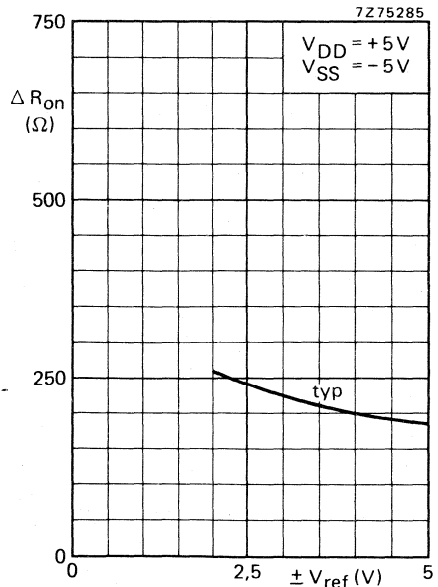
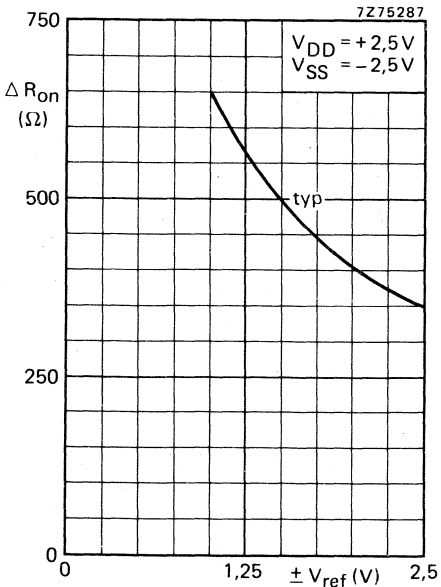
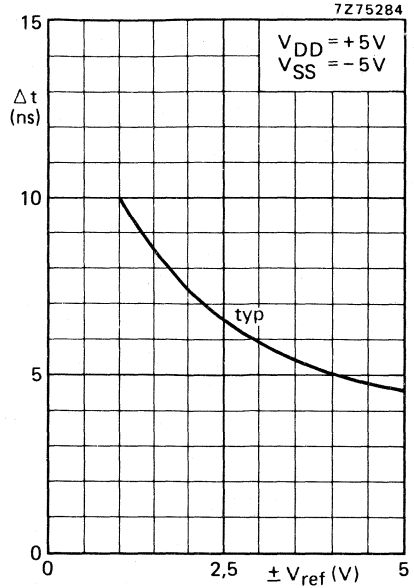
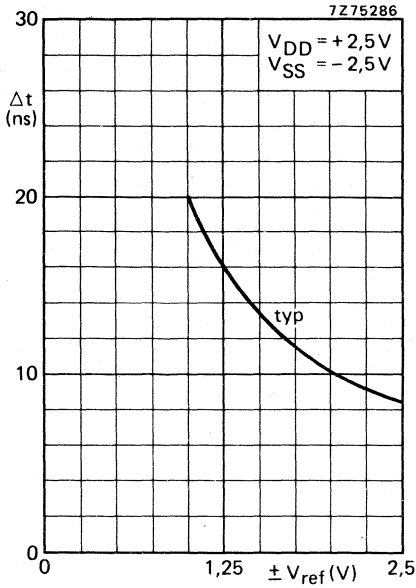
* Used for final testing in the factory.

A.C. CHARACTERISTICS

$T_{amb} = 25\text{ }^{\circ}\text{C}$; input transition time $\leq 20\text{ ns}$; input voltage swing = $V_{SS} - V_{DD}$; output load capacitance = 15 pF ; all times referred to 50% voltage swing.

	symbol	min typ max			conditions and references	
					V_{DD} V	
Clock input frequency	f_{max}	1 2	2 4	— —	MHz MHz	5 10
Switching speed unbalance of chopper	Δt	—	10 5	50 25	ns ns	$\left\{ \begin{array}{l} V_{DD} = +2,5\text{ V}; V_{SS} = -2,5\text{ V} \\ V_{ref} = \pm 2048\text{ mV} \\ V_{DD} = +5\text{ V}; V_{SS} = -5\text{ V} \\ V_{ref} = \pm 4096\text{ mV} \end{array} \right.$
ON resistance unbalance	ΔR_{on}	—	400 200	— —	Ω Ω	5 10
						$\left\{ \begin{array}{l} V_{DD} = +2,5\text{ V}; V_{SS} = -2,5\text{ V} \\ V_{ref} = \pm 2048\text{ mV} \\ V_{DD} = +5\text{ V}; V_{SS} = -5\text{ V} \\ V_{ref} = \pm 4096\text{ mV} \end{array} \right.$

DIGITAL VOLTMETER DATA



From the graphs above it is clear that the accuracy of the system is optimum when $\pm V_{ref}$ is as close as possible to the supply voltage.

D.C. CHARACTERISTICS

V_{SS} = 0 V

parameter	V _{DD} V	symbol	T _{amb} (°C)						unit	conditions
			-40		+25		+85			
			min	max	min	max	min	max		
Quiescent device current	5 10	I _{DD}	-	50 100	-	50 100	-	375 750	μA μA	} all valid input combinations; V _I = V _{SS} or V _{DD}
Clock input voltage LOW	5 10	V _{IL}	-	0,2	-	0,2	-	V		
Clock input voltage HIGH	5 10	V _{IH}	4,8	-	4,8	-	4,8	-	V	
Reference voltage	V _{DD} V _{DD}	+V _{ref} -V _{ref}	↔	min 3 max V _{DD}	↔	min 3 max V _{DD}	↔	V	} +V _{ref} > -V _{ref}	
Chopper output LOW	V _{DD}	V _{CHL}	↔	min -1 max V _{DD} -3	↔	min -1 max V _{DD} -3	↔	V		
Chopper output HIGH	V _{DD}	V _{CHH}	↔	typ -V _{ref}	↔	typ -V _{ref}	↔	V		
Output (sink) current LOW	5 10	I _{OL}	2,4 4,8	-	2,0 4,0	-	1,6 3,2	-	mA mA	} V _O = 0,4 V; V _I = 0 or 5 V V _O = 0,5 V; V _I = 0 or 10 V
Output (source) current HIGH	5 10	I _{OH}	0,7 1,4	-	0,7 1,4	-	0,4 0,8	-	mA mA	

DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

HEF4750V

LSI

FREQUENCY SYNTHESIZER

The HEF4750V frequency synthesizer is one of a pair of LOC MOS devices, primarily intended for use in high-performance frequency synthesizers, e.g. in all communication, instrumentation, television and broadcast applications. A combination of analogue and digital techniques results in an integrated circuit that enables high performance. The complementary device is the universal divider type HEF4751V.

Together with a standard prescaler, the two LOC MOS integrated circuits offer low-cost single loop synthesizers with full professional performance. Salient features offered (in combination with HEF4751V) are:

- Wide choice of reference frequency using a single crystal.
- High-performance phase comparator — low phase noise — low spuri.
- System operation to > 1 GHz.
- Typical 15 MHz input at 10 V.
- Flexible programming:
 - frequency offsets
 - ROM compatible
 - fractional channel capability.
- Programme range $6\frac{1}{2}$ decades, including up to 3 decades of prescaler control.
- Division range extension by cascading.
- Built-in phase modulator.
- Fast lock feature.
- Out-of-lock indication.
- Low power dissipation and high noise immunity.

APPLICATION INFORMATION

Some examples of applications for the HEF4750V in combination with the HEF4751V are:

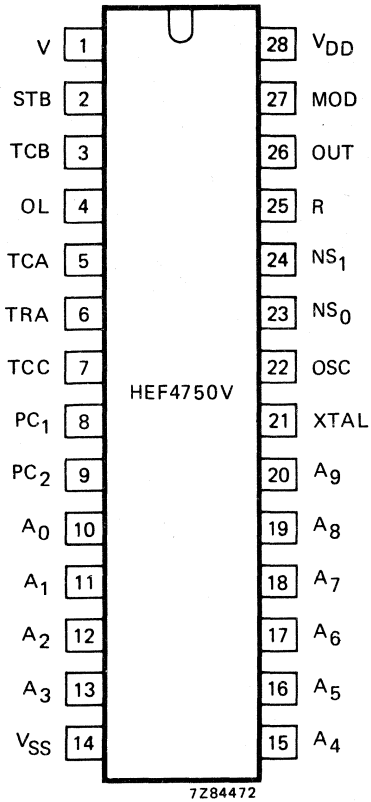
- VHF/UHF mobile radios.
- HF s.s.b. transceivers.
- Airborne and marine communications and nav aids.
- Broadcast transmitters.
- High quality radio and television receivers.
- High performance citizens band equipment.
- Signal generators.

SUPPLY VOLTAGE

rating	recommended operating
-0,5 to + 15	9,5 to 10,5 V



HEF4750V
LSI



PINNING

R	phase comparator input, reference
V	phase comparator input
STB	strobe input
TCA	timing capacitor C_A pin
TCB	timing capacitor C_B pin
TCC	timing capacitor C_C pin
TRA	biasing pin (resistor R_A)
PC ₁	analogue phase comparator output
PC ₂	digital phase comparator output
MOD	phase modulation input
OL	out-of-lock indication
OSC	reference oscillator/buffer input
XTAL	reference oscillator/buffer output
A ₀ to A ₉	programming inputs/programmable divider
NS ₀ , NS ₁	programming inputs, prescaler
OUT	reference divider output

Fig. 1 Pinning diagram.

HEF4750VD: 28-lead DIL; ceramic (SOT-135).

DEVELOPMENT SAMPLE DATA

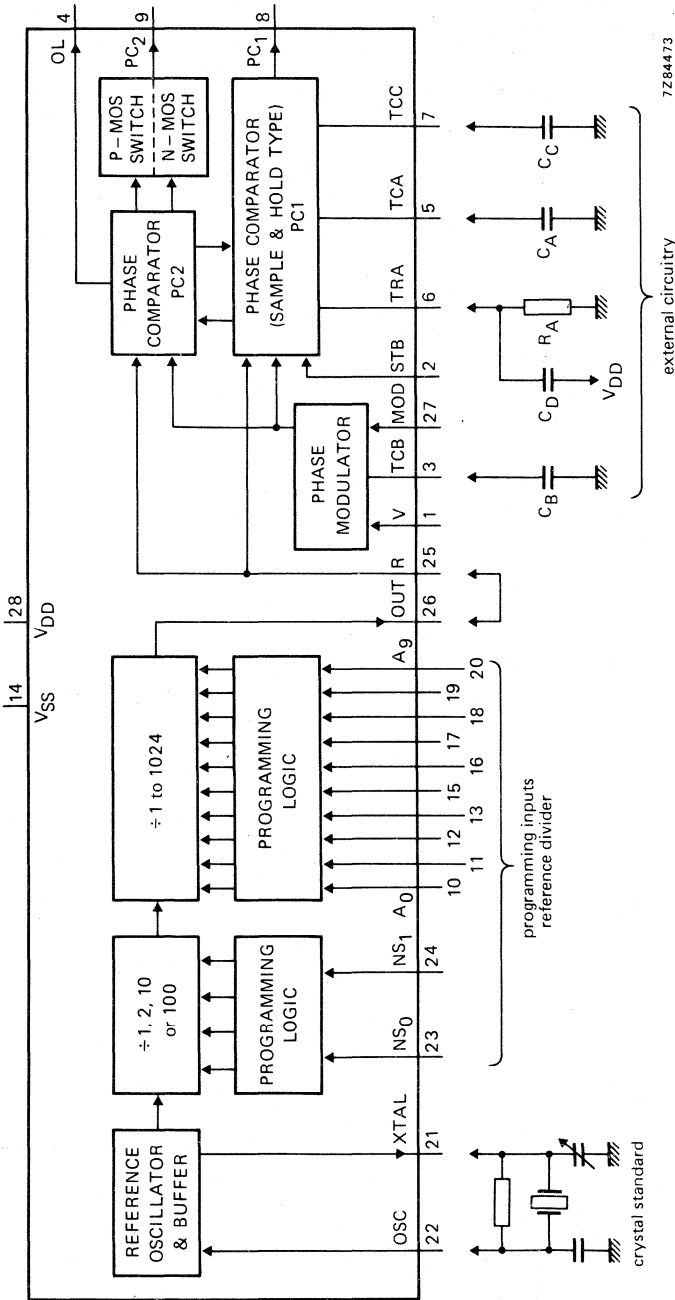


Fig. 2 Block diagram comprising five basic functions: phase comparator 1 (PC1), phase comparator 2 (PC2), phase modulator, reference oscillator and reference divider. These functions are described separately.

N.B. PC1 = analogue output; PC2 = 3-state output.

FUNCTIONAL DESCRIPTION

Phase comparator 1

Phase comparator 1 (PC1) is built around a SAMPLE and HOLD circuit. A negative-going transition at the V-input causes the hold capacitor (C_A) to be discharged and after a specified delay, caused by the Phase Modulator by means of an internal V' pulse, it produces a positive-going ramp. A negative-going transition at the R-input terminates the ramp. Capacitor C_A holds the voltage that the ramp has attained. Via an internal sampling switch this voltage is transferred to C_C and in turn buffered and made available at output PC_1 .

If the ramp terminates before an R-input is present, an internal end of ramp (EOR) signal is produced. These actions are illustrated in Fig. 3.

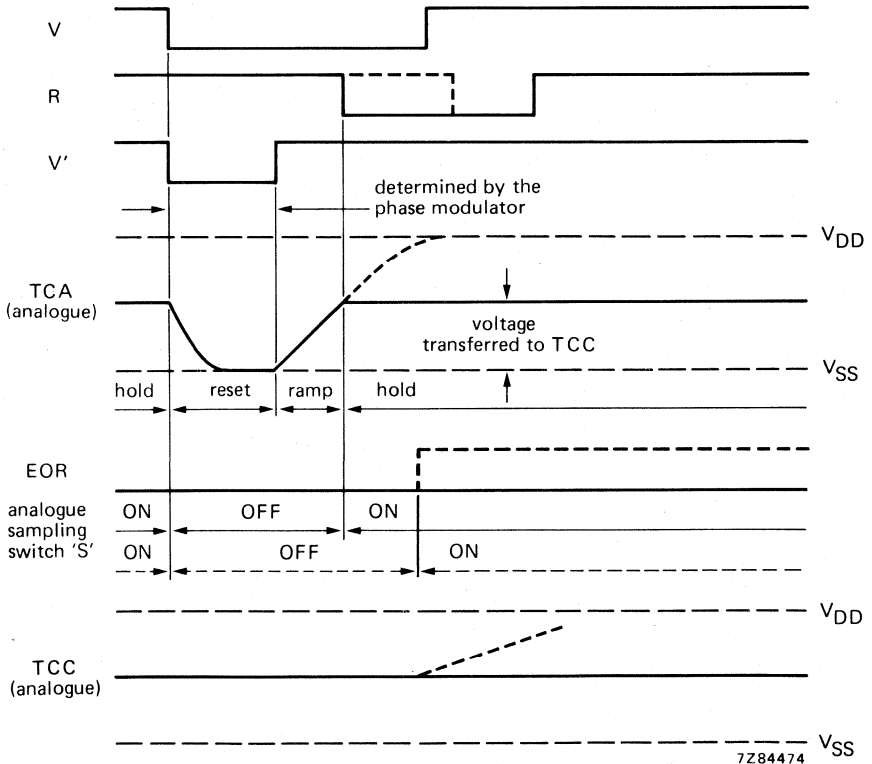


Fig. 3 Waveforms associated with PC1.

The resultant phase characteristic is shown in Fig. 4.

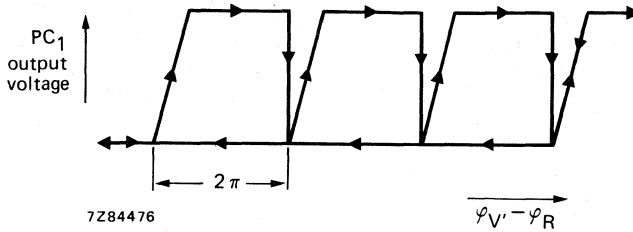


Fig. 4 Phase characteristic of PC1.

PC1 is designed to have a high gain, typically 3200 V/cycle (at 12,5 kHz). This enables a low noise performance.

Phase comparator 2

Phase comparator 2 (PC2) has a wide range, which enables faster lock times to be achieved than otherwise would be possible. It has a linear $\pm 360^\circ$ phase range, which corresponds to a gain of typically 5 V/cycle. This digital phase comparator has three stable states:

- reset state,
- V' leads R state,
- R leads V' state.

Conversion from one state to another takes place according to the state diagram of Fig. 5.

DEVELOPMENT SAMPLE DATA

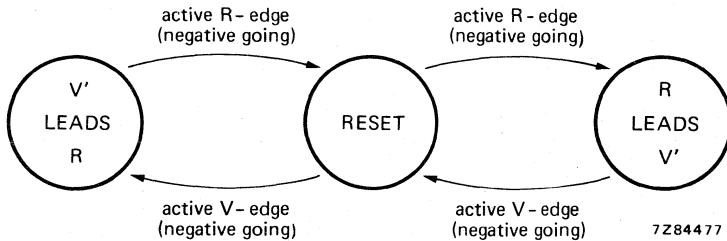


Fig. 5 State diagram of PC2.

Output PC₂ produces positive or negative-going pulses with variable width; they depend on the phase relationship of R and V'. The average output voltage is a linear function of the phase difference. Output PC₂ remains in the high impedance OFF-state in the region in which PC1 operates. The resultant phase characteristic is shown in Fig. 6.

FUNCTIONAL DESCRIPTION (continued)

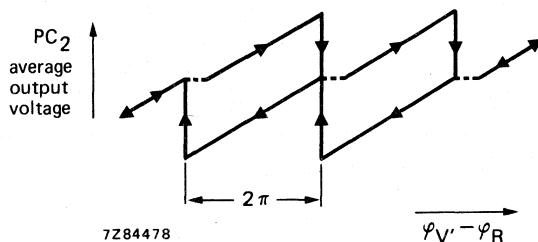


Fig. 6 Phase characteristic of PC₂.

Strobe function

The strobe function is intended for applications requiring extremely fast lock times. In normal operation the additional strobe input (STB) can be connected to the V-input and the circuit will function as described in the previous sections.

In single, phase-locked-loop type frequency synthesizers, the comparison frequency generally used is either the nominal channel spacing or a sub-multiple. PC₂ runs at the higher frequency (a higher reference frequency must also be used), whilst strobing takes place on the lower frequency, thereby obtaining a decrease in lock time. In a system using the Universal Divider HEF4751V, the output OFS cycles on the lower frequency, the output OFF cycles on the higher frequency.

Out-of-lock function

There are a number of situations in which the system goes from the locked to the out-of-lock state (OL goes HIGH):

1. When V' leads R, however out of the range of PC₁.
2. When R leads V'.
3. When an R-pulse is missing.
4. When a V-pulse is missing.
5. When two successive STB-commands occur, the first without corresponding V-signal.

Phase modulator

The phase modulator only uses one external capacitor, C_B at pin TCB. A negative-going transition at the V-input causes C_B to produce a positive-going linear ramp. When the ramp has reached a value almost equal to the modulation input voltage (at MOD), the ramp terminates, C_B discharges and a start signal to the C_A-ramp at TCA is produced. A linear phase modulation is reached in this way. If no modulation is required, the MOD-input must be connected to a fixed voltage of a certain positive value up to V_{DD}. Care must be taken that the V' pulse is never smaller than the minimum value to ensure that the external capacitor of PC₁ (C_A) can be discharged during that time. Since the V' pulse width is directly related to the TCB ramp duration, there is a requirement for the minimum value of this ramp duration.

Reference oscillator

The reference oscillator normally operates with an external crystal as shown in Fig. 2. The internal circuitry can be used as a buffer amplifier in case an external reference should be required.

Reference divider

The reference divider consists of a binary divider with a programmable division ratio of 1 to 1024 and a prescaler with selectable division ratios of 1, 2, 10 and 100, according to the following tables:

● Binary divider

N (A ₀ to A ₉)	division ratio
0	1024
0 ≤ N ≤ 1023	N

● Prescaler

programming word (NS ₀ , NS ₁)	division ratio
0	1
1	2
2	10
3	100

In this way suitable comparison frequencies can be obtained from a range of crystal frequencies. The divider can also be used as a 'stand alone' programmable divider by connecting input TRA to V_{DD}, which causes all internal analogue currents to be switched off.

Biasing circuitry

The biasing circuitry uses an external current source or resistor, which has to be connected between the TRA and V_{SS} pins. This circuitry supplies all analogue parts of the circuit. Consequently the analogue properties of the device, such as gain, charge currents, speed, power dissipation, impedance levels etc., are mainly determined by the value of the input current at TRA. The TRA input must be decoupled to V_{DD}, as shown in Fig. 7. The value of C_D has to be chosen such that the TRA input is 'clean', e.g. 10 nF at R_A = 68 kΩ.

DEVELOPMENT SAMPLE DATA

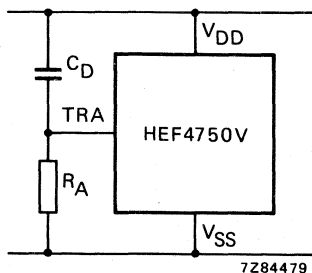


Fig. 7 Decoupling of input TRA.

HEF4750V

LSI

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{DD}	-0,5 to +15 V
Voltage on any input	V_I	-0,5 to $V_{DD} + 0,5$ V
D.C. current into any input or output	$\pm I$	max. 10 mA
Power dissipation per package for $T_{amb} = 0$ to +85 °C	P_{tot}	max. 500 mW
Power dissipation per output for $T_{amb} = 0$ to 85 °C	P	max. 100 mW
Storage temperature	T_{stg}	-65 to +150 °C
Operating ambient temperature	T_{amb}	-40 to +85 °C

D.C. CHARACTERISTICS at $V_{DD} = 10\text{ V} \pm 5\%$; voltages are referenced to $V_{SS} = 0\text{ V}$, unless otherwise specified; for definitions see note 1.

parameter	symbol	T_{amb} (°C)						unit	notes
		-40		+25		+85			
		min.	typ. max.	min.	typ. max.	min.	typ. max.		
Quiescent device current	I_{DD}	-	- 100	-	- 100	-	- 750	μA	2
Input current; logic inputs, MOD	$\pm I_{IN}$	-	- 300	-	- 300	-	- 1000	nA	3
Output leakage current at $\frac{1}{2} V_{DD}$									3, 4
TCA, hold-state	$\pm I_Z$	-	- 20	-	0,05 20	-	- 60	nA	
TCC, analogue switch OFF	$\pm I_Z$	-	- 20	-	0,05 20	-	- 60	nA	
PC ₂ , high impedance OFF-state	$\pm I_Z$	-	- 50	-	- 50	-	- 500	nA	
Logic input voltage LOW	V_{IL}	max. $0,3 V_{DD}$						V	
HIGH	V_{IH}	min. $0,7 V_{DD}$						V	
Logic output voltage LOW; at $ I_O < 1\ \mu\text{A}$	V_{OL}	-	- 50	-	- 50	-	- 50	mV	3
HIGH	V_{OH}	min. $V_{DD} - 50\text{ mV}$						mV	3
Logic output current LOW; at $V_{OL} = 0,5\text{ V}$									3
outputs OL, PC ₂ , OUT	I_{OL}	5,5	- -	4,6	- -	3,6	- -	mA	
output XTAL	I_{OL}	2,8	- -	2,4	- -	1,9	- -	mA	

DEVELOPMENT SAMPLE DATA

parameter	symbol	T _{amb} (°C)						unit	notes
		-40		+ 25		+ 85			
		min.	typ. max.	min.	typ. max.	min.	typ. max.		
Logic output current HIGH; at V _{OH} = V _{DD} - 0,5 V outputs OL, PC ₂ , OUT output XTAL	-I _{OH} -I _{OH}	1,5	- -	1,3	- -	1,0	- -	mA	3
Output TCC sink current	I _O	-	- -	-	2,1	-	- -	mA	3,4,5
Output TCC source current	-I _O	-	- -	-	1,9	-	- -	mA	3,4,6
Internal resistance of TCC output swing ≤ 200 mV specified output range: 0,3 V _{DD} to 0,7 V _{DD}	R _i	-	- -	-	0,7	-	- -	kΩ	3,4
Output TCC voltage with respect to TCA input voltage	ΔV	-	0 -	-	0 -	-	0 -	V	3,4,7
Output PC ₁ sink current	I _O	-	- -	-	1,1	-	- -	mA	3,4,8
Output PC ₁ source current	-I _O	-	- -	-	1,0	-	- -	mA	3,4,9
Internal resistance of PC ₁ output swing ≤ 200 mV specified output range: 0,3 V _{DD} to 0,7 V _{DD}	R _i	-	- -	-	1,4	-	- -	kΩ	3,4
Output PC ₁ voltage with respect to TCC input voltage	ΔV	-	0 -	-	0 -	-	0 -	V	3,4,10
EOR generation V _{EOR} = V _{DD} - V _{TCA}	V _{EOR}	-	0,9 -	-	0,7 -	-	0,6 -	V	3,4,11
Source current; HIGH at V _{OUT} = ½ V _{DD} ; output in ramp mode									3,4
TCA	I _O	-	- -	-	13	-	- -	mA	
TCB	I _O	-	- -	-	2,5	-	- -	mA	

A.C. CHARACTERISTICS

General note

The dynamic specifications are given for the circuit built-up with external components as given in Fig. 8, under the following conditions; for definitions see note 1; for definitions of times see Fig. 19; $V_{DD} = 10 \text{ V} \pm 5\%$; $T_{amb} = 25 \text{ }^\circ\text{C}$; input transition times $\leq 20 \text{ ns}$; $R_A = 68 \text{ k}\Omega \pm 30\%$ (see also note 4); $C_A = 270 \text{ pF}$; $C_B = 150 \text{ pF}$; $C_C = 1 \text{ nF}$; $C_D = 10 \text{ nF}$; unless otherwise specified.

	symbol	min.	typ.	max.	unit	conditions	notes
Slew rate							
TCA	STCA	—	52	—	V/ μ s	$R_A = \text{minimum}$	12
TCA	STCA	—	28	—	V/ μ s	$R_A = \text{maximum}$	12
TCB	STCB	—	20	—	V/ μ s	$R_A = \text{minimum}$	12
TCB	STCB	—	10	—	V/ μ s	$R_A = \text{maximum}$	12
Ramp linearity							
TCA	lTCA	—	2	—	%		13
TCB	lTCB	—	2	—	%		13
Start of TCA-ramp delay	tBCA	—	200	—	ns		
Delay of TCA-hold	tRCA	—	40	—	ns		
Delay of TCA-discharge	tVCA	—	60	—	ns		
Start of TCB-ramp delay	tVCB	—	60	—	ns		
TCB-ramp duration	t _{rCB}	—	250	—	ns	$V_{MOD} = 4 \text{ V}$	
	t _{rCB}	—	350	—	ns	$V_{MOD} = 6 \text{ V}$	
	t _{rCB}	—	450	—	ns	$V_{MOD} = 8 \text{ V}$	
Required TCB min. ramp duration	t _{rCB}	—	150	—	ns		14
Pulse width							
V : LOW	tpWVL	—	20	—	ns		
V : HIGH	tpWVH	—	20	—	ns		
R : LOW	tpWRL	—	20	—	ns		
R : HIGH	tpWRH	—	20	—	ns		
STB : LOW	tpWSL	—	20	—	ns		
STB : HIGH	tpWSH	—	20	—	ns		
Fall time							
TCA	t _{fCA}	—	50	—	ns		
TCB	t _{fCB}	—	50	—	ns		
Prescaler input frequency	fPR	—	30	—	MHz	all division ratios	
Binary divider frequency	fDIV	—	30	—	MHz	all division ratios	
Crystal oscillator frequency	fOSC	—	10	—	MHz		
Average power supply current						locked state	
with speed-up 1 : 10	I _p	—	3,6	—	mA		15
without speed-up	I _p	—	3,2	—	mA		16

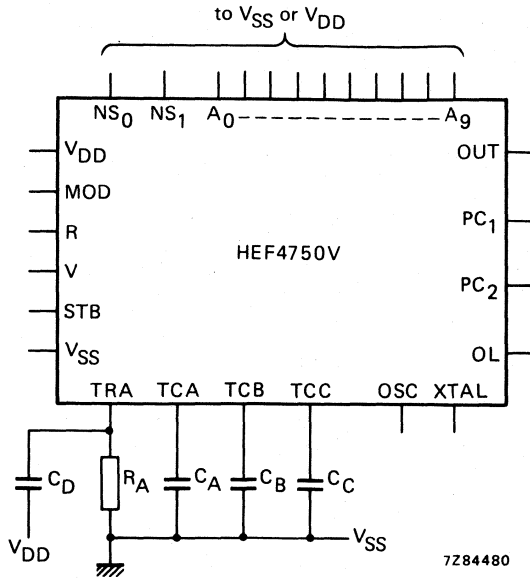


Fig. 8 Test circuit for measuring a.c. characteristics.

NOTES

1. Definitions:

- RA = external biasing resistor between pins TRA and VSS; 68 kΩ ± 30%.
- CA = external timing capacitor for time/voltage converter, between pins TCA and VSS.
- CB = external timing capacitor for phase modulator, between pins TCB and VSS.
- CC = external hold capacitor between pins TCC and VSS.
- CD = decoupling capacitor between pins TRA and VDD.

Logic inputs: V, R, STB, A0 to A9, NS0, NS1, OSC.

Logic outputs: OL, PC2, XTAL, OUT.

Analogue signals: TCA, TCB, TCC, TRA, PC1, MOD.

- 2. TRA at VDD; TCA, TCB, TCC and MOD at VSS; logic inputs at VSS or VDD.
- 3. All logic inputs at VSS or VDD.
- 4. RA connected; its value chosen such that ITRA = 100 μA.
- 5. The analogue switch is in the ON position (see Fig. 9).

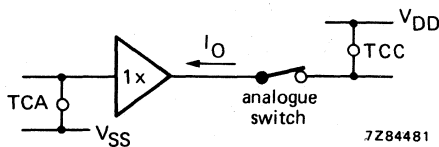


Fig. 9 Equivalent circuit for note 5.

DEVELOPMENT SAMPLE DATA

NOTES (continued)

6. The analogue switch is in the ON position (see Fig. 10).

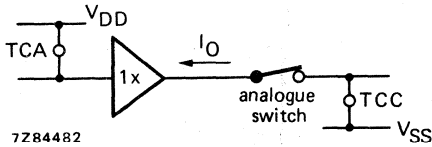


Fig. 10 Equivalent circuit for note 6.

7. This guarantees the d.c. voltage gain, combined with d.c.-offset.

Input condition: $0,3 V_{DD} \leq V_{TCA} \leq 0,7 V_{DD}$.
 $\Delta V = V_{TCC} - V_{TCA}$.

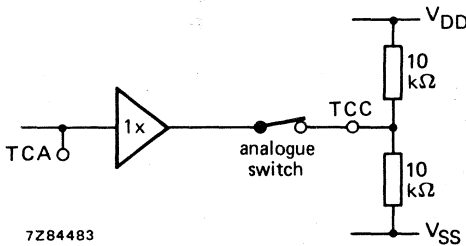


Fig. 11 Circuit for note 7.

- 8.

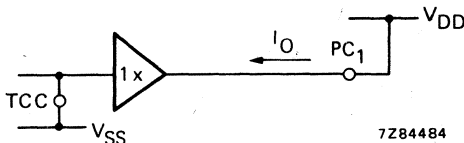


Fig. 12 Equivalent circuit for PC₁ sink current.

- 9.

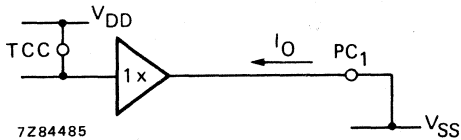


Fig. 13 Equivalent circuit for PC₁ source current.

10. This guarantees the d.c. voltage gain, combined with d.c.-offset.

Input condition: $0,3 V_{DD} \leq V_{TCC} \leq 0,7 V_{DD}$.
 $\Delta V = V_{PC1} - V_{TCC}$.

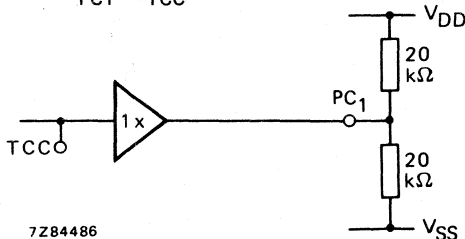


Fig. 14 Circuit for note 10.

11. Switching level at TCA, generating an EOR-signal, during increasing input voltage.
- 12.

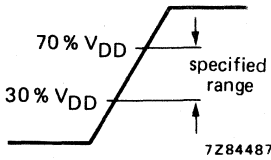


Fig. 15 Waveform at the output.

13. Definition of the ramp linearity at full swing.

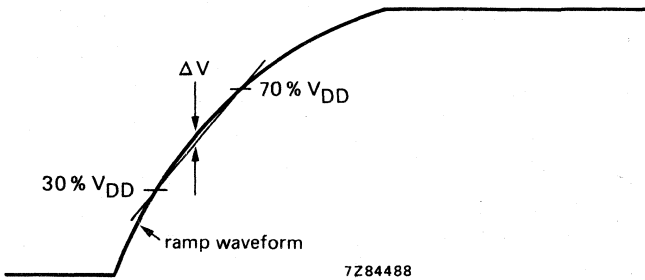


Fig. 16 ΔV is the maximum deviation of the ramp waveform to the straight line, which joins the $30\% V_{DD}$ and $70\% V_{DD}$ points.

$$\text{Linearity} = \frac{\Delta V}{\frac{1}{2} V_{DD}} \times 100\%.$$

14. The external components and modulation input voltage must be chosen such that this requirement will be fulfilled, to ensure that C_A is sufficiently discharged during that time.

DEVELOPMENT SAMPLE DATA

NOTES (continued)

15. Circuit connections for power supply current specification, with speed-up 1 : 10. V and R are in the range of PC₁, such that the output voltage at PC₁ is equal to 5 V.

$f_{OSC} = 5 \text{ MHz}$ (external clock)

$f_{STB} = 12,5 \text{ kHz}$

$f_V = 125 \text{ kHz}$

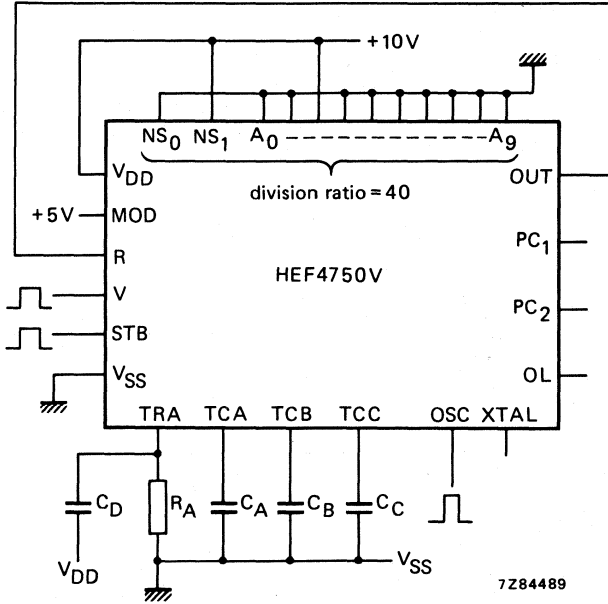


Fig. 17 Circuit for note 15.

16. Circuit connections for power supply current specification, without speed-up. V and R are in the range of PC1, such that the output voltage at PC1 is equal to 5 V.
 $f_{OSC} = 5 \text{ MHz}$ (external clock)
 $f_{STB} = 12,5 \text{ kHz}$
 $f_V = 12,5 \text{ kHz}$

DEVELOPMENT SAMPLE DATA

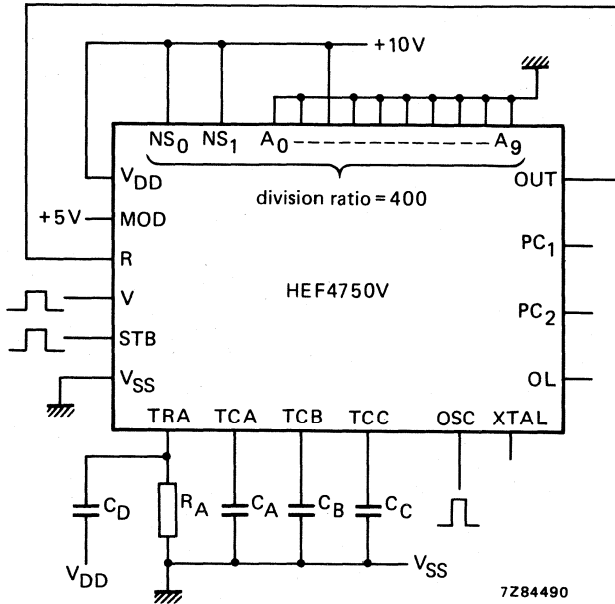
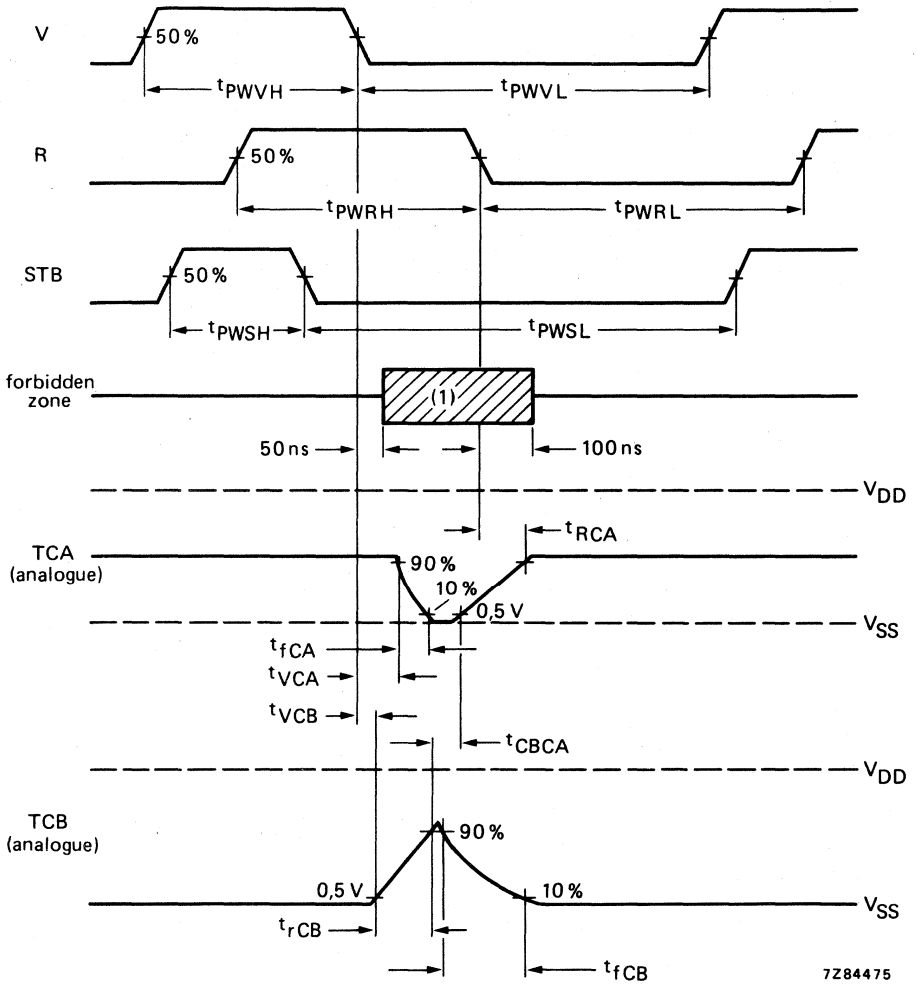


Fig. 18 Circuit for note 16.



7284475

(1) Forbidden zone in the *locked state* for the positive edge of V and R and both edges of STB.

Fig. 19 Waveforms showing times in the locked state.

DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

HEF4751V

LSI

UNIVERSAL DIVIDER

The HEF4751V is a universal divider (U.D.) intended for use in high performance phase lock loop frequency synthesizer systems. It consists of a chain of counters operating in a programmable feedback mode. Programmable feedback signals are generated for up to three external (fast) $\div 10/11$ prescaler.

The system comprising one HEF4751V U.D. together with prescalers is a fully programmable divider with a maximum configuration of: 5 decimal stages, a programmable mode M stage ($1 \leq M \leq 16$, non-decimal fraction channel selection), and a mode H stage ($H = 1$ or 2 , stage for half channel offset). Programming is performed in BCD code in a bit-parallel, digit-serial format.

To accommodate fixed or variable frequency offset, two numbers are applied in parallel, one being subtracted from the other to produce the internal programme.

The decade selection address is generated by an internal programme counter which may run continuously or on demand. Two or more universal dividers can be cascaded, each extra U.D. (in slave mode) adds two decades to the system. The combination retains the full programmability and features of a single U.D. The U.D. provides a fast output signal FF at output OFF, which can have a phase jitter of ± 1 system input period, to allow fast frequency locking. The slow output signal FS at output OFS, which is jitter-free, is used for fine phase control at a lower speed.

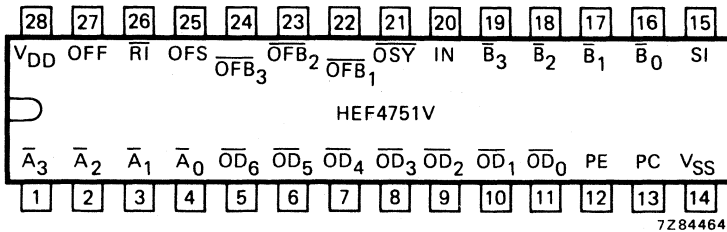


Fig. 1 Pinning diagram.

SUPPLY VOLTAGE

rating	recommended operating
-0,5 to +18	4,5 to 12,5 V

HEF4751VP: 28-lead DIL; plastic (SOT-117).
HEF4751VD: 28-lead DIL; ceramic (SOT-135).

FAMILY DATA

I_{DD} LIMITS category LSI

} see Family Specifications

HEF4751V

LSI

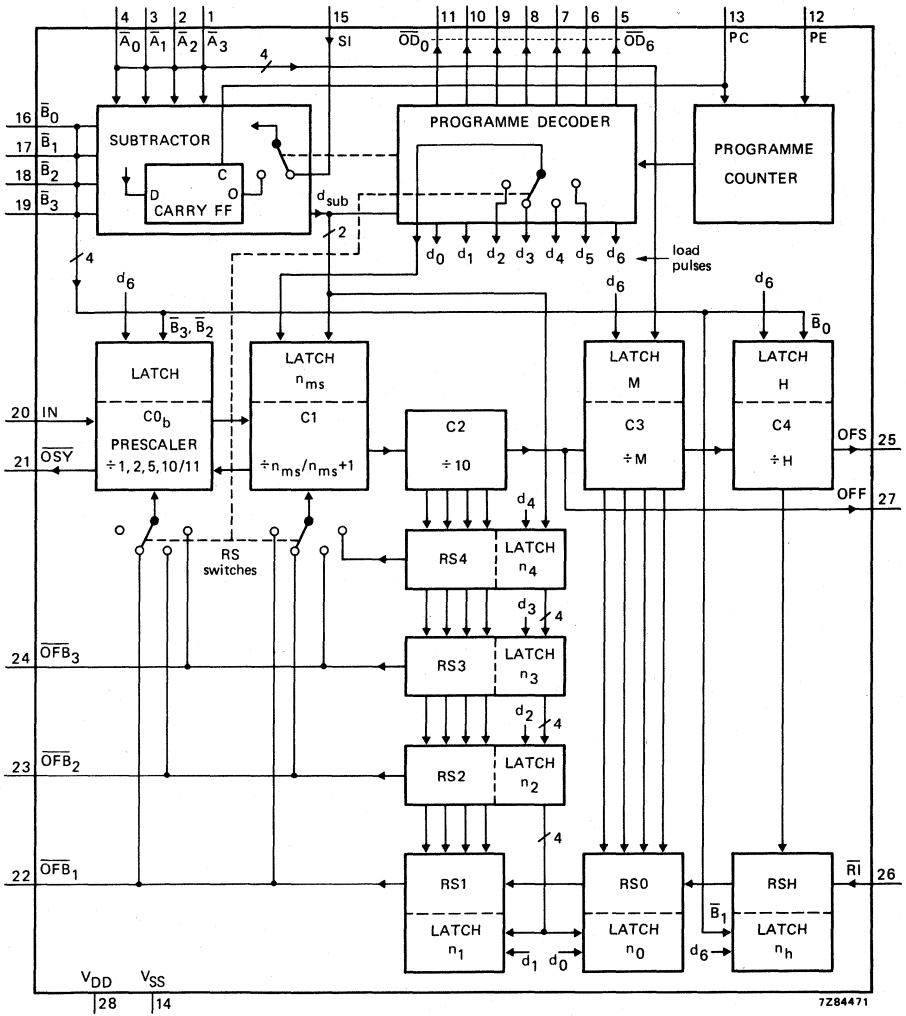


Fig. 2 Block diagram.

DEVELOPMENT SAMPLE DATA

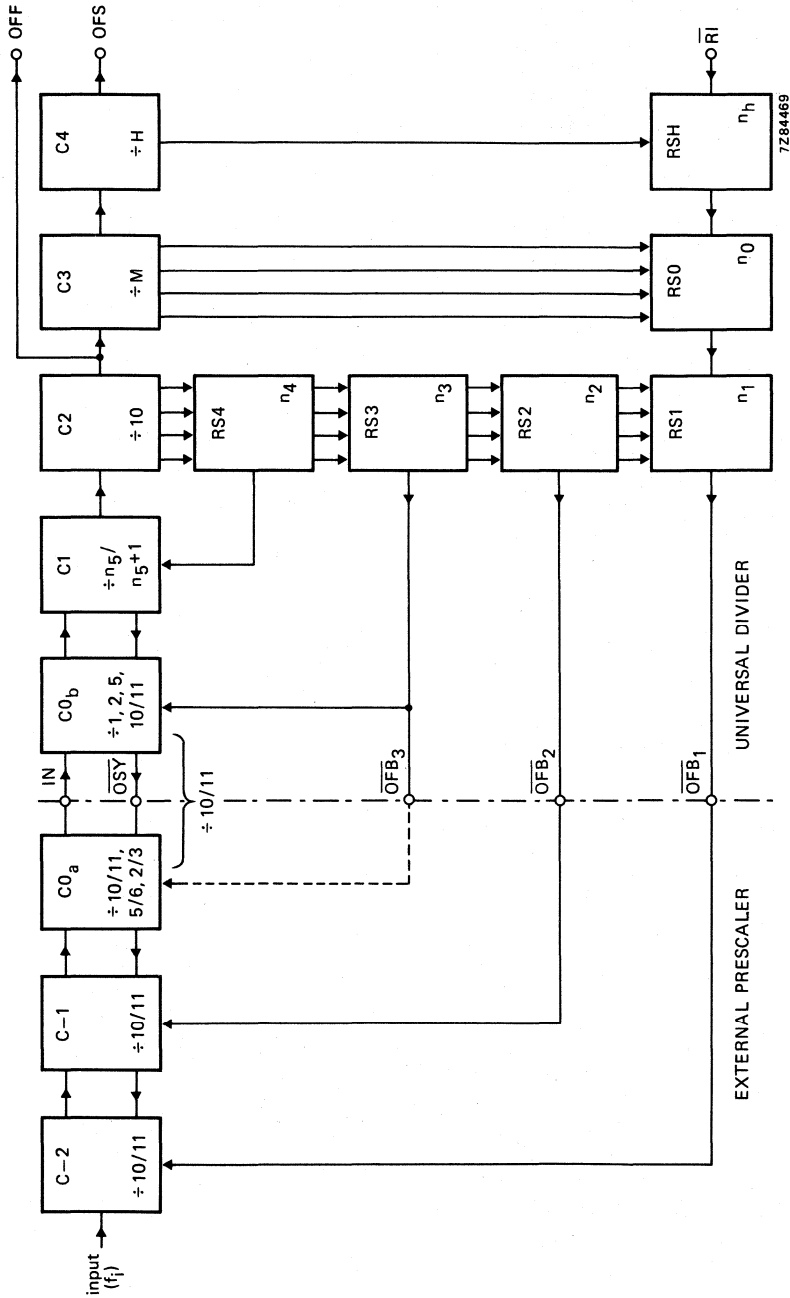
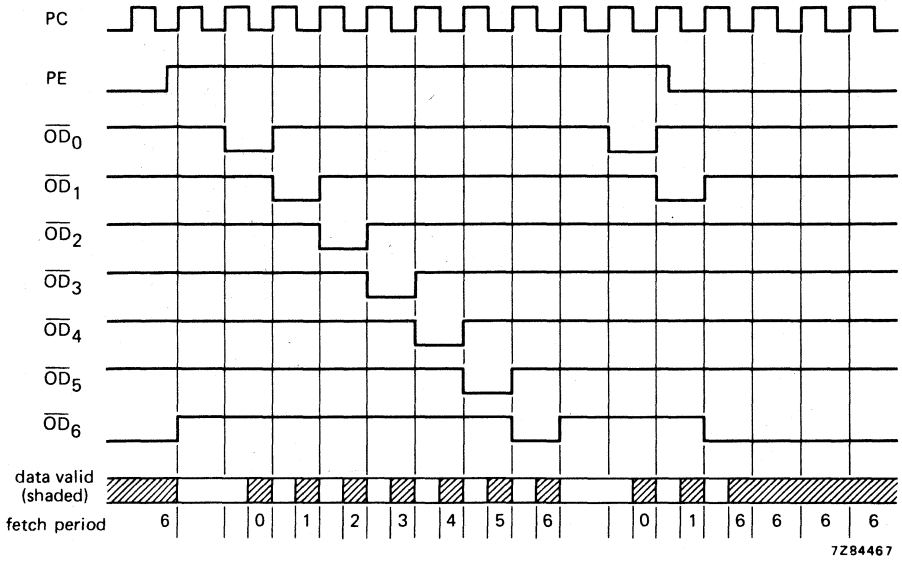


Fig. 3 The HEF4751V U.D. used in a system with 3 (fast) prescalers.
 $1 \leq M \leq 16; 1 \leq H \leq 2; n_5 > 0; f_i/f_{OFS} = \{(n_5 \cdot 10^4 + n_4 \cdot 10^3 + n_3 \cdot 10^2 + n_2 \cdot 10 + n_1) M + n_0\} H + n_h$.



7284467

Fig. 4 Timing diagram showing programme data inputs.

Allocation of data input

fetch period	inputs								
	\overline{A}_3	\overline{A}_2	\overline{A}_1	\overline{A}_0	\overline{B}_3	\overline{B}_2	\overline{B}_1	\overline{B}_0	SI
0		$n0A$				$n0B$			b_{in}
1		$n1A$				$n1B$			X
2		$n2A$				$n2B$			X
3		$n3A$				$n3B$			X
4		$n4A$				$n4B$			X
5		$n5A$				$n5B$			X
6		M			CO_b control		$\frac{1}{2}$ channel control		X

Allocation of data input \overline{B}_3 to \overline{B}_0 during fetch period 6

\overline{B}_3	\overline{B}_2	CO_b division ratio	\overline{B}_1	\overline{B}_0	$\frac{1}{2}$ channel configuration
L	L	1	L	L	H = 1
L	H	2	L	H	H = 2; $n_h = 0$
H	L	5	H	H	H = 2; $n_h = 1$
H	H	10/11	H	L	test state

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

PROGRAMME DATA INPUT (see also Figs 3 and 4)

The programming process is timed and controlled by input PC and PE. When the programme enable (PE) input is HIGH, the positive edges of the programme clock (PC) signal step through the internal programme counter in a sequence of 8 states. Seven states define fetch periods, each indicated by a LOW signal at one of the corresponding data address outputs (\overline{OD}_0 to \overline{OD}_6). These data address signals may be used to address the external programme source. The data fetched from the programme source is applied to inputs \overline{A}_0 to \overline{A}_3 and \overline{B}_0 to \overline{B}_3 . When PC is LOW in a fetch period an internal load pulse is generated, the data is valid during this time and has to be stable. When PE is LOW, the programming cycle is interrupted on the first positive edge of PC. On the next negative edge at input PC fetch period 6 is entered. Data may enter asynchronously in fetch period 6.

Ten blocks in the U.D. need programme input signals (see Fig. 2). Four of these (CO_b , C3, C4 and RSH) are concerned with the configuration of the U.D. and are programmed in fetch period 6. The remaining blocks (RS0 to RS4 and C1) are programmed with number P, consisting of six internal digits n_0 to n_5 .

$$P = (n_5 \cdot 10^4 + n_4 \cdot 10^3 + n_3 \cdot 10^2 + n_2 \cdot 10 + n_1) \cdot M + n_0$$

These digits are formed by a subtractor from two external numbers A and B and a borrow-in (b_{in}).

$$P = A - B - b_{in} \text{ or if this result is negative; } P = A - B - b_{in} + M \cdot 10^5.$$

The numbers A and B, each consisting of six four bit digits n_{0A} to n_{5A} and n_{0B} to n_{5B} , are applied in fetch period 0 to 5 to the inputs \overline{A}_0 to \overline{A}_3 (data A) and \overline{B}_0 to \overline{B}_3 (data B) in binary coded negative logic.

$$A = (n_{5A} \cdot 10^4 + n_{4A} \cdot 10^3 + n_{3A} \cdot 10^2 + n_{2A} \cdot 10 + n_{1A}) \cdot M + n_{0A}$$

$$B = (n_{5B} \cdot 10^4 + n_{4B} \cdot 10^3 + n_{3B} \cdot 10^2 + n_{2B} \cdot 10 + n_{1B}) \cdot M + n_{0B}$$

Borrow-in (b_{in}) is applied via input SI in fetch period 0 (SI = HIGH: borrow, SI = LOW: no borrow).

Counter C1 is automatically programmed with the most significant non-zero digit (n_{m5}) from the internal digits n_5 to n_2 of number P. The counter chain C - 2 to C1 (see Fig. 3) is fully programmable by the use of pulse rate feedback.

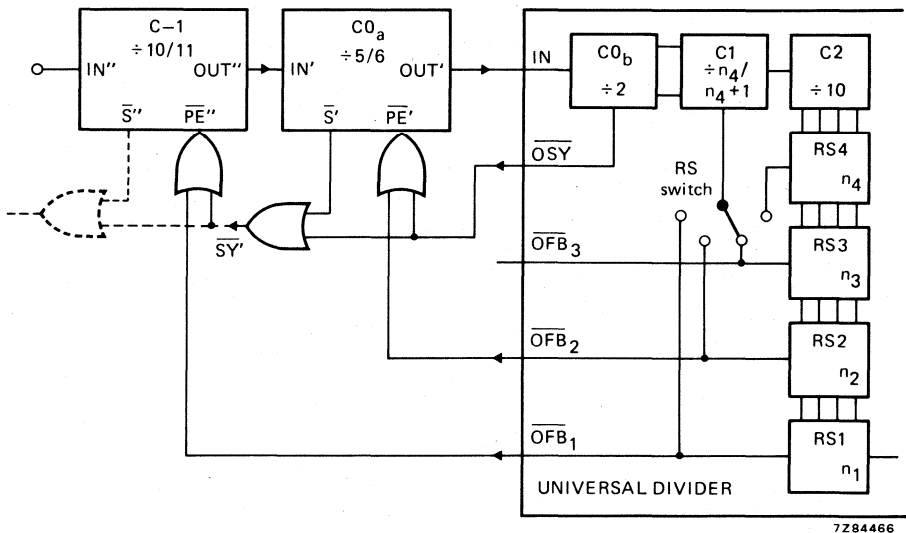
Rate feedback is generated by the rate selectors RS4 to RS0 and RSH, which are programmed with digits n_4 to n_0 and n_h respectively. In fetch period 6 the fractional counter C3, half channel counter C4 and CO_b are programmed and configured via data B inputs. Counter C3 is programmed in fetch period 6 via data A inputs in negative logic (except all HIGH is understood as: $M = 16$). The counter C0 is a side steppable 10/11 counter composed of an internal part CO_b and an external part CO_a . CO_b is configured via \overline{B}_3 and \overline{B}_2 to a division ratio of 1 or 2 or 5 or 10/11; CO_a must have the complementary ratio 10/11 or 5/6 or 2/3 or 1 respectively. In the latter case CO_b comprises the whole C0 counter with internal feedback, CO_a is then not required.

The half channel counter C4 is enabled with $\overline{B}_0 = \text{HIGH}$ and disabled with $\overline{B}_0 = \text{LOW}$. With C4 enabled, a half channel offset can be programmed with input $\overline{B}_1 = \text{HIGH}$, and no offset with $\overline{B}_1 = \text{LOW}$.

FEEDBACK TO PRESCALERS (see also Figs 5 and 6)

The counters C1, C0, C-1 and C-2 are side-steppable counters, i.e. its division ratio may be increased by one, by applying a pulse to a control terminal for the duration of one division cycle. Counter C2 has 10 states, which are accessible as timing signals for the rate selectors RS1 to RS4. A rate selector, programmed with n (n_1 to n_4 in the U.D.) generates n of 10 basic timing periods an active signal. Since $n \leq 9$, 1 of 10 periods is always non-active. In this period RS1 transfers the output of rate selector RS0, which is timed by counter C3 and programmed with n_0 . Similarly, RS0 transfers RSH output during one period of C3. Rate selector RSH is timed by C4 and programmed with n_h . In one of the two states of C4, if enabled, or always, if C4 is disabled, RSH transfers the LOW active signal at input \overline{RI} to RS0. If \overline{RI} is not used it must be connected to HIGH. The feedback output signals of RS1, RS2 and RS3 are externally available as active LOW signals at outputs \overline{OFB}_1 , \overline{OFB}_2 and \overline{OFB}_3 .

Output \overline{OFB}_1 is intended for the prescaler at the highest frequency (if present), \overline{OFB}_2 for the next (if present) and \overline{OFB}_3 for the lowest frequency prescaler (if present). A prescaler needs a feedback signal, which is timed on one of its own division cycles in a basic timing period. The timing signal at \overline{OSY} is LOW during the last U.D. input period of a basic timing period and is suitable for timing of the feedback for the last external prescaler. The synchronization signal for a preceding prescaler is the OR-function of the sync. input and sync. output of the following prescaler (all sync. signals active LOW).



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Fig. 5 Block diagram showing feedback to prescalers.

DEVELOPMENT SAMPLE DATA

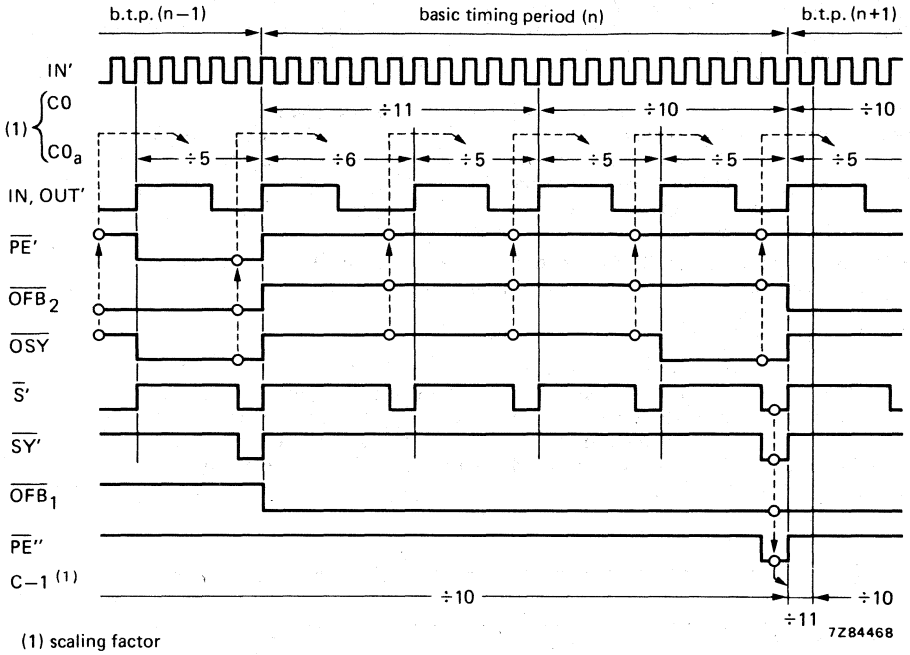


Fig. 6 Timing diagram showing signals occurring in Fig. 5.

CASCADING OF U.D.s (see also Fig. 8)

A U.D. is programmed into the 'slave' mode by the programme input data: $n_{2A} = 11$, $n_{2B} = 10$, $n_{3A} = n_{4A} = n_{3B} = n_{4B} = n_{5B} = 0$. A U.D. operating in the slave mode performs the function of two extra programmable stages C2' and C3' to a 'master' (not slave) mode operating U.D. More slave U.D.s may be used, every slave adding two lower significant digits to the system.

Output \overline{OFB}_3 is converted to the borrow output of the programme data subtractor, which is valid after fetch period 5. Input SI is the borrow input (both in master and in slave mode), which has to be valid in fetch period 0. Input SI has to be connected to output \overline{OFB}_3 of a following slave, if not present, to LOW. For proper transfer of the borrow from a lower to a higher significant U.D. subtractor, the U.D.s have to be programmed sequentially in order of significance or synchronously if the programme is repeated at least the number of U.D.s in the system.

Rate input \overline{RI} and output OFS must be connected to rate output \overline{OFB}_1 and the input IN of the next slave U.D. The combination thus formed retains the full programmability and features of one U.D.

OUTPUT (see also Fig. 7)

The normal output of the U.D. is the slow output OFS, which consists of evenly spaced LOW pulses. This output is intended for accurate phase comparison. If a better frequency acquisition time is required, the fast output OFF can be used. The output frequency on OFF is a factor $M \cdot H$ higher than the frequency on OFS. However, phase jitter of maximum ± 1 system input period occurs at OFF, since the division ratio of the counters preceding OFF are varied by slow feedback pulse trains from rate selectors following OFF.

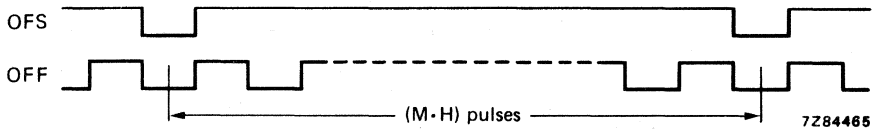


Fig. 7 Timing diagram showing output pulses.

DEVELOPMENT SAMPLE DATA

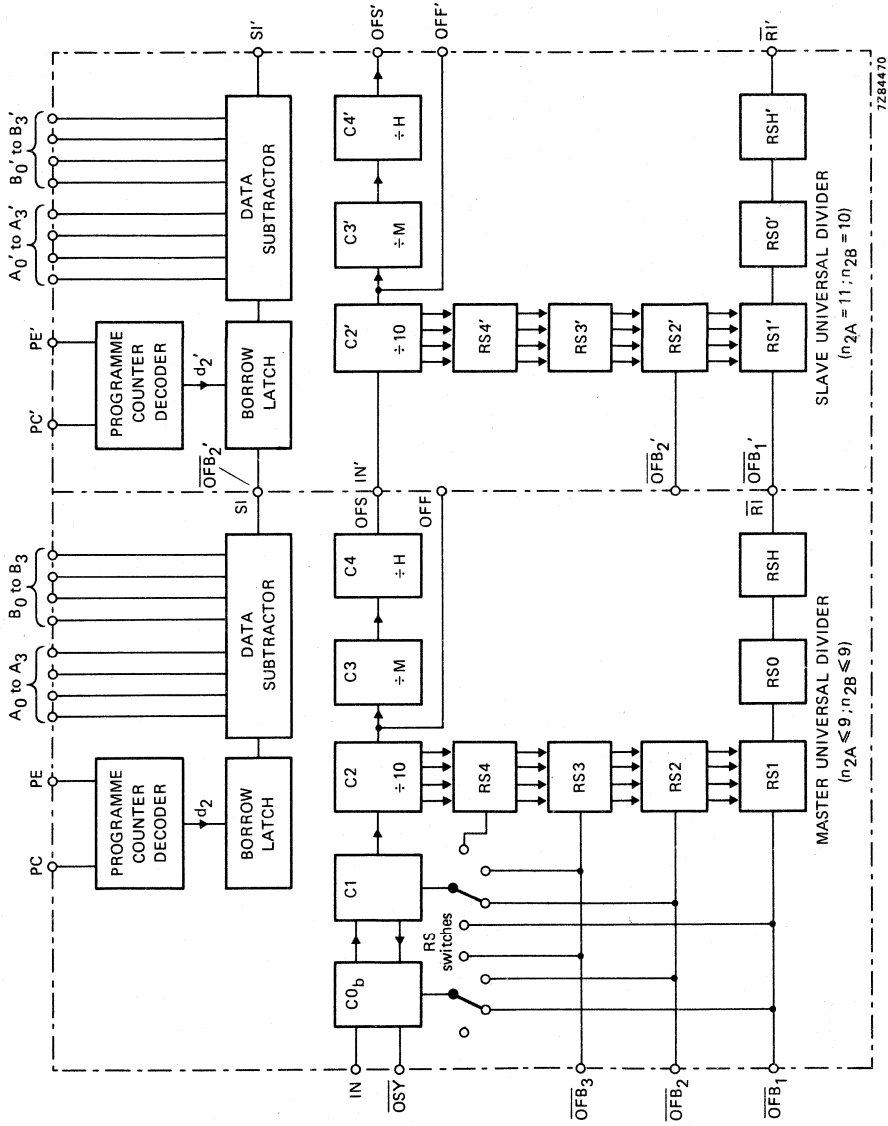


Fig. 8 Block diagram showing cascading of U.D.s.

D.C. CHARACTERISTICS $V_{SS} = 0$ V

	V_{DD} V	V_{OH} V	V_{OL} V	symbol	T_{amb} (°C)					
					-40		+25		+85	
					min.	max.	min.	max.	min.	max.
Output (sink) current LOW	4,75		0,4	I_{OL}	1,6		1,4		1,3	mA
	5		0,4		1,7		1,5		1,4	mA
	10		0,5		2,9		2,7		2,6	mA
Output (source) current HIGH	5	4,6		$-I_{OH}$	1,0		0,85		0,65	mA
	5	2,5			3,0		2,5		2,0	mA
	10	9,5			3,0		2,5		2,0	mA

A.C. CHARACTERISTICS

 $V_{SS} = 0$ V; $T_{amb} = -40$ to $+85$ °C; input transition times ≤ 20 ns

	V_{DD} V	symbol	min.	typ.	max.	
Propagation delay $IN \rightarrow \overline{OSY}$ HIGH to LOW	10	t_{PHL}		50		ns
Maximum input frequency	10	f_{IN}		15		MHz C_{0b} ratio > 1
Maximum input frequency	10	f_{IN}		7,5		MHz C_{0b} ratio = 1

DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

HEF4752V

LSI

A.C. MOTOR CONTROL CIRCUIT

The HEF4752V is a circuit for a.c. motor speed control utilizing LOC MOS technology. The circuit synthesizes three 120° out of phase signals, of which the average voltage varies sinusoidally with time in the frequency range 0 to 200 Hz. The method employed is based upon the pulse width modulation principle, in order to achieve a sufficient accuracy of the output voltages over the whole frequency range. A pure digital waveform generation is used.

All outputs are of the push-pull type. Inputs and outputs are protected against electrostatic effects in a wide variety of device-handling situations. However, to be totally safe, it is desirable to take handling precautions into account.

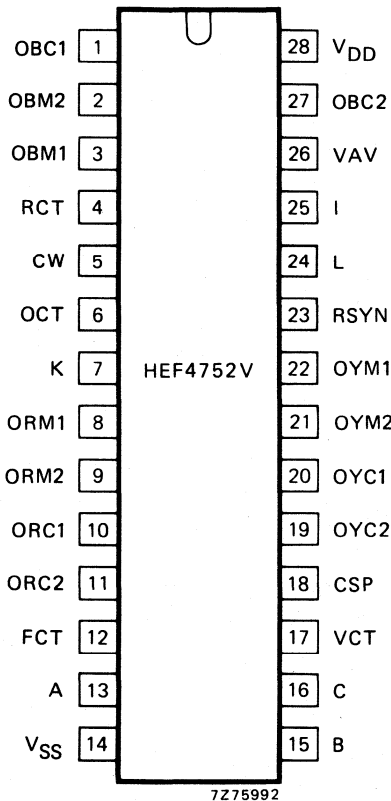


Fig. 1 Pinning diagram.

HEF4752VP: 28-lead DIL; plastic (SOT-117).
HEF4752VD: 28-lead DIL; ceramic (SOT-135).

PINNING

Inputs; group I

- 24 = L data
- 25 = I data
- 7 = K data
- 5 = CW data
- 13 = A data
- 15 = B data
- 16 = C data

Inputs; group II

- 12 = FCT frequency clock
- 17 = VCT voltage clock
- 4 = RCT reference clock
- 6 = OCT output delay clock

Outputs; group I

- 23 = RSYN R-phase synchronization
- 26 = VAV average voltage
- 18 = CSP current sampling pulses

Outputs; group II

- 8 = ORM1 R-phase main
- 9 = ORM2 R-phase main
- 10 = ORC1 R-phase commutation
- 11 = ORC2 R-phase commutation
- 22 = OYM1 Y-phase main
- 21 = OYM2 Y-phase main
- 20 = OYC1 Y-phase commutation
- 19 = OYC2 Y-phase commutation
- 3 = OBM1 B-phase main
- 2 = OBM2 B-phase main
- 1 = OBC1 B-phase commutation
- 27 = OBC2 B-phase commutation

SUPPLY VOLTAGE

	rating	recommended operating
HEF4752V	-0,5 to 18	4,5 to 12,5 V

FAMILY DATA see Family Specifications

D.C. CHARACTERISTICS $V_{SS} = 0\text{ V}$

parameter	V_{DD} V	symbol	T_{amb} (°C)			unit	conditions
			-40 min.	+25 min. max.	+85 min. max.		
Quiescent device current	5 10	I_{DD}	— —	— —	— —	μA μA	all valid input combinations; $V_I = V_{SS}$ or V_{DD} $V_O = 0$ or 10 V
Input leakage current	10	$\pm I_{IN}$	—	0,3	1	μA	
Input voltage HIGH	5 10	V_{IH}	3,5 7,0	— —	— —	V V	inputs: group I
Input voltage LOW	5 10	V_{IL}	— —	1,5 3,0	— —	V V	
Output voltage HIGH	5 10	V_{OH}	4,95 9,95	— —	— —	V V	$V_I = V_{SS}$ or V_{DD} ; $ I_O < 1\ \mu\text{A}$
Output voltage LOW	5 10	V_{OL}	— —	0,05 0,05	— —	V V	
Input tripping level; input voltage increasing	5 10	V_{ti}	1,5 3,0	4,0 8,0	1,5 3,0	V V	inputs: group II
Input tripping level; input voltage decreasing	5 10	V_{td}	1,0 2,0	3,5 7,0	1,0 2,0	V V	
Output current LOW	5 10	I_{OL}	0,45 1,4	— —	0,3 —	mA mA	$V_{OH} = 0,4\text{ V}$ } outputs: groups I and II
Output current HIGH	5 10	$-I_{OH}$	0,3 0,9	— —	0,9 —	mA mA	
Output current HIGH	5 10	$-I_{OH}$	0,9 —	— —	0,6 —	mA mA	$V_{OH} = 4,6\text{ V}$ } outputs: group I
Output current HIGH	5 10	$-I_{OH}$	0,6 1,8	— —	0,6 —	mA mA	
Output current HIGH	5	$-I_{OH}$	1,8	—	1,2	mA	$V_{OH} = 9,5\text{ V}$ } outputs: group I $V_{OH} = 2,5\text{ V}$; outputs: group I $V_{OH} = 4,6\text{ V}$ } outputs: group II $V_{OH} = 9,5\text{ V}$ } outputs: group II
Total supply current	10	I_{tot}	—	typ.2	—	mA	

APPLICATION INFORMATION

Figure 2 shows the functional block diagram of a 3-phase a.c. motor speed control system using a thyristorized inverter with variable frequency output. The inverter control signals are generated by the HEF4752V (PWM-IC). A special feature of the PWM (Pulse-Width Modulation) - IC is here, that the motor is supplied by sinoidally modulated pulses, hence the resulting motor current will approach a sine-wave with a minimum on higher harmonics. In this way, an optimum speed drive with high performance is obtained.

Furthermore, the HEF4752V contains all logic circuitry required for this special waveform generation, so that the amount of control circuit components is reduced considerable. The speed drive system in Fig. 2 is controlled by the analogue control section.

The FCT and VCT clock pulse oscillators are driven in such a way, that a fast response speed control of the a.c. motor is obtained, depending on: the reference values for speed; motor voltage; motor current (Limited by the measured motor current via DCCT - d.c. current transformer -); the increasing value of V_{Cb} during braking action.

DEVELOPMENT SAMPLE DATA

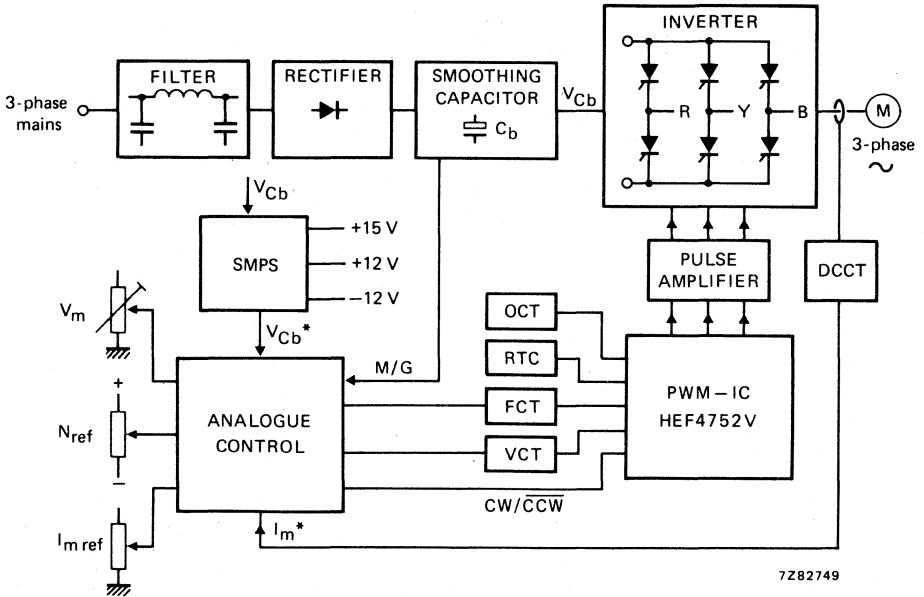


Fig. 2 PWM motor speed control system using HEF4752V.

MORE APPLICATION INFORMATION SUPPLIED ON REQUEST

DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

HEF4753B

LSI

UNIVERSAL TIMER MODULE

The HEF4753B is a universal timer module for counting and dividing as well as for event-recognition and manipulation of input sequences.

The following functions are included: synchronization and edge-detection of the input signal, programmable counter, clock divider with different lengths, operating mode decoder, control logic and output multiplexer.

Depending on the operating mode and the application, the circuit works as a presettable 8-bit counter with transient-pulse suppression, pulse duration selector divider, counter, positive or negative edge delaying module or low-frequency control circuit.

All manipulation possibilities depend on a time scaling, which is adjustable by the 8-bit programmable counter and the system clock. The system clock can be divided internally by 1, 16, 256 or 4096 as input clock for the counter. In all cases the manipulated input sequence appears at the only output OUT.

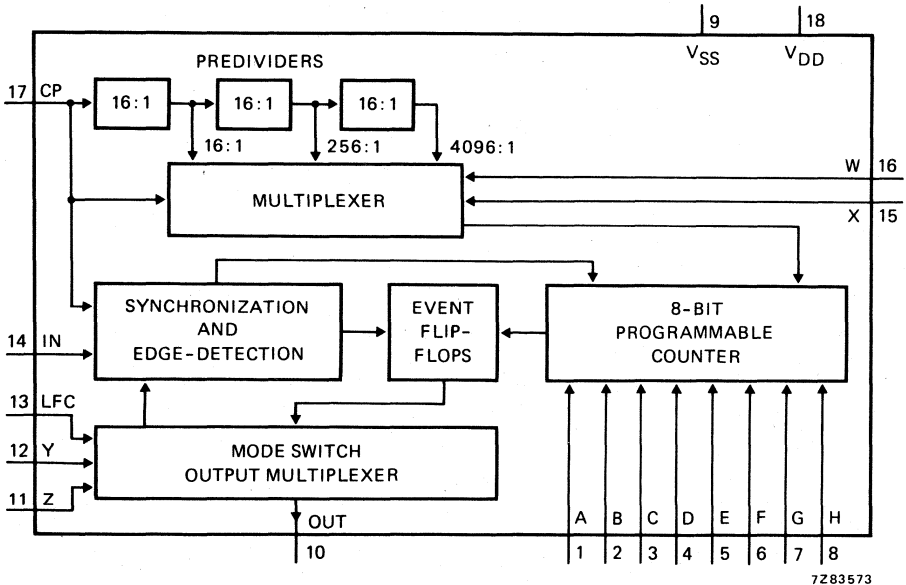


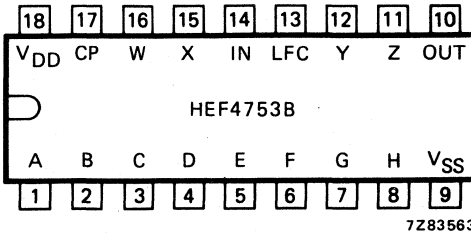
Fig. 1 Functional diagram.

FAMILY DATA

I_{DD} LIMITS category LSI

} see Family Specifications

HEF4753B
LSI



HEF4753BP: 18-lead DIL; plastic (SOT-102A).
HEF4753BD: 18-lead DIL; ceramic (SOT-133).

Fig. 2 Pinning diagram.

FUNCTION TABLES

inputs			operating mode
LFC	Y	Z	
L	L	H	counter
L	H	L	divider
H	H	L	delayed LOW to HIGH edge
H	L	H	delayed HIGH to LOW edge
H	H	H	transient pulse suppression
L	H	H	frequency recognition
LFC	L	L	digital pulse duration selector

H = HIGH state (the more positive voltage).
L = LOW state (the less positive voltage).

Programmable 8-bit counter *

inputs active LOW	value
A	1
B	2
C	4
D	8
E	16
F	32
G	64
H	128

12-bit predivider

W	X	clock for programmable counter CP/X
L	L	X = 1
H	H	X = 16
H	L	X = 256
H	H	X = 4096

* All inputs A to H HIGH is not allowed.

FUNCTIONAL DESCRIPTION

Clock divider and decoder

The clock signal at input CP is, at its original frequency, the system clock, but it also drives the programmable counter. The counter input frequency can be predivided by the factors 1/16, 1/256 and 1/4096, depending on the logic state of inputs W and X (according to the function tables above).

8-bit programmable counter

The 8 inputs A to H are the set inputs of the 8 counter flip-flops. The setting is triggered by an edge of the input signal (at input IN) depending on of the chosen mode.

Event flip-flops, synchronization and edge-detection

The event flip-flops are used to recognize the positive and/or negative edge of the input signal at IN. Parts of the flip-flops are used together with the programmable 8-bit counter as a retriggerable mono-flop, which defines the time scaling for event recognition. The input IN is synchronized by the clock signal CP.

Mode switch and output multiplexer

This function switches the chosen output to the output (OUT) and gives the mode of which the edge at input IN has to be detected. The inputs Z, Y and LFC give 7 modes +1, that means in mode 'Digital Filter' the input LFC can be HIGH or LOW.

OPERATING MODES

The circuit has 6 operating modes which are activated by the logic state of inputs LFC, Y and Z. An extra mode is possible by using two circuits which are connected such so they function as a digital band-filter.

1. Counter mode (LFC = LOW; Y = LOW; Z = HIGH)

In this mode the output OUT should be connected to input IN. If not, only one counter cycle starts after a transition at input IN (see Fig. 3 and note 1).

DEVELOPMENT SAMPLE DATA

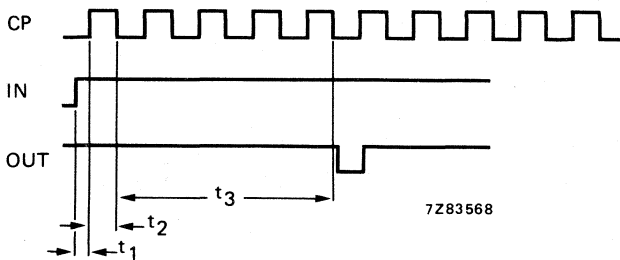
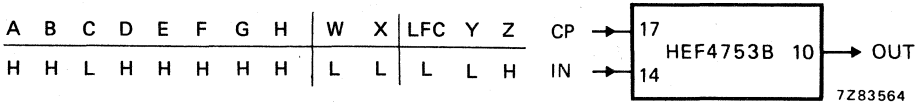


Fig. 3 Timing diagram for counter mode; t_1 = delay until set of 8-bit counter; t_2 = delay to set 8-bit counter; t_3 = predefined delay by programming.

OPERATING MODES (continued)

2. Divider mode (LFC = LOW; Y = HIGH; Z = LOW)

In this mode the output OUT should be connected to input IN. If not, only one counter cycle starts after a transition at input IN (see Fig. 4 and note 1).

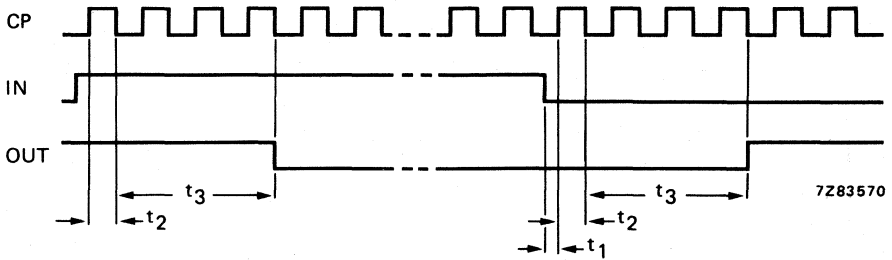
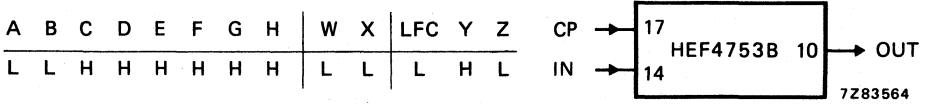


Fig. 4 Timing diagram for divider mode; t_1 = delay until set of 8-bit counter; t_2 , t_3 see Fig. 3.

3. Delayed LOW to HIGH edge mode; see note 2 (LFC = HIGH; Y = HIGH; Z = LOW)

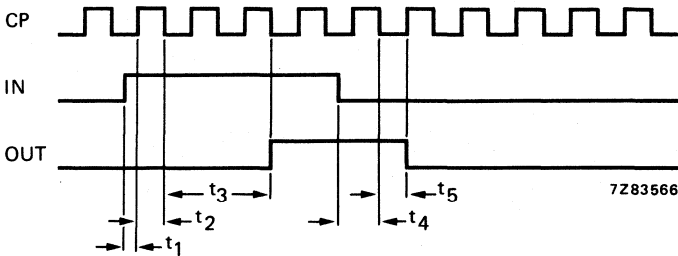
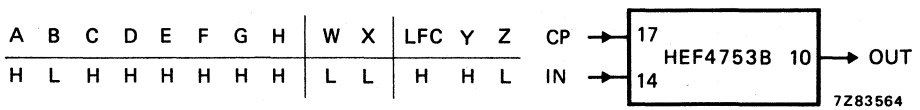


Fig. 5 Timing diagram for delayed LOW to HIGH edge mode; t_1 = delay until set of 8-bit counter; t_2 = delay to set 8-bit counter; t_3 = predefined delay by programming; t_4 = delay until next negative clock edge; t_5 = delay until next positive clock edge.

4. Delayed HIGH to LOW edge mode; see note 2 (LFC = HIGH; Y = LOW; Z = HIGH)

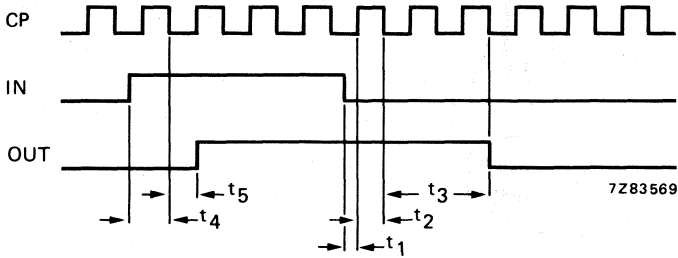
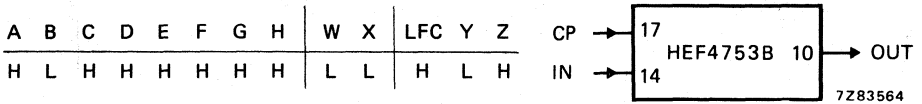


Fig. 6 Timing diagram for delayed HIGH to LOW edge mode; for t_1 to t_5 see Fig. 5.

5. Transient pulse suppression and pulse delaying mode; see note 2 (LFC = Y = Z = HIGH)

In this mode the circuit is working as a digital low-pass filter. An undisturbed pulse will only be delayed (see Fig. 7).

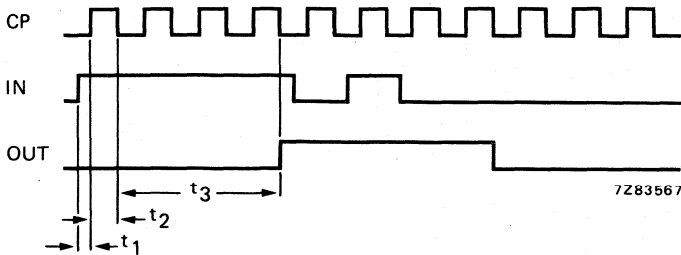
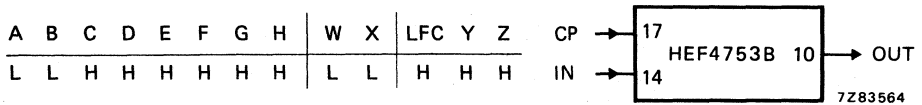


Fig. 7 Timing diagram for transient pulse suppression and pulse delaying mode; for t_1 , t_2 and t_3 see Fig. 5.

DEVELOPMENT SAMPLE DATA

OPERATING MODES (continued)

6. Frequency recognition mode (LFC = LOW; Y = HIGH; Z = HIGH)

The incoming signal must be symmetrical within the limits as given by the specified delay time in note 2, to achieve lower or higher frequency detection (see Fig. 8).

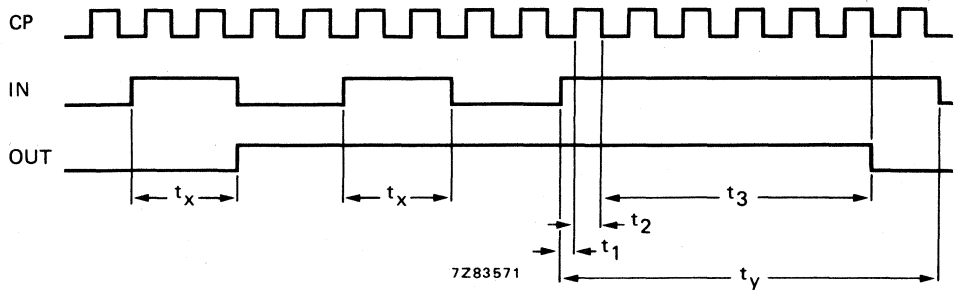
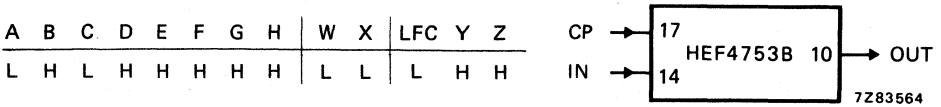
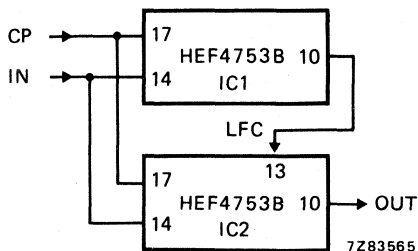


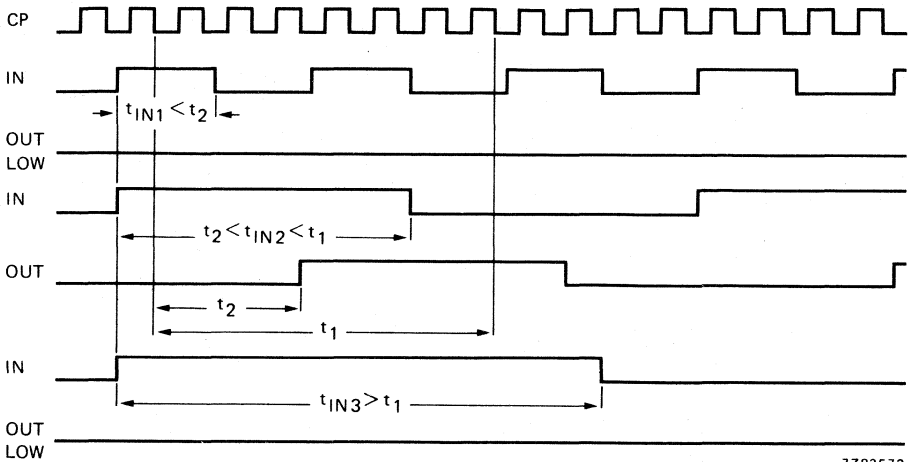
Fig. 8 Timing diagram for frequency recognition mode; t_x = time shorter than t_3 (OUT = H); t_y = time greater than t_3 (OUT = L); for t_1 , t_2 and t_3 see Fig. 5.

7. Digital pulse duration selector mode (Y = Z = LOW)

This mode is a combination of two circuits, both used for frequency recognition. Both circuits are driven by the same clock and same input signal, but programmed for different frequencies. The LFC input of the low-frequency circuit is set to logic LOW, the output is connected to the LFC input of the high-frequency circuit, whose output (OUT) is the 'filter' output. The delay time depends on the same facts as given in note 2. For timing diagram see Fig. 9.

A	B	C	D	E	F	G	H	W	X	LFC	Y	Z	
L	L	L	H	H	H	H	H	L	L	L	H	H	IC1
L	L	H	H	H	H	H	H	L	L	OUT (IC1)	L	L	IC2





7283572

Fig. 9 Timing diagram for digital pulse duration selector mode; t_{IN1} , t_{IN2} and t_{IN3} are the IN input pulse durations; t_1 = predefined delay by programming IC1; t_2 = predefined delay by programming IC2.

Notes to operating modes

1. The number of clocks for one cycle in the counter and divider mode is:
 - a. Contents of programmable counter plus one if $X = W = \text{LOW}$.
 - b. Contents of programmable counter multiplied by 16, 256 or 4096 if X and/or W = LOW.
2. The delay in the modes 3, 4, 6 and 7, and the delay which is identical to the maximum duration of the transient pulse in mode 5 depend on the optional divided clock frequency, the input conditions of the 8-bit presetable counter and in addition, different times of propagation delays, jitter and maximum one half of a clock frequency period.

DEVELOPMENT SAMPLE DATA

D.C. CHARACTERISTICS

 $V_{SS} = 0\text{ V}$

	V_{DD} V	V_{OH} V	V_{OL} V	symbol	T_{amb} (°C)						
					-40		+25		+85		
					min.	max.	min.	max.	min.	max.	
Output (sink) current LOW (pin 10)	4,75		0,4	I_{OL}	2,7	—	2,3	—	1,8	—	mA
	10		0,5		9,5	—	8,0	—	6,3	—	mA
	15		1,5		24,0	—	20,0	—	16,0	—	mA
Output (source) current HIGH (pin 10)	5	4,6		$-I_{OH}$	0,6	—	0,5	—	0,4	—	mA
	10	9,5			1,8	—	1,5	—	1,2	—	mA
	15	13,5			6,0	—	5,0	—	4,0	—	mA

A.C. CHARACTERISTICS

 $V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ °C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	symbol				typical extrapolation formula
			min.	typ.	max.	
Propagation delays CP \rightarrow OUT HIGH to LOW	5	t_{PHL}		420	850	ns
	10			180	360	ns
	15			120	250	ns
LOW to HIGH	5	t_{PLH}		450	900	ns
	10			200	400	ns
	15			140	280	ns
Output transition times HIGH to LOW	5	t_{THL}		30	60	ns
	10			15	30	ns
	15			10	20	ns
LOW to HIGH	5	t_{TLH}		60	120	ns
	10			30	60	ns
	15			20	40	ns
Input rise and fall times pins 13, 14, 17	5	t_r, t_f	}	no limit		
	10					
	15					
Maximum clock pulse frequency pin 17; $\delta = 50\%$	5	f_{max}	3	6		MHz
	10		7	14		MHz
	15		8	17		MHz

	V_{DD} V	typical formula for P (μW)	where
			Dynamic power dissipation per package (P)
	10	$8000 f_i + \Sigma (f_o C_L) \times V_{DD}^2$	
	15	$19000 f_i + \Sigma (f_o C_L) \times V_{DD}^2$	

DEVELOPMENT SAMPLE DATA

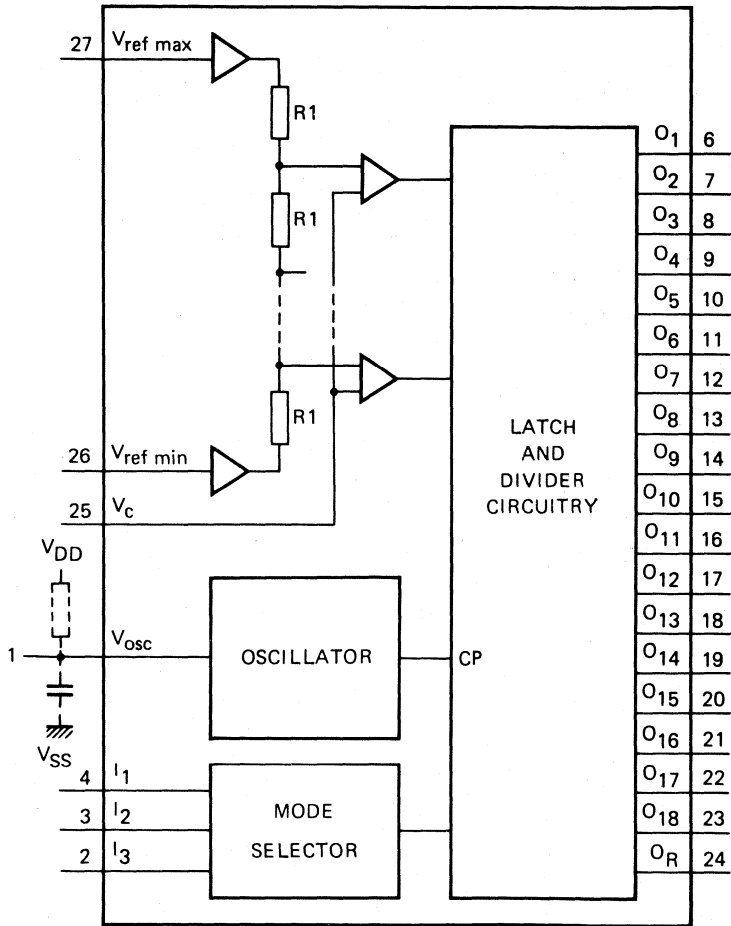
This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

HEF4754V

LSI

18-ELEMENT BAR GRAPH LCD DRIVER

The HEF4754V drives an 18-element bar graph LCD in linear relation to the control voltage (V_c) in a pointer or thermometer mode.

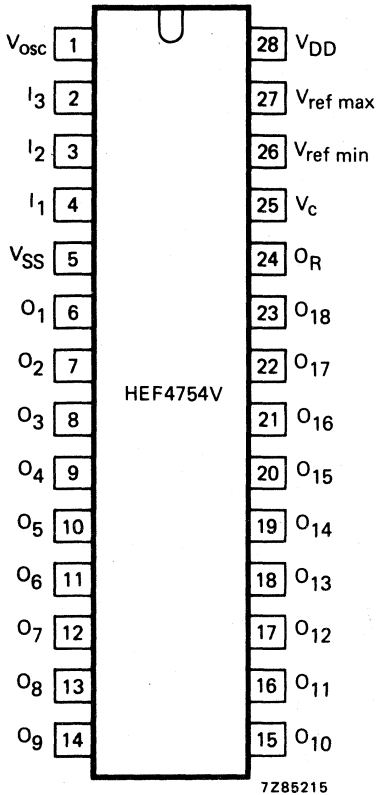


7Z85217

Fig. 1 Functional diagram.

FAMILY DATA see Family Specifications

HEF4754V
LSI



PINNING

- V_{osc} oscillator terminal
- V_c control voltage input
- $V_{ref\ min}$ } reference voltage inputs
- $V_{ref\ max}$ }
- I_1 thermometer/pointer (choice select input)
- I_2 peak value; reset/9 or 18 bars (choice select input)
- I_3 reset; repetitively reset (choice select input)
- O_1 to O_{18} bar outputs
- O_R back plate output

HEF4754VP: 28-lead DIL; plastic (SOT-117).
HEF4754VD: 28-lead DIL; ceramic (SOT-135).

Fig. 2 Pinning diagram.

FUNCTION TABLE

I_1	I_2	I_3	mode
L	L	X	pointer; 18 bars
L	H	X	pointer; 9 bars
H	L	X	thermometer; no peak value
H	H	L	thermometer; peak value, repetitively reset
H	H	H	thermometer; peak value, manually reset

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

GENERAL DESCRIPTION

The HEF4754V drives an 18-element bar graph LCD in linear relation to the control voltage (V_C) in a pointer or thermometer mode. The first bar lights up when V_C is smaller than $V_{T(\text{bar})2}$ (see equation [3] below).

In the pointer mode, the circuit can drive 9 or 18 bars; in the thermometer mode, the circuit also drives the peak value indication. This can be reset or repetitively reset, after 1,5 to 2 seconds.

The circuit has analogue and digital parts. The analogue part consists of 17 comparators, with their non-inverting inputs connected together and coupled to the control input V_C . The inverting inputs of the comparators are connected in succession to the nodes of an 18-part resistor divider. The distance between the switching levels of the comparators is defined by the voltage difference across this divider. The extremities of the resistor divider are coupled via high-input amplifiers to the maximum reference voltage input and the minimum reference voltage input.

The digital part has one reference output (O_R) to drive the back plate, and 18 outputs (O_1 to O_{18}) to drive each bar. Three latches and some gates are incorporated for each bar output. An on-chip oscillator (1024 Hz) with external R and C drives the circuit. The outputs are driven at 64 Hz. The select inputs I_1 to I_3 are provided with an on-chip pull-up element, and they may therefore be left floating (equals HIGH state).

LINEARITY

$V_{DD} = 10 \text{ V}$; $V_{\text{ref max}} = 9,5 \text{ V}$; $V_{\text{ref min}} = 0,5 \text{ V}$; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$

$\Delta V_1 = 250 \text{ mV}$ (this is the tolerance of the step voltage).

$$V_{\text{step}} = V_{\text{step}'} + \Delta V_1 \quad [1]$$

$V_{\text{step}'}$ is the (internal) voltage drop across the resistor-ladder network.

$$V_{\text{step}'} = \frac{(V_{\text{ref max}} \pm \Delta V_2) - (V_{\text{ref min}} \pm \Delta V_2)}{18} \quad [2]$$

ΔV_2 is the maximum offset voltage spread of the on-chip voltage follower.

$\Delta V_2 = 250 \text{ mV}$.

ABSOLUTE VOLTAGE TRIGGER LEVEL

The absolute voltage trigger level at the V_C pin is $V_{T(\text{bar})n}$:

$$V_{T(\text{bar})n} = (V_{\text{ref min}} \pm \Delta V_2^*) + \{ (n-1) V_{\text{step}'} \pm \Delta V_1 \}, \text{ in which } [3]$$

$n = \text{number of bars}; 2 \leq n \leq 18$.

For $n = 1$ (first bar) see text above.

DEVELOPMENT SAMPLE DATA

* For ΔV_2 the same sign (+ or -) should be used as in equation [2].



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{DD}	-0,5 to +18 V
Voltage on any input	V_I	-0,5 to $V_{DD} + 0,5$ V
D.C. current into any input or output	$\pm I_I$	max. 10 mA
Storage temperature	T_{stg}	-25 to +125 °C
Operating ambient temperature	T_{amb}	-20 to +70 °C

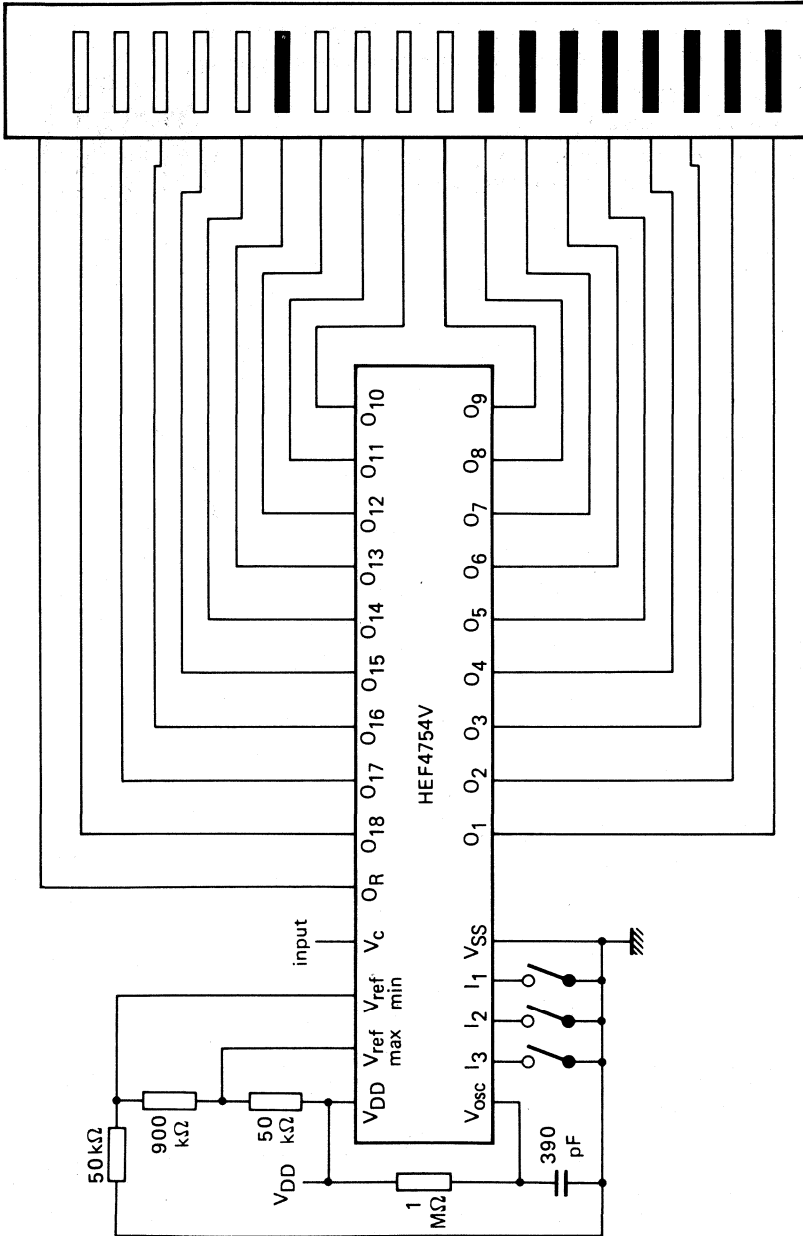
D.C. CHARACTERISTICS

$V_{SS} = 0$ V

	V_{DD} V	symbol	T_{amb} (°C)						notes		
			-40		+25		+85				
			min.	max.	min.	typ.	max.	min.		max.	
Quiescent device current	10	I_{DD}	-	-	-	-	1000	-	-	μ A	1
Input leakage current (except select inputs)	5	$\pm I_{IN}$	-	-	-	-	100	-	-	nA	2
	10		-	-	-	-	100	-	-	nA	
Input voltage HIGH select inputs	5	V_{IH}	3,5	-	3,5	-	-	3,5	-	V	3
	10		7,0	-	7,0	-	-	7,0	-	V	
Input voltage LOW select inputs	5	V_{IL}	-	1,5	-	-	1,5	-	1,5	V	3
	10		-	3,0	-	-	3,0	-	3,0	V	
Output voltage HIGH	5	V_{OH}	4,99	-	4,99	-	-	4,95	-	V	3
	10		9,99	-	9,99	-	-	9,95	-	V	
Output voltage LOW	5	V_{OL}	-	0,01	-	-	0,01	-	0,05	V	3
	10		-	0,01	-	-	0,01	-	0,05	V	
Output current HIGH	5	$-I_{OH}$	0,36	-	0,3	-	-	0,24	-	mA	4
	10		0,84	-	0,7	-	-	0,56	-	mA	
Output current LOW	5	I_{OL}	0,36	-	0,3	-	-	0,24	-	mA	5
	10		1,08	-	0,9	-	-	0,72	-	mA	
Input voltage control input V_C	5	V_I	-	-	0	-	5	-	-	V	3
	10		-	-	0	-	10	-	-	V	
	15		-	-	0	-	15	-	-	V	
Input voltage V_{ref} max input	5	V_I	-	-	4,5	-	4,5	-	-	V	3
	10		-	-	4,5	-	9,5	-	-	V	
	15		-	-	4,5	-	14,5	-	-	V	
Input voltage V_{ref} min input	5	V_I	-	-	0,5	-	0,5	-	-	V	3
	10		-	-	0,5	-	5,5	-	-	V	
	15		-	-	0,5	-	10,5	-	-	V	
Operating supply current	10	I_{DD}	-	-	-	750	-	-	μ A	Fig. 3	

NOTES

1. $V_{\text{ref min}} = 0,5 \text{ V}$; $V_{\text{ref max}} = 9,5 \text{ V}$; $V_{\text{osc}} = V_{\text{c}} = 0 \text{ V}$; I_1 , I_2 and I_3 at V_{DD} .
2. Pin under test at V_{SS} or V_{DD} , all other inputs simultaneously at V_{SS} or V_{DD} .
3. $I_{\text{O}} = 0$; all inputs at V_{SS} or V_{DD} .
4. $V_{\text{OH}} = V_{\text{DD}} - 0,5 \text{ V}$; inputs at V_{SS} or V_{DD} .
5. At $V_{\text{DD}} = 5 \text{ V}$: $V_{\text{OL}} = 0,4 \text{ V}$; inputs at V_{SS} or V_{DD} .
At $V_{\text{DD}} = 10 \text{ V}$: $V_{\text{OL}} = 0,5 \text{ V}$; inputs at V_{SS} or V_{DD} .



7Z85216

Fig. 3 Typical operating set-up.

3-STATE HEX NON-INVERTING BUFFER



The HEF40097B is a hex non-inverting buffer with 3-state outputs. The 3-state outputs are controlled by two enable inputs (\overline{EO}_4 and \overline{EO}_2). A HIGH on \overline{EO}_4 causes four of the six buffer elements to assume a high impedance or OFF-state, regardless of the other input conditions and a HIGH on \overline{EO}_2 causes the outputs of the remaining two buffer elements to assume a high impedance or OFF-state, regardless of the other input conditions.

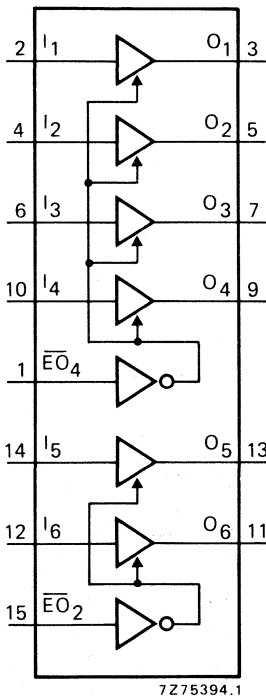


Fig. 1 Functional diagram.

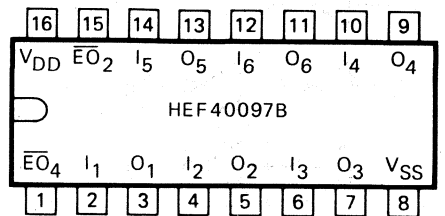


Fig. 2 Pinning diagram.

HEF40097BP: 16-lead DIL; plastic (SOT-38Z).
HEF40097BD: 16-lead DIL; ceramic (SOT-74).
HEF40097BT: 16-lead flat pack; plastic (SO-16; SOT-109A).

PINNING

I_1 to I_6 buffer inputs
 \overline{EO}_4 , \overline{EO}_2 enable inputs (active LOW)
 O_1 to O_6 buffer outputs (active HIGH)

FAMILY DATA

I_{DD} LIMITS category BUFFERS

see Family Specifications

HEF40097B

buffers

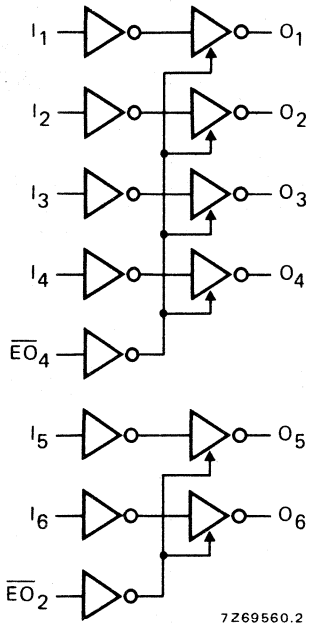


Fig. 3 Logic diagram.

D.C. CHARACTERISTICS

$V_{SS} = 0\text{ V}$

	V_{DD} V	V_{OH} V	V_{OL} V	symbol	T_{amb} (°C)						
					-40		+25		+85		mA
					min.	max.	min.	max.	min.	max.	
Output current HIGH	5	4,6		- I_{OH}	1,2		1,0		0,8		
	10	9,5			3,8		3,2		2,5		
	15	13,5			12,0		10,0		8,0		
HIGH	5	2,5		- I_{OH}	3,8		3,2		2,5		
	10		0,4		3,5		2,9		2,3		
	15		0,5		12,0		10,0		8,0		
Output current LOW	5		0,4	I_{OL}	3,5		2,9		2,3		
	10		0,5		12,0		10,0		8,0		
	15		1,5		24,0		20,0		16,0		

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V _{DD} V	symbol	typ.	max.		typical extrapolation formula
Propagation delays I _n → O _n HIGH to LOW	5	t _{PHL}	70	140	ns	60 ns + (0,20 ns/pF) C _L
	10		30	60	ns	26 ns + (0,08 ns/pF) C _L
	15		25	50	ns	22 ns + (0,06 ns/pF) C _L
LOW to HIGH	5	t _{PLH}	60	120	ns	45 ns + (0,30 ns/pF) C _L
	10		25	50	ns	19 ns + (0,13 ns/pF) C _L
	15		20	40	ns	16 ns + (0,09 ns/pF) C _L
Output transition times HIGH to LOW	5	t _{THL}	30	60	ns	15 ns + (0,30 ns/pF) C _L
	10		15	30	ns	10 ns + (0,11 ns/pF) C _L
	15		10	20	ns	7 ns + (0,07 ns/pF) C _L
LOW to HIGH	5	t _{TLH}	35	70	ns	10 ns + (0,50 ns/pF) C _L
	10		20	40	ns	8 ns + (0,24 ns/pF) C _L
	15		15	30	ns	6 ns + (0,18 ns/pF) C _L
3-state propagation delays						
Output disable times EO ₂ , EO ₄ → O _n HIGH	5	t _{PHZ}	45	95	ns	
	10		35	70	ns	
	15		30	60	ns	
LOW	5	t _{PLZ}	60	120	ns	
	10		35	70	ns	
	15		25	55	ns	
Output enable times EO ₂ , EO ₄ → O _n HIGH	5	t _{PZH}	75	150	ns	
	10		35	70	ns	
	15		30	60	ns	
LOW	5	t _{PZL}	95	190	ns	
	10		40	80	ns	
	15		30	65	ns	

	V _{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	5 400 f _i + Σ(f _o C _L) × V _{DD} ²	f _i = input freq. (MHz)
	10	25 200 f _i + Σ(f _o C _L) × V _{DD} ²	f _o = output freq. (MHz)
	15	96 500 f _i + Σ(f _o C _L) × V _{DD} ²	C _L = load cap. (pF)
			Σ(f _o C _L) = sum of outputs
			V _{DD} = supply voltage (V)

3-STATE HEX INVERTING BUFFER



The HEF40098B is a hex inverting buffer with 3-state outputs. The 3-state outputs are controlled by two enable inputs (\overline{EO}_4 and \overline{EO}_2). A HIGH on \overline{EO}_4 causes four of the six buffer elements to assume a high impedance or OFF-state regardless of the other input conditions and a HIGH on \overline{EO}_2 causes the outputs of the remaining two buffer elements to assume a high impedance or OFF-state regardless of the other input conditions.

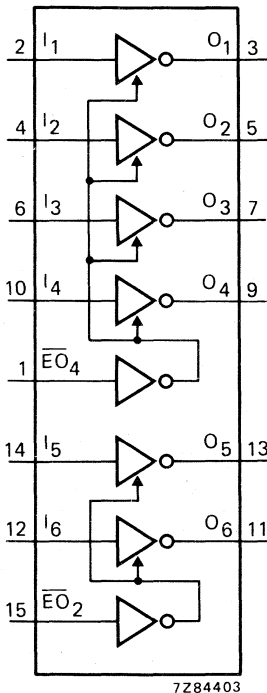


Fig. 1 Functional diagram.

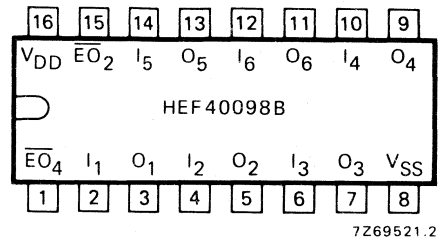


Fig. 2 Pinning diagram.

HEF40098BP: 16-lead DIL; plastic (SOT-38Z).
 HEF40098BD: 16-lead DIL; ceramic (SOT-74).
 HEF40098BT: 16-lead flat pack; plastic (SO-16; SOT-109A).

PINNING

I_1 to I_6 buffer inputs
 \overline{EO}_4 , \overline{EO}_2 enable inputs (active LOW)
 O_1 to O_6 buffer outputs (active LOW)

FAMILY DATA

I_{DD} LIMITS category BUFFERS

see Family Specifications

HEF40098B

buffers

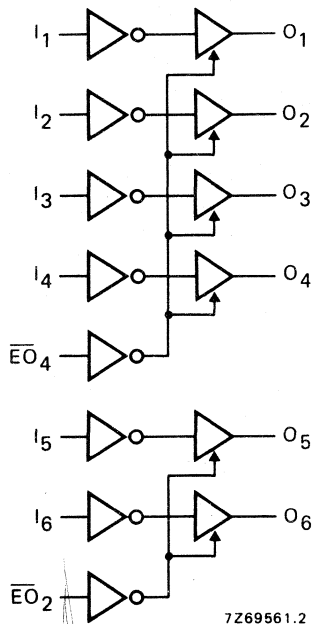


Fig. 3 Logic diagram.

D.C. CHARACTERISTICS

$V_{SS} = 0\text{ V}$

	V_{DD} V	V_{OH} V	V_{OL} V	symbol	T_{amb} (°C)						
					-40		+25		+85		mA
					min.	max.	min.	max.	min.	max.	
Output current HIGH	5	4,6		- I_{OH}	1,2		1,0		0,8		mA
	10	9,5			3,8		3,2		2,5		mA
	15	13,5			12,0		10,0		8,0		mA
HIGH	5	2,5		- I_{OH}	3,8		3,2		2,5		mA
Output current LOW	4,75		0,4	I_{OL}	3,5		2,9		2,3		mA
	10		0,5		12,0		10,0		8,0		mA
	15		1,5		24,0		20,0		16,0		mA

A.C. CHARACTERISTICS

 $V_{SS} = 0 \text{ V}$; $T_{amb} = 25 \text{ }^\circ\text{C}$; $C_L = 50 \text{ pF}$; input transition times $\leq 20 \text{ ns}$

	V_{DD} V	symbol	typ.	max.		typical extrapolation formula
Propagation delays $I_n \rightarrow O_n$ HIGH to LOW	5	t_{PHL}	80	160	ns	$70 \text{ ns} + (0,20 \text{ ns/pF}) C_L$
	10		35	70	ns	$31 \text{ ns} + (0,08 \text{ ns/pF}) C_L$
	15		25	50	ns	$22 \text{ ns} + (0,06 \text{ ns/pF}) C_L$
LOW to HIGH	5	t_{PLH}	65	130	ns	$50 \text{ ns} + (0,30 \text{ ns/pF}) C_L$
	10		30	60	ns	$24 \text{ ns} + (0,13 \text{ ns/pF}) C_L$
	15		25	50	ns	$21 \text{ ns} + (0,05 \text{ ns/pF}) C_L$
Output transition times HIGH to LOW	5	t_{THL}	30	60	ns	$15 \text{ ns} + (0,30 \text{ ns/pF}) C_L$
	10		15	30	ns	$10 \text{ ns} + (0,11 \text{ ns/pF}) C_L$
	15		10	20	ns	$7 \text{ ns} + (0,07 \text{ ns/pF}) C_L$
LOW to HIGH	5	t_{TLH}	35	70	ns	$10 \text{ ns} + (0,50 \text{ ns/pF}) C_L$
	10		20	40	ns	$8 \text{ ns} + (0,24 \text{ ns/pF}) C_L$
	15		15	30	ns	$6 \text{ ns} + (0,18 \text{ ns/pF}) C_L$
3-state propagation delays						
Output disable times $EO_2, EO_4 \rightarrow O_n$ HIGH	5	t_{PHZ}	45	85	ns	
	10		35	65	ns	
	15		30	60	ns	
LOW	5	t_{PLZ}	65	135	ns	
	10		40	80	ns	
	15		35	70	ns	
Output enable times $EO_2, EO_4 \rightarrow O_n$ HIGH	5	t_{PZH}	70	140	ns	
	10		35	75	ns	
	15		30	65	ns	
LOW	5	t_{PZL}	90	185	ns	
	10		40	85	ns	
	15		35	70	ns	

	V_{DD} V	typical formula for P (μW)	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load cap. (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
Dynamic power dissipation per package (P)	5	$5\,000 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	10	$22\,800 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$81\,000 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

HEX SCHMITT TRIGGER



Each circuit of the HEF40106B functions as an inverter with Schmitt-trigger action. The Schmitt-trigger switches at different points for the positive and negative-going input signals. The difference between the positive-going voltage (V_{IH}) and the negative-going voltage (V_{IL}) is defined as hysteresis voltage (V_H).

This device may be used for exchanged noise immunity or to "square up" slowly changing waveforms.

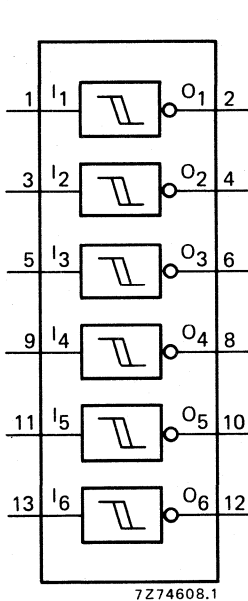


Fig. 1 Function diagram.

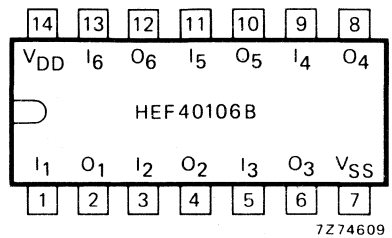


Fig. 2 Pinning diagram.

HEF40106BP: 14-lead DIL; plastic (SOT-27S, T, V).
HEF40106BD: 14-lead DIL; ceramic (SOT-73).
HEF40106BT: 14-lead flat pack; plastic (SO-14; SOT-108A).

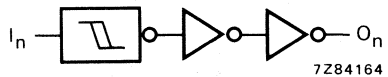


Fig. 3 Logic diagram (one inverter).

FAMILY DATA

I_{DD} LIMITS category GATES

} see Family Specifications

D.C. CHARACTERISTICS

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$

	V_{DD} V	symbol	min.	typ.	max.	
Hysteresis voltage	5	V_H	0,5	0,8		V
	10		0,7	1,3		V
	15		0,9	1,8		V
Switching levels positive-going input voltage	5	V_{IH}		3,0	3,5	V
	10			5,8	7	V
	15			8,3	11	V
negative-going input voltage	5	V_{IL}	1,5	2,2		V
	10		3	4,5		V
	15		4	6,5		V

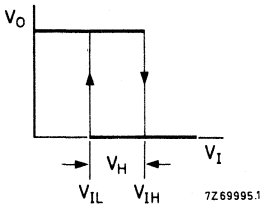


Fig. 4 Transfer characteristic.

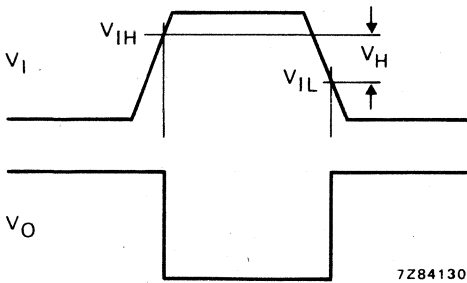


Fig. 5 Waveforms showing definition of V_{IH} , V_{IL} and V_H , where V_{IL} and V_{IH} are between limits of 30% and 70%.

A.C. CHARACTERISTICS

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	symbol	typ.	max.		typical extrapolation formula	
Propagation delays $I_n \rightarrow O_n$ HIGH to LOW	5	t_{PHL}	90	180	ns	$63\text{ ns} + (0,55\text{ ns/pF}) C_L$	
	10		35	70	ns	$24\text{ ns} + (0,23\text{ ns/pF}) C_L$	
	15		30	60	ns	$22\text{ ns} + (0,16\text{ ns/pF}) C_L$	
	LOW to HIGH	5	t_{PLH}	75	150	ns	$48\text{ ns} + (0,55\text{ ns/pF}) C_L$
		10		35	70	ns	$24\text{ ns} + (0,23\text{ ns/pF}) C_L$
		15		30	60	ns	$22\text{ ns} + (0,16\text{ ns/pF}) C_L$
Output transition times	HIGH to LOW	t_{THL}	5	60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$
			10	30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$
			15	20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$
	LOW to HIGH	t_{TLH}	5	60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$
			10	30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$
			15	20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$2\,300 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz)
	10		f_o = output freq. (MHz)
	15		C_L = load capacitance (pF)
			$\Sigma(f_o C_L)$ = sum of outputs
			V_{DD} = supply voltage (V)

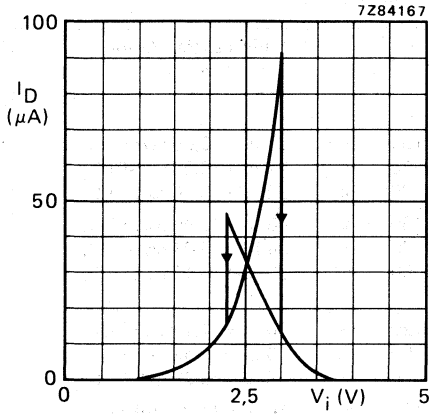


Fig. 6 Typical drain current as a function of input voltage; $V_{DD} = 5$ V; $T_{amb} = 25$ °C.

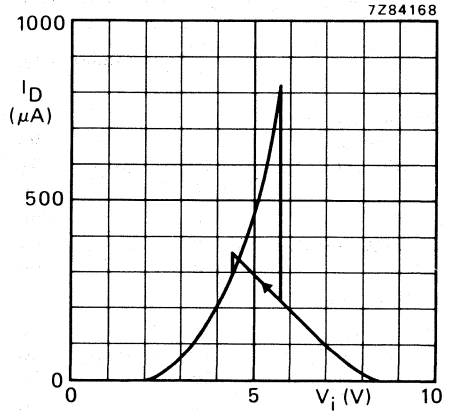


Fig. 7 Typical drain current as a function of input voltage; $V_{DD} = 10$ V; $T_{amb} = 25$ °C.

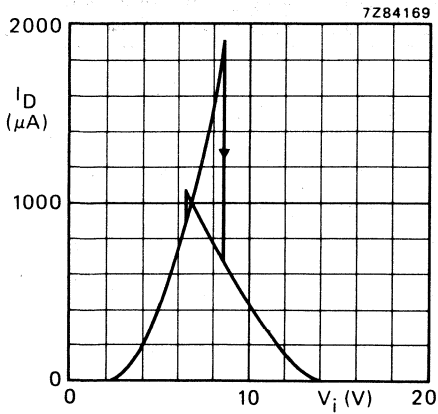


Fig. 8 Typical drain current as a function of input voltage; $V_{DD} = 15$ V; $T_{amb} = 25$ °C.

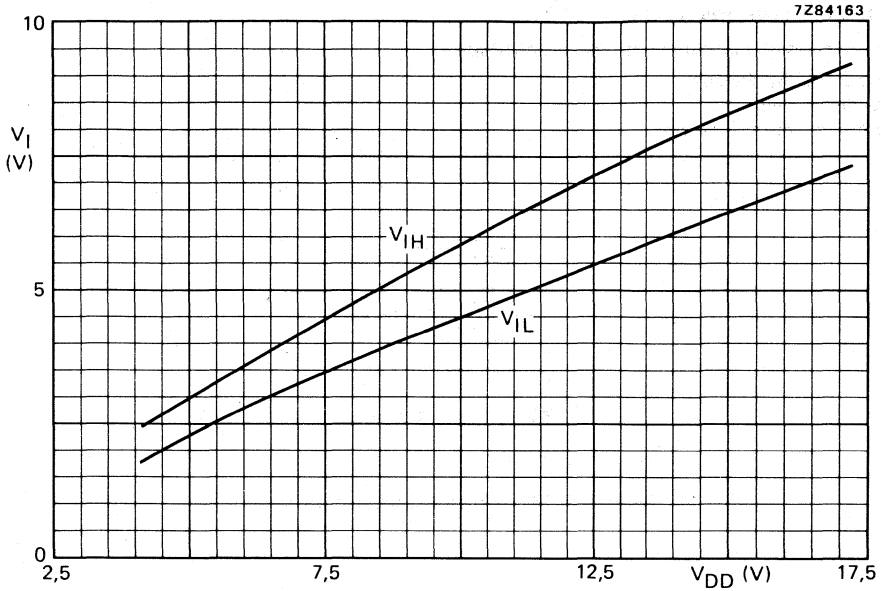


Fig. 9 Typical switching levels as a function of supply voltage V_{DD} ; $T_{amb} = 25\text{ }^{\circ}\text{C}$.

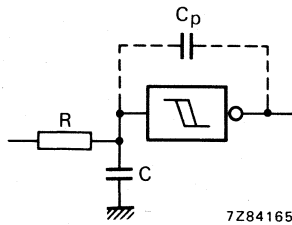


Fig. 10 Schmitt trigger driven via a high impedance ($R > 1\text{ k}\Omega$).

If a Schmitt trigger is driven via a high impedance ($R > 1\text{ k}\Omega$) then it is necessary to incorporate a capacitor C of such value that: $\frac{C}{C_p} > \frac{V_{DD}-V_{SS}}{V_H}$, otherwise oscillation can occur on the edges of a pulse.

C_p is the external parasitic capacitance between input and output; the value depends on the circuit board layout.

APPLICATION INFORMATION

Some examples of applications for the HEF40106B are:

- Wave and pulse shapers
- Astable multivibrators
- Monostable multivibrators.

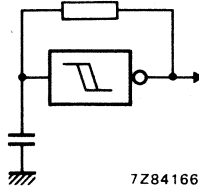


Fig. 11 The HEF40106B used as an astable multivibrator.

4-BIT SYNCHRONOUS DECADE COUNTER WITH ASYNCHRONOUS RESET



The HEF40160B is a fully synchronous edge-triggered 4-bit decade counter with a clock input (CP), an overriding asynchronous master reset ($\overline{\text{MR}}$), four parallel data inputs (P_0 to P_3), three synchronous mode control inputs (parallel enable ($\overline{\text{PE}}$), count enable parallel (CEP) and count enable trickle (CET)), buffered outputs from all four bit positions (O_0 to O_3) and a terminal count output (TC).

Operation is fully synchronous (except for the $\overline{\text{MR}}$ input) and occurs on the LOW to HIGH transition of CP. When $\overline{\text{PE}}$ is LOW, the next LOW to HIGH transition of CP loads data into the counter from P_0 to P_3 regardless of the levels of CEP and CET inputs.

When $\overline{\text{PE}}$ is HIGH, the next LOW to HIGH transition of CP advances the counter to its next state only if both CEP and CET are HIGH; otherwise, no change occurs in the state of the counter. TC is HIGH when the state of the counter is 9 ($O_0 = O_3 = \text{HIGH}$, $O_1 = O_2 = \text{LOW}$) and when CET is HIGH. A LOW on $\overline{\text{MR}}$ sets all outputs (O_0 to O_3 and TC) LOW, independent of the state of all other inputs. Multistage synchronous counting is possible without additional components by using a carry look-ahead counting technique; in this case, TC is used to enable successive cascaded stages. CEP, CET and $\overline{\text{PE}}$ must be stable only during the set-up time before the LOW to HIGH transition of CP.

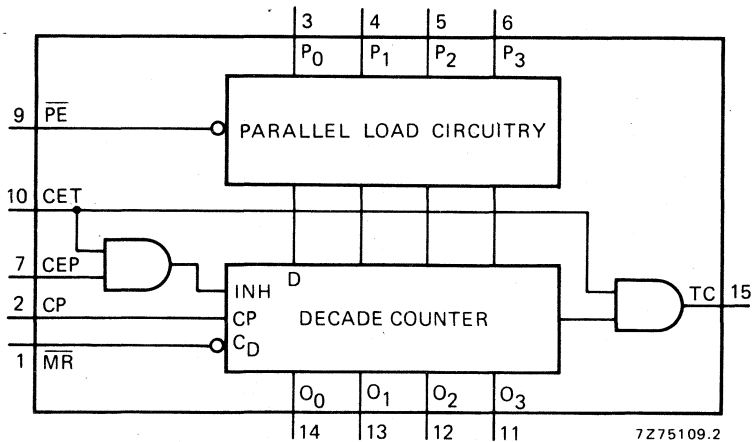
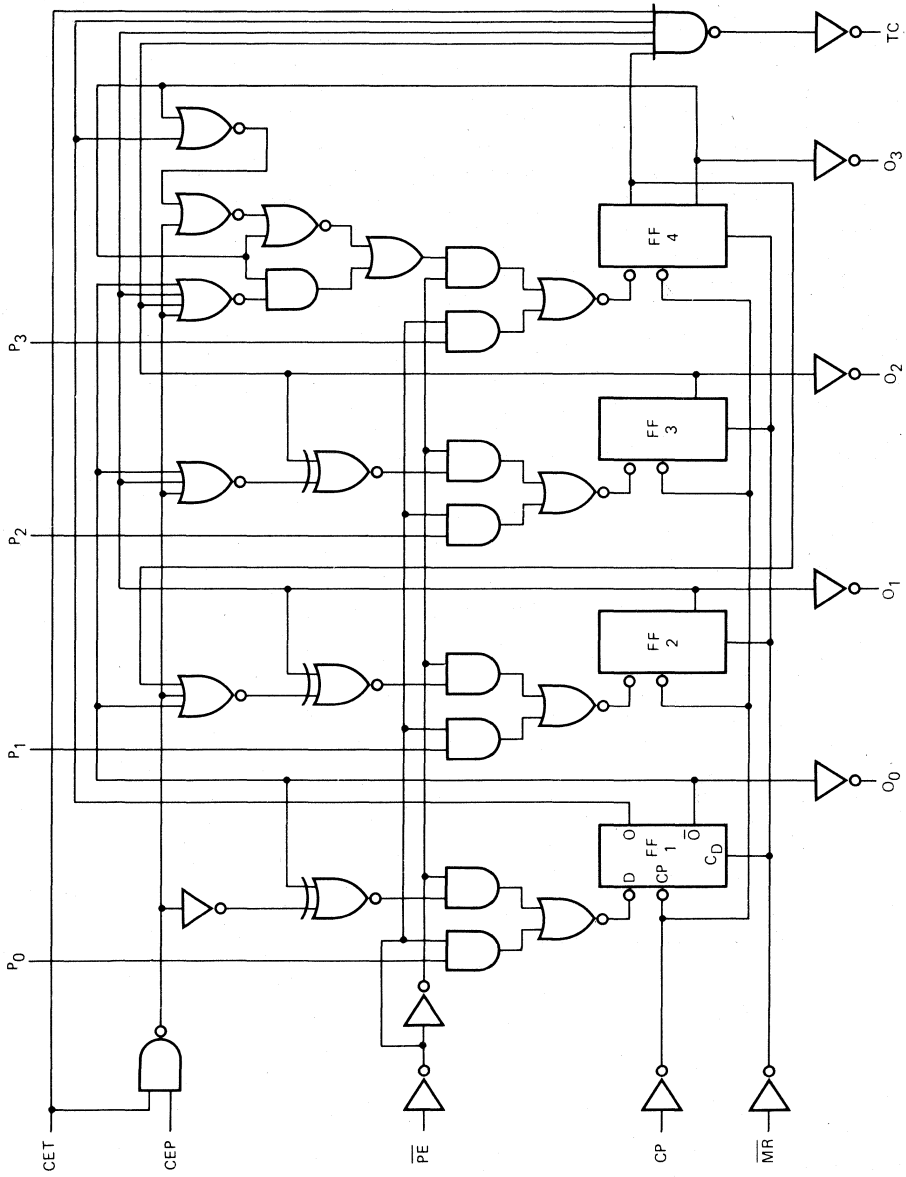


Fig. 1 Functional diagram.

FAMILY DATA

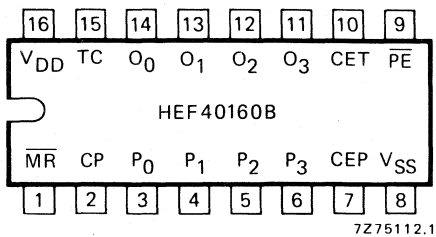
I_{DD} LIMITS category MSI

see Family Specifications



7275085.1

Fig. 2 Logic diagram.



PINNING

- \overline{PE} parallel enable input
- P_0 to P_3 parallel data inputs
- CEP count enable parallel input
- CET count enable trickle input
- CP clock input (LOW to HIGH, edge-triggered)
- \overline{MR} master reset input (active LOW)
- O_0 to O_3 parallel outputs
- TC terminal count output

Fig. 3 Pinning diagram.

HEF40160BP: 16-lead DIL; plastic (SOT-38Z).
 HEF40160BD: 16-lead DIL; ceramic (SOT-74).
 HEF40160BT: 16-lead flat pack; plastic (SO-16; SOT-109A).

SYNCHRONOUS MODE SELECTION

\overline{PE}	CEP	CET	mode
L	X	X	preset
H	L	X	no change
H	X	L	no change
H	H	H	count

TERMINAL COUNT GENERATION

CET	$(O_0 \cdot \overline{O}_1 \cdot \overline{O}_2 \cdot O_3)$	TC
L	L	L
L	H	L
H	L	L
H	H	H

\overline{MR} = HIGH

- H = HIGH state (the more positive voltage)
- L = LOW state (the less positive voltage)
- X = state is immaterial

$$TC = CET \cdot O_0 \cdot \overline{O}_1 \cdot \overline{O}_2 \cdot O_3$$

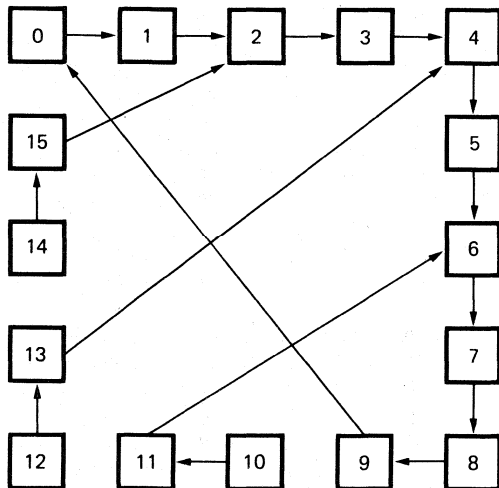


Fig. 4 State diagram.

7Z75086

A.C. CHARACTERISTICS

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^\circ\text{C}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	typical formula for P (μW)	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
Dynamic power dissipation per package (P)	5	$1\,200 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	10	$5\,600 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$16\,000 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

A.C. CHARACTERISTICS

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^\circ\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	symbol	min.	typ.	max.	typical extrapolation formula	
Propagation delays CP \rightarrow O_n HIGH to LOW	5	t_{PHL}		110	220	ns	$83\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10			45	90	ns	$34\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			30	60	ns	$22\text{ ns} + (0,16\text{ ns/pF}) C_L$
LOW to HIGH	5	t_{PLH}		115	230	ns	$88\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10			45	95	ns	$34\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			35	65	ns	$27\text{ ns} + (0,16\text{ ns/pF}) C_L$
CP \rightarrow TC HIGH to LOW	5	t_{PHL}		130	260	ns	$103\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10			55	105	ns	$44\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			35	75	ns	$27\text{ ns} + (0,16\text{ ns/pF}) C_L$
LOW to HIGH	5	t_{PLH}		140	280	ns	$113\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10			55	115	ns	$44\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			40	80	ns	$32\text{ ns} + (0,16\text{ ns/pF}) C_L$
CET \rightarrow TC HIGH to LOW	5	t_{PHL}		105	210	ns	$78\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10			50	100	ns	$39\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			35	75	ns	$27\text{ ns} + (0,16\text{ ns/pF}) C_L$
LOW to HIGH	5	t_{PLH}		90	185	ns	$63\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10			35	70	ns	$24\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			25	50	ns	$17\text{ ns} + (0,16\text{ ns/pF}) C_L$
$\overline{\text{MR}} \rightarrow O_n$ HIGH to LOW	5	t_{PHL}		120	245	ns	$93\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10			50	100	ns	$39\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			35	70	ns	$27\text{ ns} + (0,16\text{ ns/pF}) C_L$
$\overline{\text{MR}} \rightarrow TC$ HIGH to LOW	5	t_{PHL}		145	295	ns	$118\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10			60	120	ns	$49\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			45	85	ns	$37\text{ ns} + (0,16\text{ ns/pF}) C_L$
Output transition times HIGH to LOW	5	t_{THL}		60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$
	10			30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$
	15			20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$
LOW to HIGH	5	t_{TLH}		60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$
	10			30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$
	15			20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$

A.C. CHARACTERISTICS

 $V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	symbol	min.	typ.	max.	
Minimum clock pulse width; LOW	5	tWCPL	100	50	ns	see also waveforms Figs 5, 6, 7 and 8
	10		40	20	ns	
	15		30	15	ns	
Minimum $\overline{\text{MR}}$ pulse width; LOW	5	tWMRL	100	50	ns	
	10		40	20	ns	
	15		30	15	ns	
Recovery time for MR	5	tRMR	25	0	ns	
	10		15	0	ns	
	15		10	0	ns	
Set-up times $P_n \rightarrow \text{CP}$	5	t _{su}	110	55	ns	
	10		40	20	ns	
	15		30	15	ns	
$\overline{\text{PE}} \rightarrow \text{CP}$	5	t _{su}	120	60	ns	
	10		40	20	ns	
	15		25	10	ns	
CEP, CET \rightarrow CP	5	t _{su}	260	130	ns	
	10		100	50	ns	
	15		70	35	ns	
Hold times $P_n \rightarrow \text{CP}$	5	t _{hold}	20	-35	ns	
	10		10	-10	ns	
	15		5	-10	ns	
$\overline{\text{PE}} \rightarrow \text{CP}$	5	t _{hold}	15	-45	ns	
	10		5	-15	ns	
	15		5	-10	ns	
CEP, CET \rightarrow CP	5	t _{hold}	25	-105	ns	
	10		15	-35	ns	
	15		10	-25	ns	
Maximum clock pulse frequency	5	f _{max}	5	10	MHz	
	10		12	25	MHz	
	15		17	35	MHz	

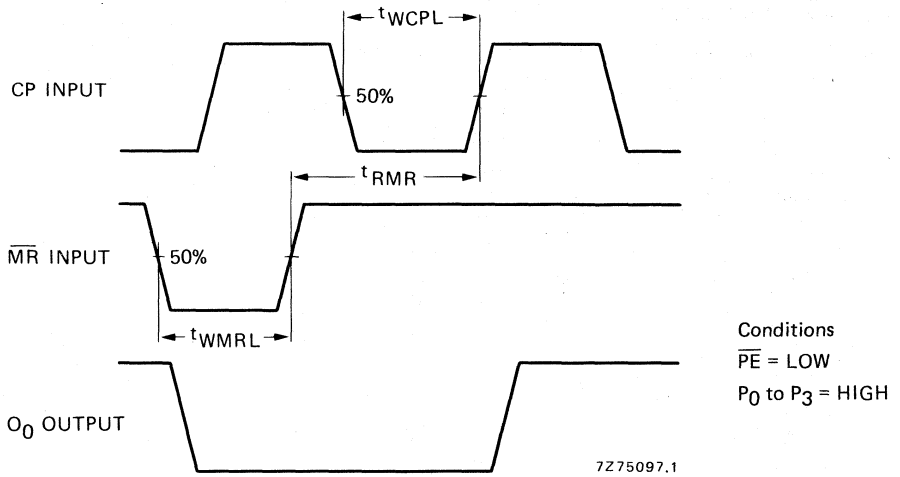


Fig. 5 Waveforms showing minimum CP and \overline{MR} pulse widths and \overline{MR} to CP recovery time.

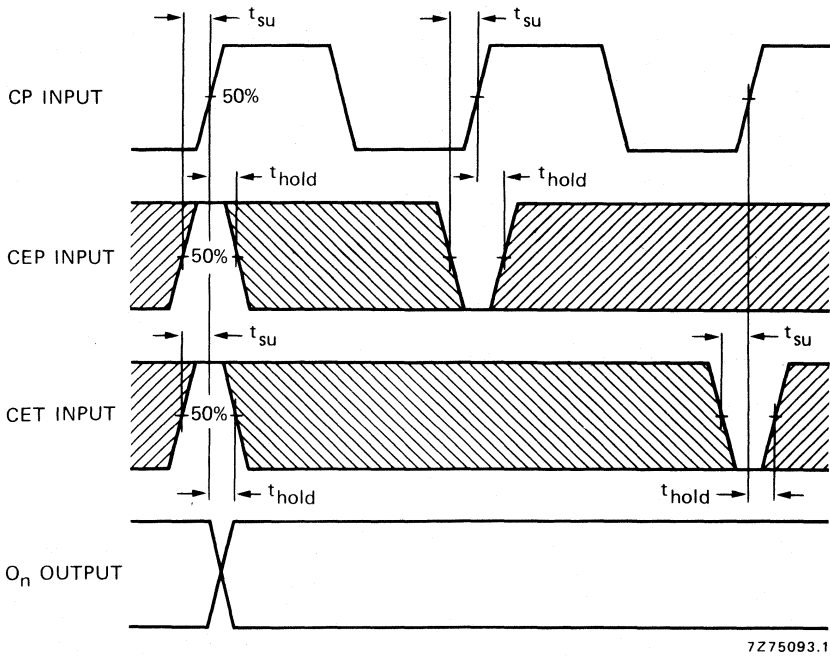
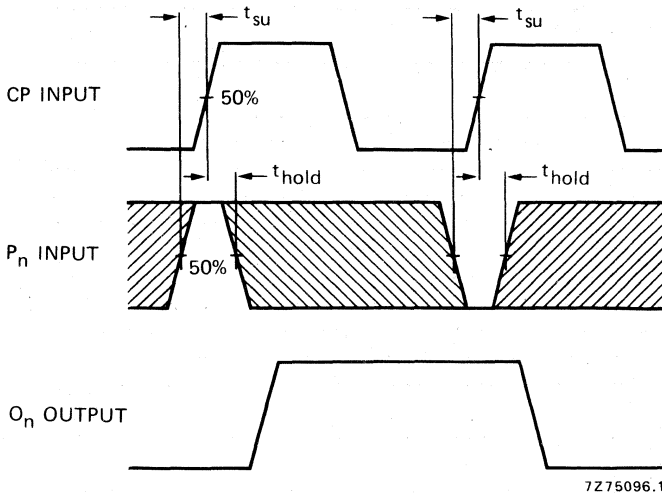


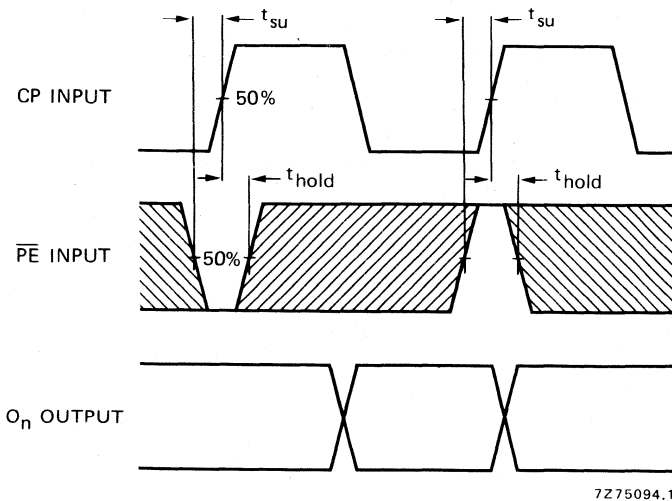
Fig. 6 Waveforms showing set-up times and hold times for CEP and CET inputs.

Conditions: $\overline{PE} = \overline{MR} = \text{HIGH}$.



Conditions
 $\overline{PE} = \text{LOW}$
 $\overline{MR} = \text{HIGH}$

Fig. 7 Waveforms showing set-up times and hold times for P_n inputs.



Condition
 $\overline{MR} = \text{HIGH}$

Fig. 8 Waveforms showing set-up times and hold times for \overline{PE} inputs.

Note

Set-up and hold times are shown as positive values but may be specified as negative values.

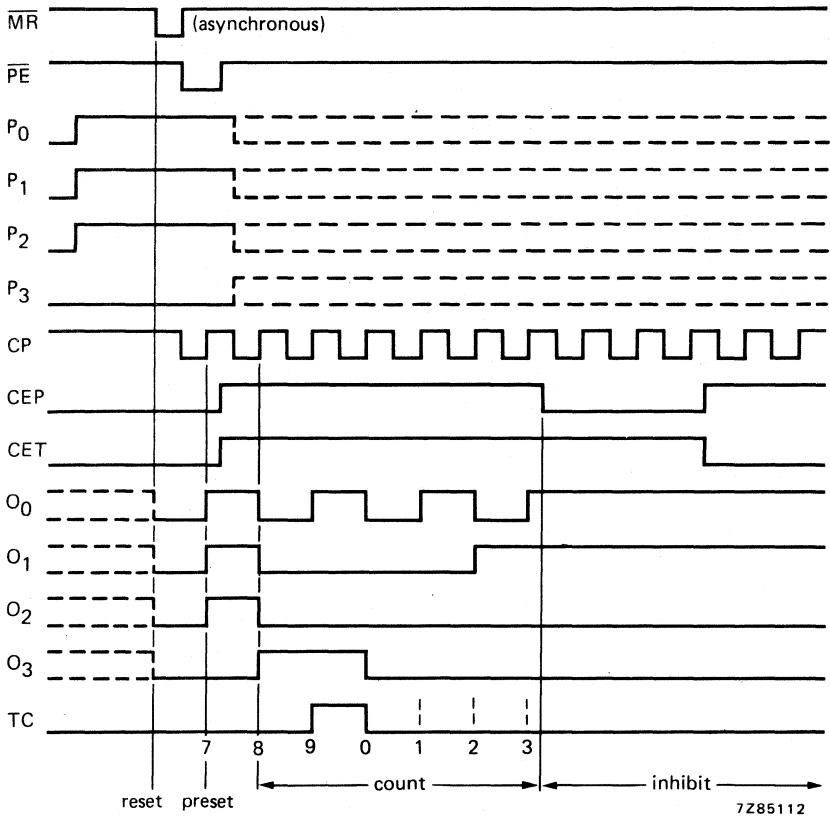
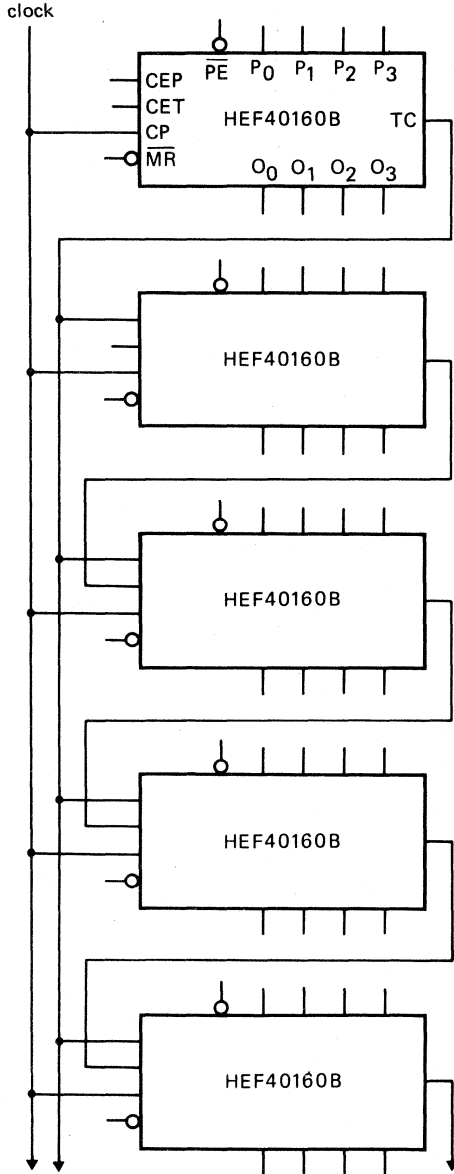


Fig. 9 Timing diagram.

APPLICATION INFORMATION

An example of an application for the HEF40160B is:

- Programmable decade counter.



NOTE

On the TC outputs, glitches can occur during counting. In totally synchronous mode they will not have any adverse affect. However the TC output in asynchronous mode can cause problems.

Fig. 10 Synchronous multi-stage counting scheme.

7285114

4-BIT SYNCHRONOUS BINARY COUNTER WITH ASYNCHRONOUS RESET



The HEF40161B is a fully synchronous edge-triggered 4-bit binary counter with a clock input (CP), an overriding asynchronous master reset (\overline{MR}), four parallel data inputs (P_0 to P_3), three synchronous mode control inputs (parallel enable (PE), count enable parallel (CEP) and count enable trickle (CET)), buffered outputs from all four bit positions (O_0 to O_3) and a terminal count output (TC).

Operation is fully synchronous (except for the \overline{MR} input) and occurs on the LOW to HIGH transition of CP. When \overline{PE} is LOW, the next LOW to HIGH transition of CP loads data into the counter from P_0 to P_3 regardless of the levels of CEP and CET inputs.

When \overline{PE} is HIGH, the next LOW to HIGH transition of CP advances the counter to its next state only if both CEP and CET are HIGH; otherwise, no change occurs in the state of the counter. TC is HIGH when the state of the counter is 15 (O_1 to O_3 = HIGH) and when CET is HIGH. A LOW on \overline{MR} sets all outputs (O_0 to O_3 and TC) LOW, independent of the state of all other inputs. Multistage synchronous counting is possible without additional components by using a carry look-ahead counting technique; in this case, TC is used to enable successive cascaded stages. CEP, CET and PE must be stable only during the set-up time before the LOW to HIGH transition of CP.

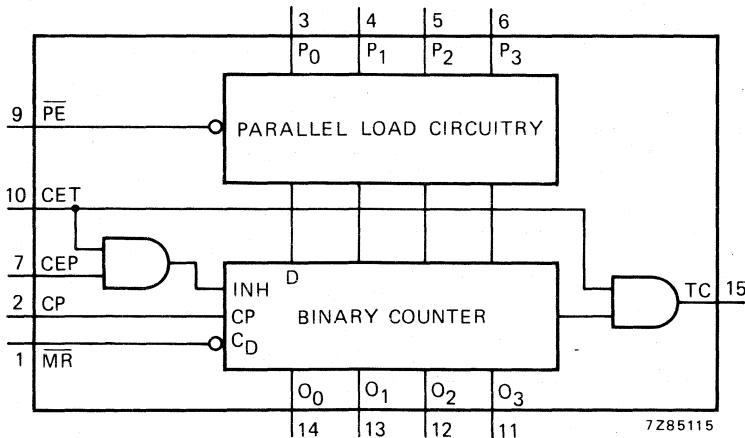
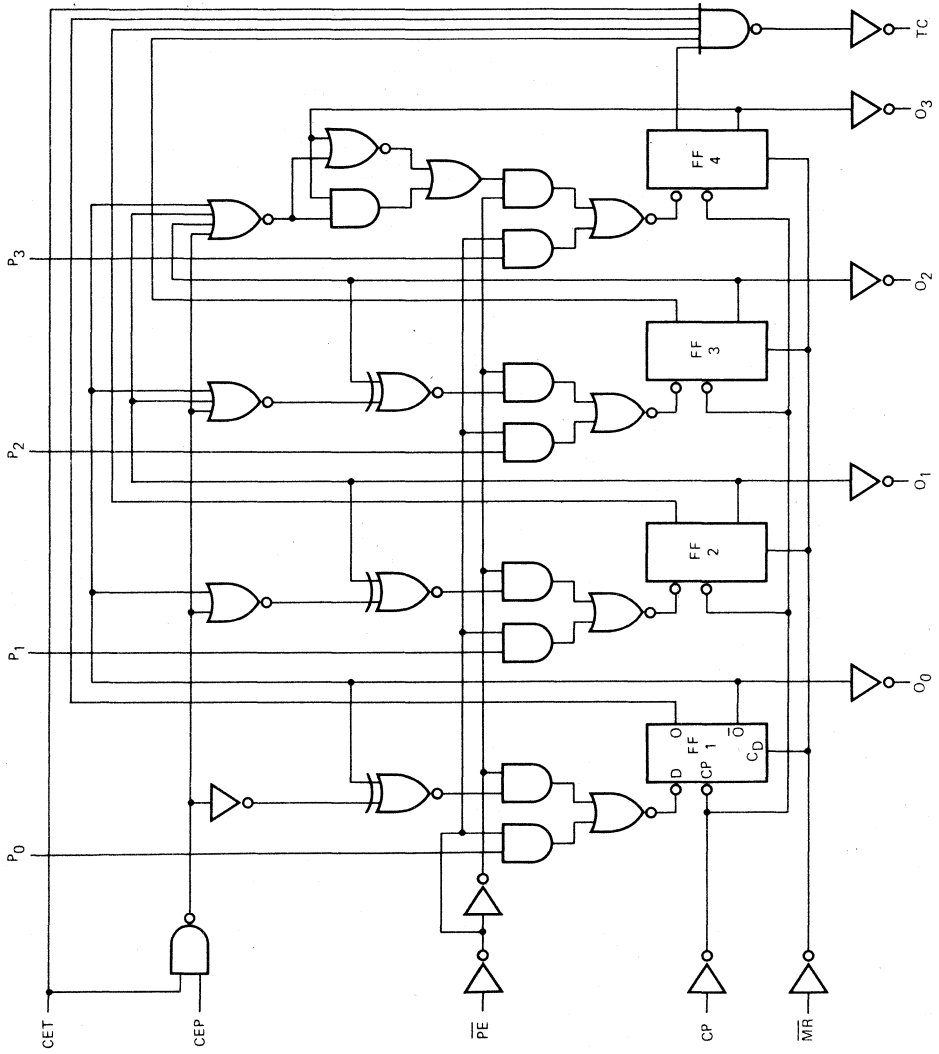


Fig. 1 Functional diagram.

FAMILY DATA

I_{DD} LIMITS category MSI

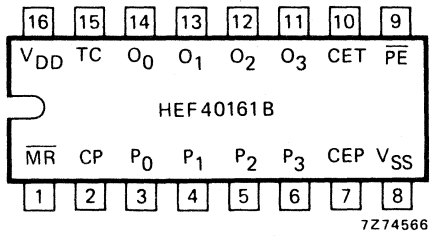
see Family Specifications



7775084.1

Fig. 2 Logic diagram.





PINNING

- \overline{PE} parallel enable input
- P_0 to P_3 parallel data inputs
- CEP count enable parallel input
- CET count enable trickle input
- CP clock input (LOW to HIGH, edge-triggered)
- \overline{MR} master reset input (active LOW)
- O_0 to O_3 parallel outputs
- TC terminal count output

Fig. 3 Pinning diagram.

HEF40161BP: 16-lead DIL; plastic (SOT-38Z).
 HEF40161BD: 16-lead DIL; ceramic (SOT-74).
 HEF40161BT: 16-lead flat pack; plastic (SO-16; SOT-109A)

SYNCHRONOUS MODE SELECTION

\overline{PE}	CEP	CET	mode
L	X	X	preset
H	L	X	no change
H	X	L	no change
H	H	H	count

TERMINAL COUNT GENERATION

CET	$(O_0 \cdot O_1 \cdot O_2 \cdot O_3)$	TC
L	L	L
L	H	L
H	L	L
H	H	H

\overline{MR} = HIGH

H = HIGH state (the more positive voltage)
 L = LOW state (the less positive voltage)
 X = state is immaterial

$$TC = CET \cdot O_0 \cdot O_1 \cdot O_2 \cdot O_3$$

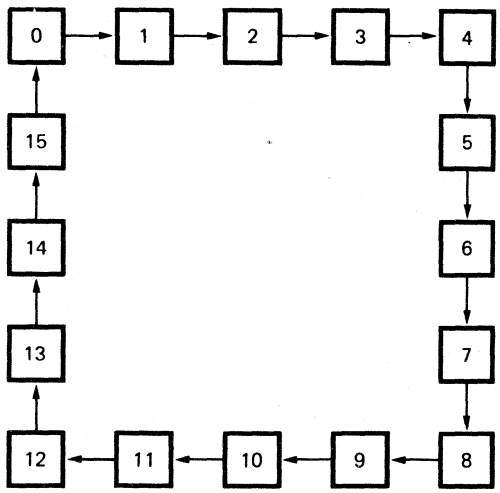


Fig. 4 State diagram.

7Z75087

A.C. CHARACTERISTICS

 $V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	typical formula for P (μW)	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
Dynamic power dissipation per package (P)	5	$1\,200 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	10	$5\,600 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$16\,000 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

A.C. CHARACTERISTICS

 $V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	symbol	min.	typ.	max.	typical extrapolation formula	
Propagation delays $CP \rightarrow O_n$ HIGH to LOW	5			110	220	ns	$83\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10	t _{PHL}		45	90	ns	$34\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			30	60	ns	$22\text{ ns} + (0,16\text{ ns/pF}) C_L$
LOW to HIGH	5			115	230	ns	$88\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10	t _{PLH}		45	95	ns	$34\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			35	65	ns	$27\text{ ns} + (0,16\text{ ns/pF}) C_L$
$CP \rightarrow TC$ HIGH to LOW	5			130	260	ns	$103\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10	t _{PHL}		55	105	ns	$44\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			35	75	ns	$27\text{ ns} + (0,16\text{ ns/pF}) C_L$
LOW to HIGH	5			140	280	ns	$113\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10	t _{PLH}		55	115	ns	$44\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			40	80	ns	$32\text{ ns} + (0,16\text{ ns/pF}) C_L$
$CET \rightarrow TC$ HIGH to LOW	5			105	210	ns	$78\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10	t _{PHL}		50	100	ns	$39\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			35	75	ns	$27\text{ ns} + (0,16\text{ ns/pF}) C_L$
LOW to HIGH	5			90	185	ns	$63\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10	t _{PLH}		35	70	ns	$24\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			25	50	ns	$17\text{ ns} + (0,16\text{ ns/pF}) C_L$
$\overline{MR} \rightarrow O_n$ HIGH to LOW	5			120	245	ns	$93\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10	t _{PHL}		50	100	ns	$39\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			35	70	ns	$27\text{ ns} + (0,16\text{ ns/pF}) C_L$
$\overline{MR} \rightarrow TC$ HIGH to LOW	5			145	295	ns	$118\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10	t _{PHL}		60	120	ns	$49\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			45	85	ns	$37\text{ ns} + (0,16\text{ ns/pF}) C_L$
Output transition times HIGH to LOW	5			60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$
	10	t _{THL}		30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$
	15			20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$
LOW to HIGH	5			60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$
	10	t _{TLH}		30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$
	15			20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$

A.C. CHARACTERISTICS

 $V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	symbol	min.	typ.	max.	
Minimum clock pulse width; LOW	5		100	50	ns	see also waveforms Figs 5, 6, 7 and 8
	10	t_{WCPL}	40	20	ns	
	15		30	15	ns	
Minimum \overline{MR} pulse width; LOW	5		100	50	ns	
	10	t_{WMRL}	40	20	ns	
	15		30	15	ns	
Recovery time for \overline{MR}	5		25	0	ns	
	10	t_{RMR}	15	0	ns	
	15		10	0	ns	
Set-up times $P_n \rightarrow CP$	5		110	55	ns	
	10	t_{su}	40	20	ns	
	15		30	15	ns	
$\overline{PE} \rightarrow CP$	5		120	60	ns	
	10	t_{su}	40	20	ns	
	15		25	10	ns	
$CEP, CET \rightarrow CP$	5		260	130	ns	
	10	t_{su}	100	50	ns	
	15		70	35	ns	
Hold times $P_n \rightarrow CP$	5		20	-35	ns	
	10	t_{hold}	10	-10	ns	
	15		5	-10	ns	
$\overline{PE} \rightarrow CP$	5		15	-45	ns	
	10	t_{hold}	5	-15	ns	
	15		5	-10	ns	
$CEP, CET \rightarrow CP$	5		25	-105	ns	
	10	t_{hold}	15	-35	ns	
	15		10	-25	ns	
Maximum clock pulse frequency	5		5	10	MHz	
	10	f_{max}	12	25	MHz	
	15		17	35	MHz	

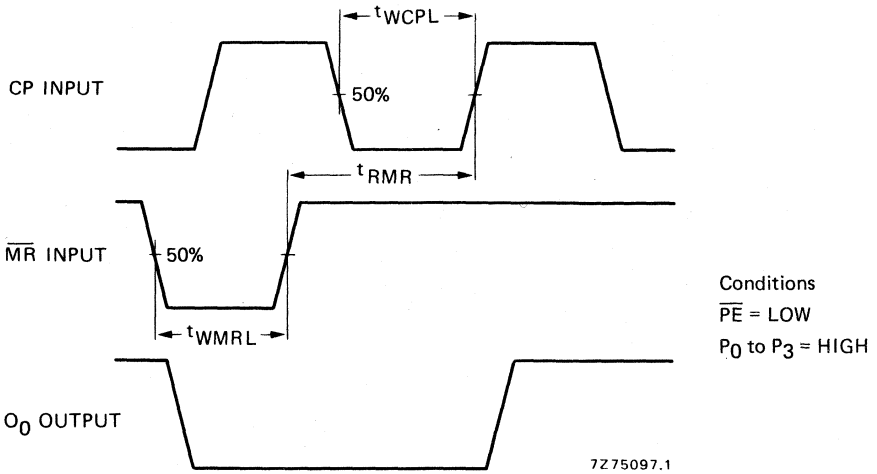


Fig. 5 Waveforms showing minimum CP and \overline{MR} pulse widths and \overline{MR} to CP recovery time.

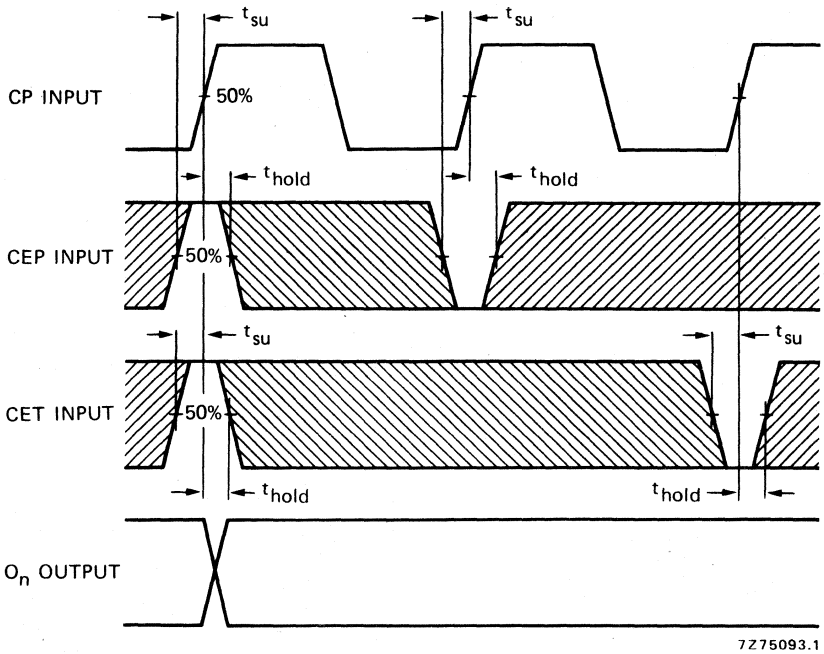
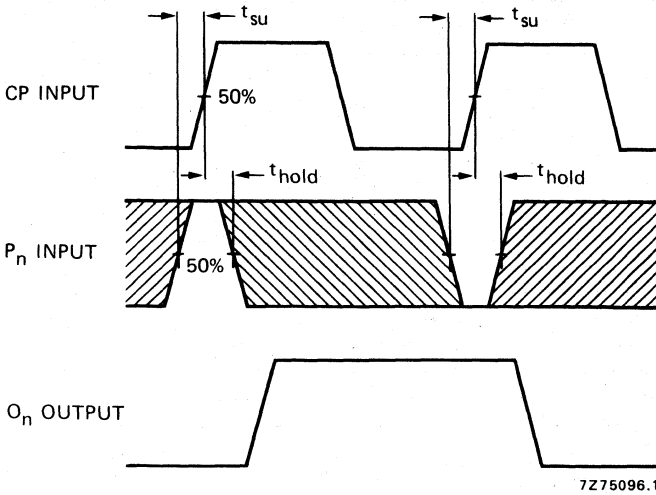
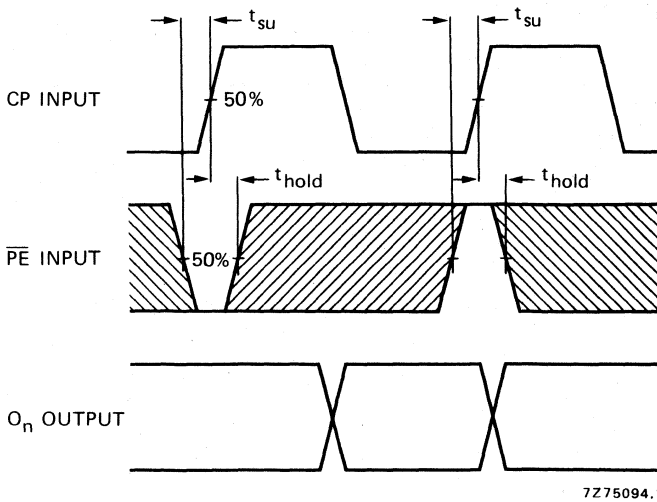


Fig. 6 Waveforms showing set-up times and hold times for CEP and CET inputs.
 Condition: $\overline{PE} = \overline{MR} = \text{HIGH}$.



Conditions
 $\overline{PE} = \text{LOW}$
 $\overline{MR} = \text{HIGH}$

Fig. 7 Waveforms showing set-up times and hold times for P_n inputs.



Condition
 $\overline{MR} = \text{HIGH}$

Fig. 8 Waveforms showing set-up times and hold times for \overline{PE} input.

Note

Set-up and hold times are shown as positive values but may be specified as negative values.

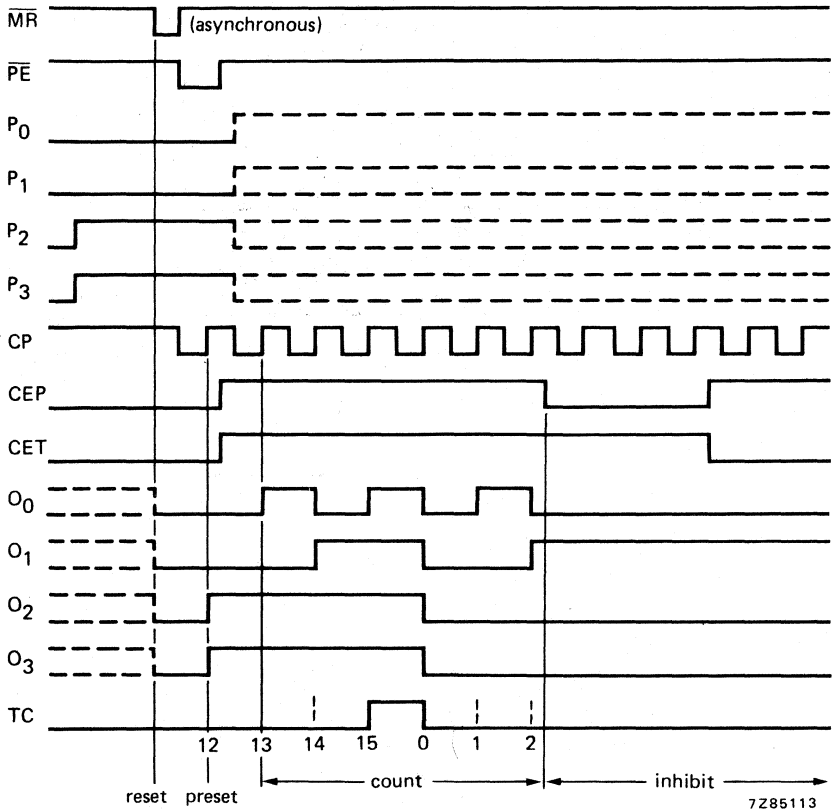
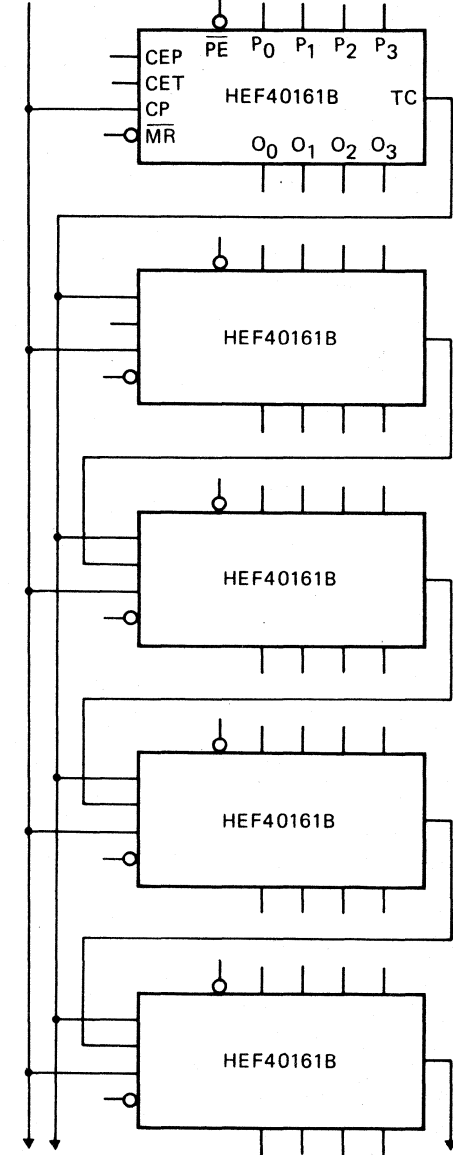


Fig. 9 Timing diagram.

APPLICATION INFORMATION

An example of an application for the HEF40161B is:

- Programmable binary counter.



NOTE

On the TC outputs, glitches can occur during counting. In totally synchronous mode they will not have any adverse affect. However the TC output in asynchronous mode can cause problems.

Fig. 10 Synchronous multi-stage counting scheme.

7285119

4-BIT SYNCHRONOUS DECADE COUNTER WITH SYNCHRONOUS RESET



The HEF40162B is a fully synchronous edge-triggered 4-bit decade counter with a clock input (CP), four synchronous parallel data inputs (P_0 to P_3), four synchronous mode control inputs (parallel enable (\overline{PE}), count enable parallel (CEP), count enable trickle (CET) and synchronous reset (\overline{SR}), buffered outputs from all four bit positions (O_0 to O_3) and a terminal count output (TC).

Operation is synchronous and occurs on the LOW to HIGH transition of CP. When \overline{PE} is LOW, the next LOW to HIGH transition of CP loads data into the counter from P_0 to P_3 . When \overline{PE} is HIGH, the next LOW to HIGH transition of CP advances the counter to its next state only if both CEP and CET are HIGH; otherwise no change occurs in the state of the counter. TC is HIGH when the state of the counter is 9 ($O_0 = O_3 = \text{HIGH}$, $O_1 = O_2 = \text{LOW}$) and when CET is HIGH. A LOW on \overline{SR} sets all outputs (O_0 to O_3 and TC) LOW on the next LOW to HIGH transition of CP, independent of the state of all other synchronous mode control inputs (CEP, CET and \overline{PE}). Multistage synchronous counting is possible without additional components by using a carry look-ahead counting technique; in this case, TC is used to enable successive cascaded stages. CEP, CET, \overline{PE} and \overline{SR} must be stable only during the set-up time before the LOW to HIGH transition of CP.

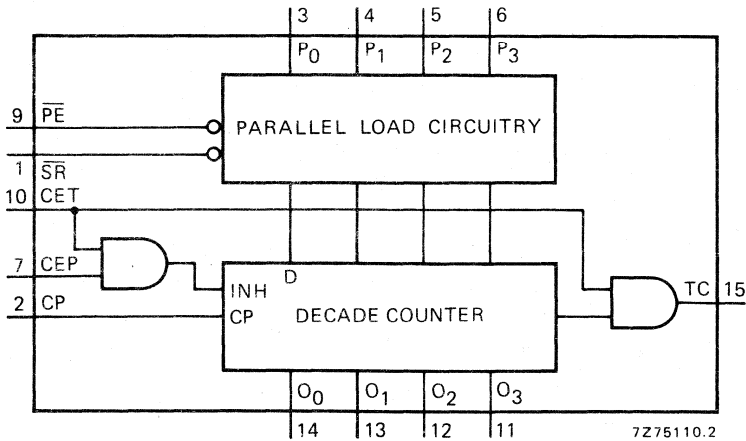
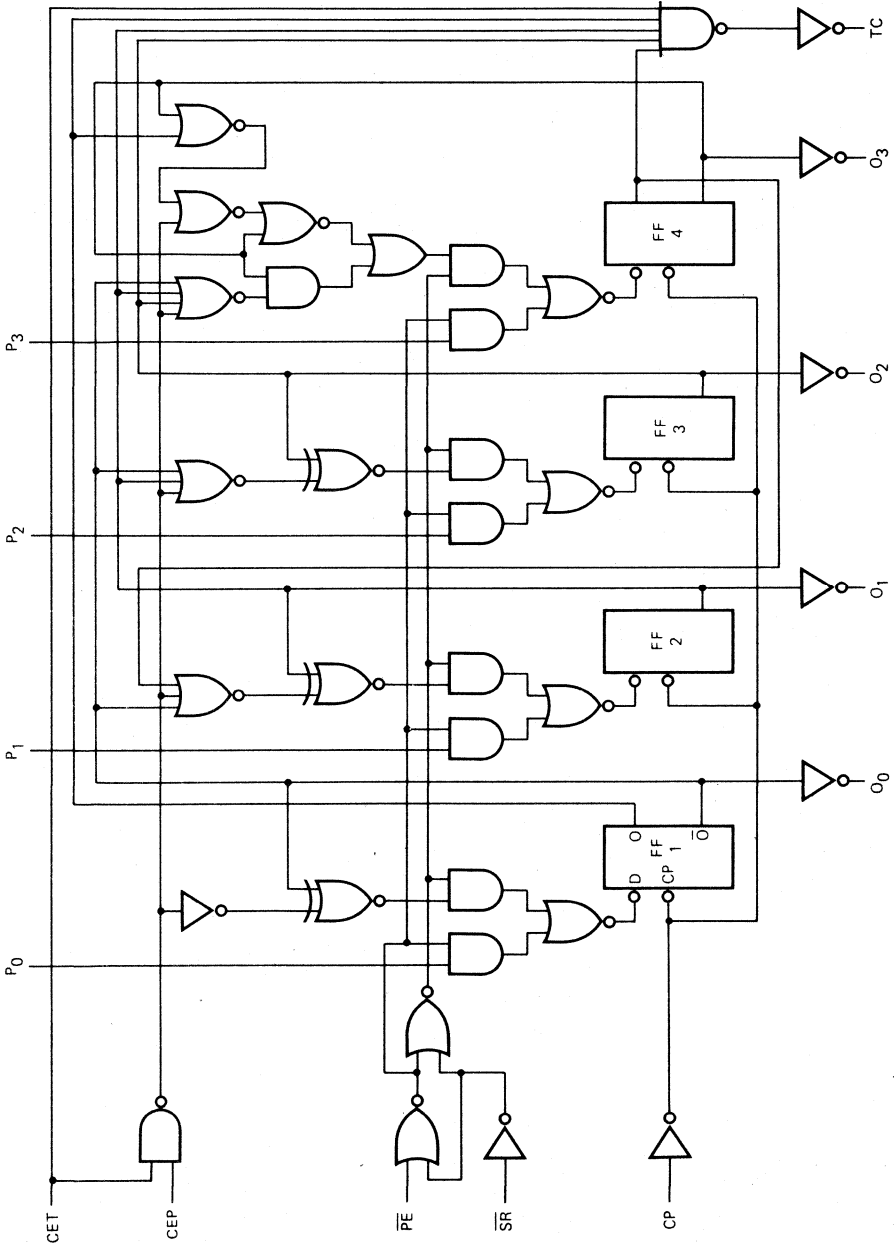


Fig. 1 Functional diagram.

FAMILY DATA

I_{DD} LIMITS category MSI

see Family Specifications



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Fig. 2 Logic diagram.

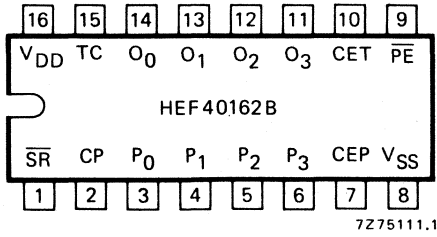


Fig. 3 Pinning diagram.

PINNING

- PE parallel enable input
- P₀ to P₃ parallel data inputs
- CEP count enable parallel input
- CET count enable trickle input
- CP clock input (LOW to HIGH, edge-triggered)
- SR synchronous reset input (active LOW)
- O₀ to O₃ parallel outputs
- TC terminal count output

HEF40162BP: 16-lead DIL; plastic (SOT-38Z).
 HEF40162BD: 16-lead DIL; ceramic (SOT-74).
 HEF40162BT: 16-lead flat pack; plastic (SO-16; SOT-109A).

SYNCHRONOUS MODE SELECTION

SR	PE	CEP	CET	mode
H	L	X	X	preset
H	H	L	X	no change
H	H	X	L	no change
H	H	H	H	count
L	X	X	X	reset

H = HIGH state (the more positive voltage)
 L = LOW state (the less positive voltage)
 X = state is immaterial

TERMINAL COUNT GENERATION

CET	(O ₀ · \bar{O}_1 · \bar{O}_2 · O ₃)	TC
L	L	L
L	H	L
H	L	L
H	H	H

$$TC = CET \cdot O_0 \cdot \bar{O}_1 \cdot \bar{O}_2 \cdot O_3$$

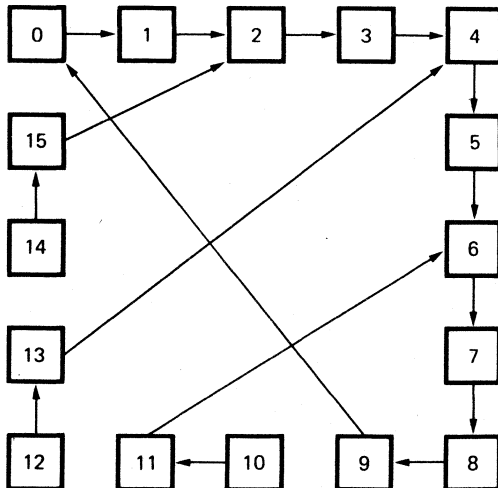


Fig. 4 State diagram.

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A.C. CHARACTERISTICS

 $V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$1\,200 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz)
	10	$5\,600 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_o = output freq. (MHz)
	15	$16\,000 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	C_L = load capacitance (pF)
			$\Sigma(f_o C_L)$ = sum of outputs
			V_{DD} = supply voltage (V)

A.C. CHARACTERISTICS

 $V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	symbol	min.	typ.	max.	typical extrapolation formula	
Propagation delays CP \rightarrow O_n HIGH to LOW	5	t _{PHL}		110	220	ns	83 ns + (0,55 ns/pF) C_L
	10		45	90	ns	34 ns + (0,23 ns/pF) C_L	
	15		30	60	ns	22 ns + (0,16 ns/pF) C_L	
LOW to HIGH	5	t _{PLH}		115	230	ns	88 ns + (0,55 ns/pF) C_L
	10		45	95	ns	34 ns + (0,23 ns/pF) C_L	
	15		35	65	ns	27 ns + (0,16 ns/pF) C_L	
CP \rightarrow TC HIGH to LOW	5	t _{PHL}		130	260	ns	103 ns + (0,55 ns/pF) C_L
	10		55	105	ns	44 ns + (0,23 ns/pF) C_L	
	15		35	75	ns	27 ns + (0,16 ns/pF) C_L	
LOW to HIGH	5	t _{PLH}		140	280	ns	113 ns + (0,55 ns/pF) C_L
	10		55	115	ns	44 ns + (0,23 ns/pF) C_L	
	15		40	80	ns	32 ns + (0,16 ns/pF) C_L	
CET \rightarrow TC HIGH to LOW	5	t _{PHL}		105	210	ns	78 ns + (0,55 ns/pF) C_L
	10		50	100	ns	39 ns + (0,23 ns/pF) C_L	
	15		35	75	ns	27 ns + (0,16 ns/pF) C_L	
LOW to HIGH	5	t _{PLH}		90	185	ns	63 ns + (0,55 ns/pF) C_L
	10		35	70	ns	24 ns + (0,23 ns/pF) C_L	
	15		25	50	ns	17 ns + (0,16 ns/pF) C_L	
Output transition times HIGH to LOW	5	t _{THL}		60	120	ns	10 ns + (1,0 ns/pF) C_L
	10		30	60	ns	9 ns + (0,42 ns/pF) C_L	
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L	
LOW to HIGH	5	t _{TLH}		60	120	ns	10 ns + (1,0 ns/pF) C_L
	10		30	60	ns	9 ns + (0,42 ns/pF) C_L	
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L	

A.C. CHARACTERISTICS

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	symbol	min.	typ.	max.	
Minimum clock pulse width; LOW	5	t_{WCPL}	100	50	ns	see also waveforms Figs 5, 6, 7 and 8
	10		40	20	ns	
	15		30	15	ns	
Set-up times $P_n \rightarrow CP$	5	t_{su}	110	55	ns	
	10		40	20	ns	
	15		30	15	ns	
$\overline{PE} \rightarrow CP$	5	t_{su}	120	60	ns	
	10		40	20	ns	
	15		25	10	ns	
CEP, CET $\rightarrow CP$	5	t_{su}	260	130	ns	
	10		100	50	ns	
	15		70	35	ns	
$\overline{SR} \rightarrow CP$	5	t_{su}	50	25	ns	
	10		20	10	ns	
	15		15	10	ns	
Hold times $P_n \rightarrow CP$	5	t_{hold}	20	-35	ns	
	10		10	-10	ns	
	15		5	-10	ns	
$\overline{PE} \rightarrow CP$	5	t_{hold}	15	-45	ns	
	10		5	-15	ns	
	15		5	-10	ns	
CEP, CET $\rightarrow CP$	5	t_{hold}	25	-105	ns	
	10		15	-35	ns	
	15		10	-25	ns	
$\overline{SR} \rightarrow CP$	5	t_{hold}	15	-10	ns	
	10		5	-5	ns	
	15		5	0	ns	
Maximum clock pulse frequency	5	f_{max}	5	10	MHz	
	10		12	25	MHz	
	15		17	35	MHz	

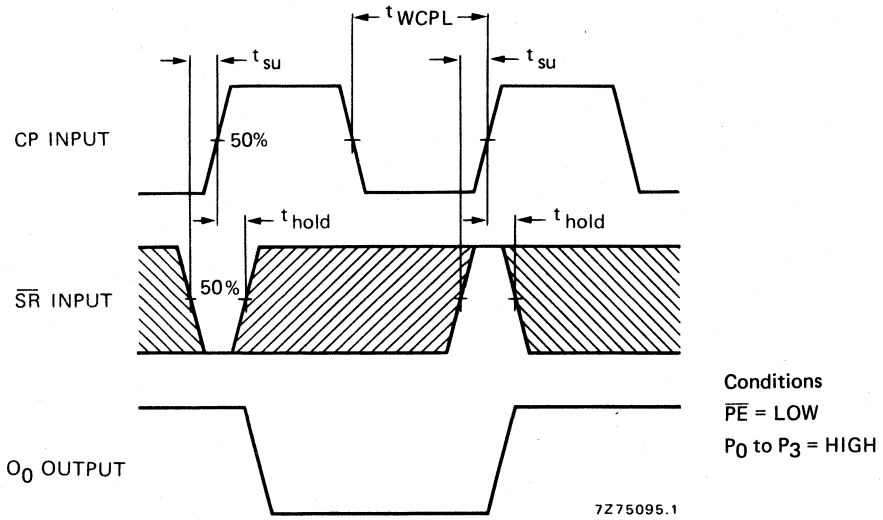


Fig. 5 Waveforms showing set-up times and hold times for \overline{SR} input and minimum CP pulse width.

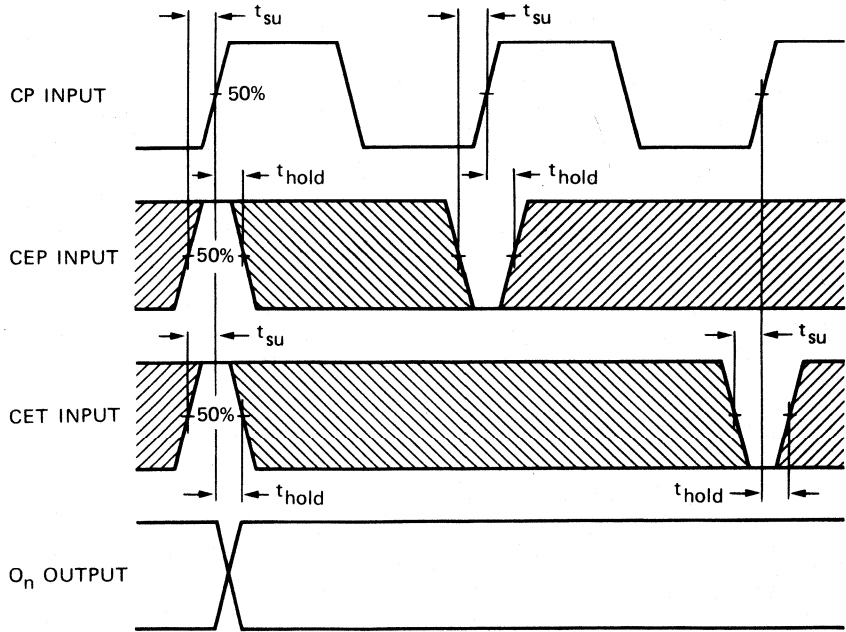
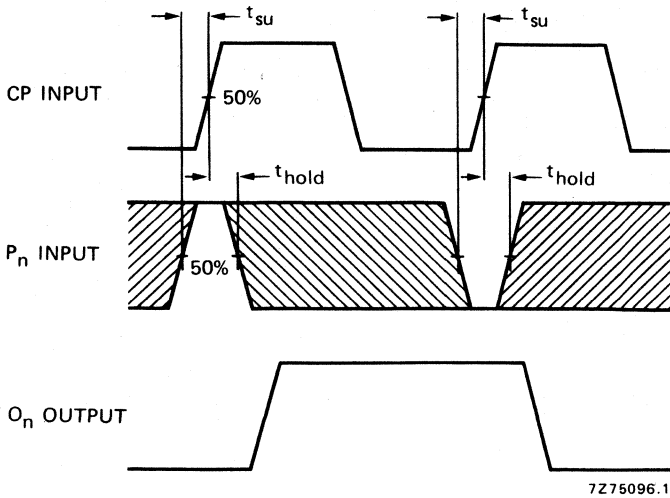


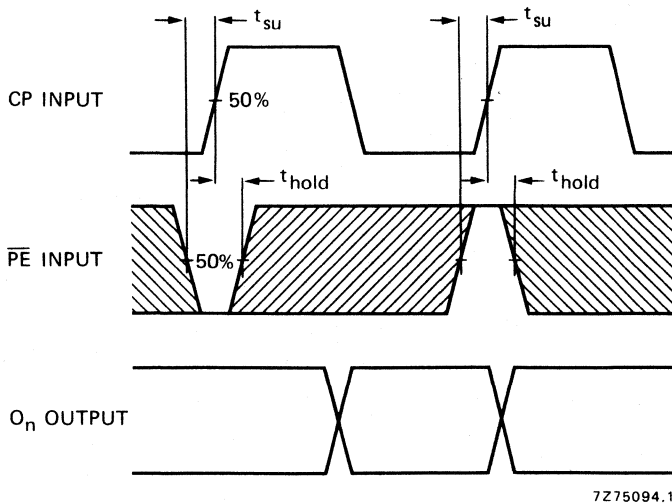
Fig. 6 Waveforms showing set-up times and hold times for CEP and CET inputs.

Condition: $\overline{PE} = \overline{SR} = \text{HIGH}$.



Conditions
PE = LOW
SR = HIGH

Fig. 7 Waveforms showing set-up times and hold times for P_n inputs.



Condition
SR = HIGH

Fig. 8 Waveforms showing set-up times and hold times for PE input.

Note

Set-up and hold times are shown as positive values but may be specified as negative values.

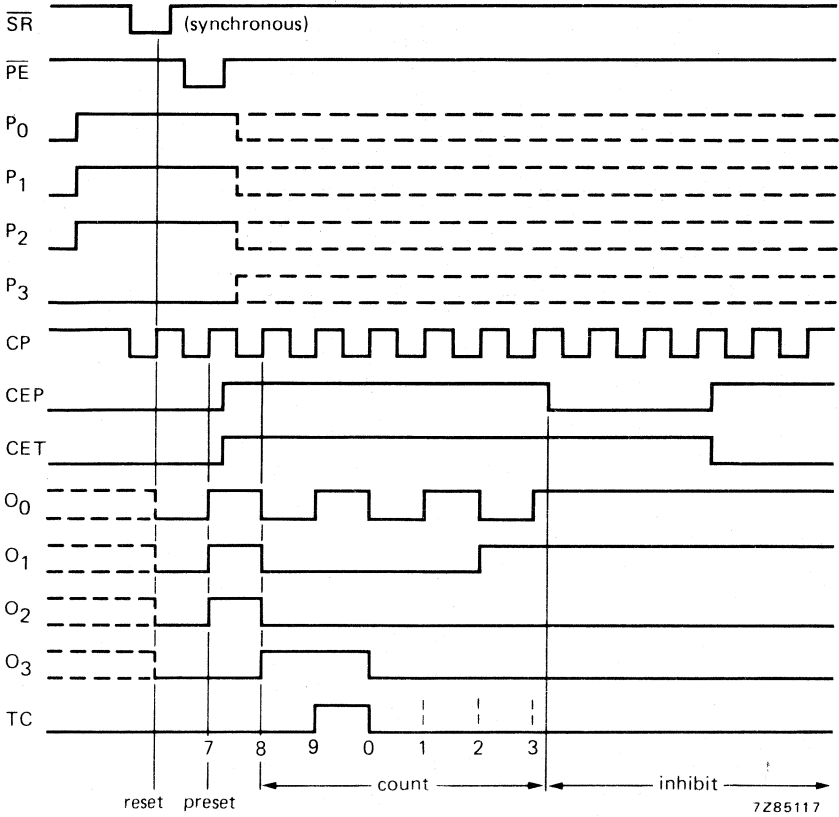
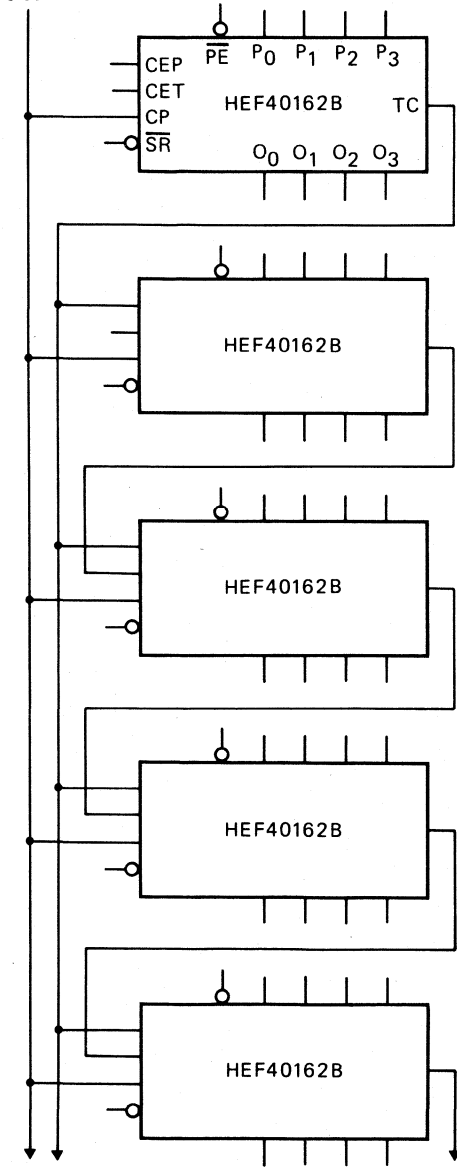


Fig. 9 Timing diagram.

APPLICATION INFORMATION

An example of an application for the HEF40162B is:

- Programmable decade counter.



NOTE

On the TC outputs, glitches can occur during counting. In totally synchronous mode they will not have any adverse affect. However the TC output in asynchronous mode can cause problems.

Fig. 10 Synchronous multi-stage counting scheme.

7Z85120

4-BIT SYNCHRONOUS BINARY COUNTER WITH SYNCHRONOUS RESET



The HEF40163B is a fully synchronous edge-triggered 4-bit binary counter with a clock input (CP), four synchronous parallel data inputs (P_0 to P_3), four synchronous mode control inputs (parallel enable (\overline{PE}), count enable parallel (CEP), count enable trickle (CET) and synchronous reset (\overline{SR}), buffered outputs from all four bit positions (O_0 to O_3) and a terminal count output (TC).

Operation is fully synchronous and occurs on the LOW to HIGH transition of CP. When \overline{PE} is LOW, the next LOW to HIGH transition of CP loads data into the counter from P_0 to P_3 . When \overline{PE} is HIGH, the next LOW to HIGH transition of CP advances the counter to its next state only if both CEP and CET are HIGH; otherwise no change occurs in the state of the counter. TC is HIGH when the state of the counter is 15 (O_0 to O_3 = HIGH) and when CET is HIGH. A LOW on \overline{SR} sets all outputs (O_0 to O_3 and TC) LOW on the next LOW to HIGH transition of CP, independent of the state of all other synchronous mode control inputs (CEP, CET and \overline{PE}). Multistage synchronous counting is possible without additional components by using a carry look-ahead counting technique; in this case, TC is used to enable successive cascaded stages. CEP, CET, \overline{PE} and \overline{SR} must be stable only during the set-up time before the LOW to HIGH transition of CP.

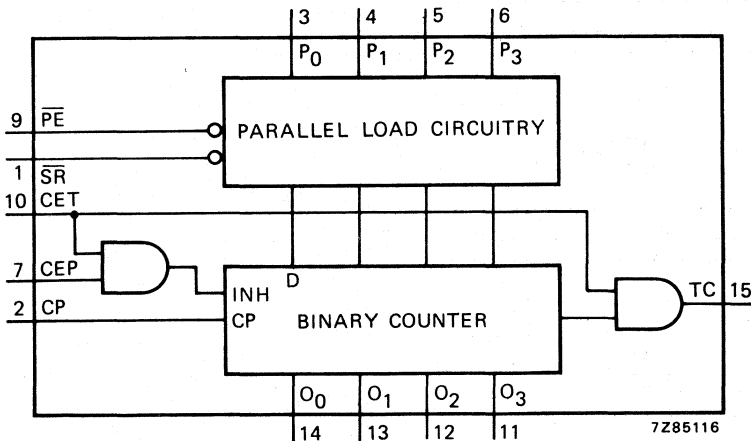


Fig. 1 Functional diagram.

FAMILY DATA

I_{DD} LIMITS category MSI

see Family Specifications

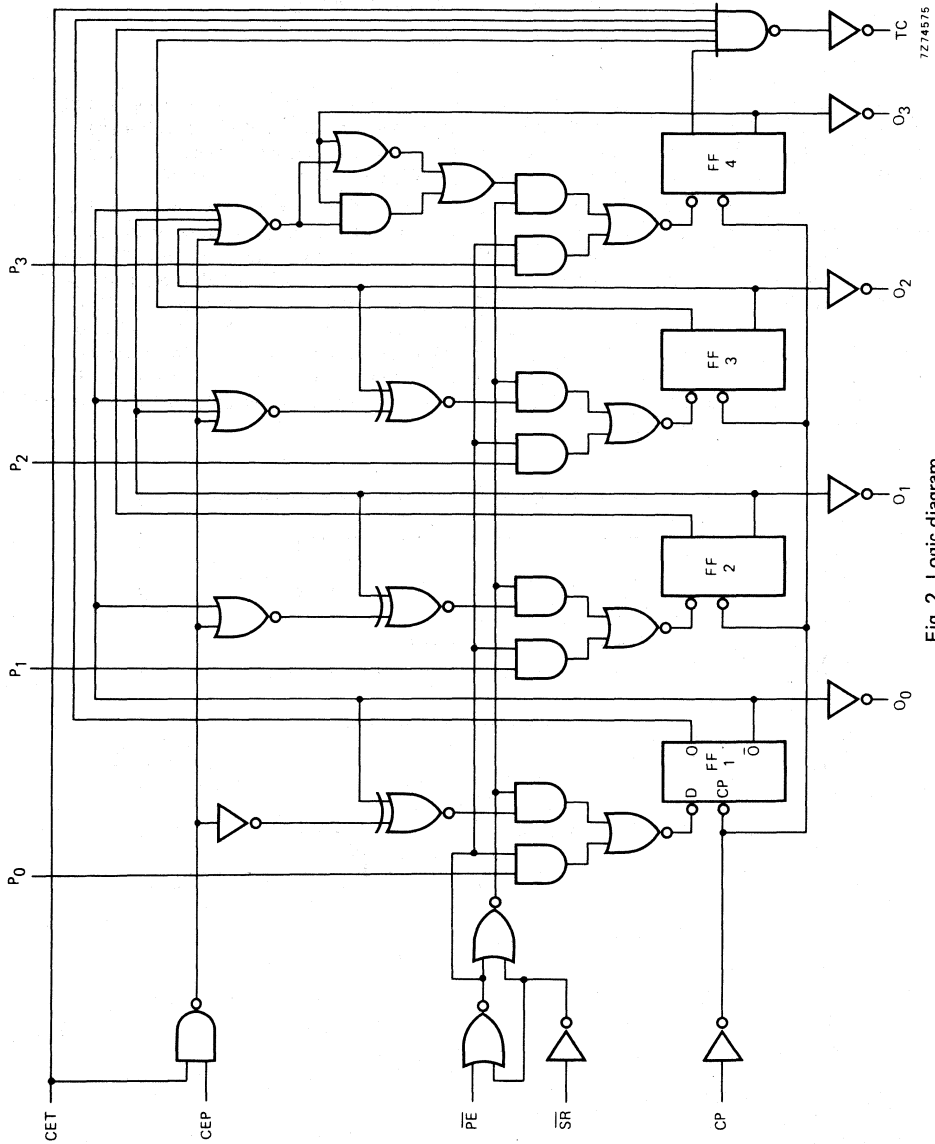


Fig. 2 Logic diagram.

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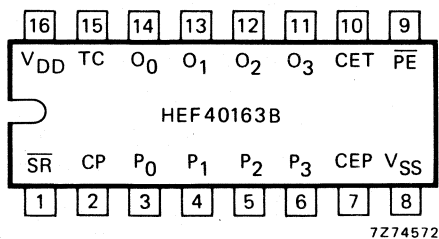


Fig. 3 Pinning diagram.

PINNING

- PE parallel enable input
- P₀ to P₃ parallel data inputs
- CEP count enable parallel input
- CET count enable trickle input
- CP clock input (LOW to HIGH, edge-triggered)
- SR-bar synchronous reset input (active LOW)
- O₀ to O₃ parallel outputs
- TC terminal count output

HEF40163BP: 16-lead DIL; plastic (SOT-38Z).
 HEF40163BD: 16-lead DIL; ceramic (SOT-74).
 HEF40163BT: 16-lead flat pack; plastic (SO-16; SOT-109A).

SYNCHRONOUS MODE SELECTION

SR-bar	PE-bar	CEP	CET	mode
H	L	X	X	preset
H	H	L	X	no change
H	H	X	L	no change
H	H	H	H	count
L	X	X	X	reset

H = HIGH state (the more positive voltage)
 L = LOW state (the less positive voltage)
 X = state is immaterial

TERMINAL COUNT GENERATION

CET	(O ₀ · O ₁ · O ₂ · O ₃)	TC
L	L	L
L	H	L
H	L	L
H	H	H

$$TC = CET \cdot O_0 \cdot O_1 \cdot O_2 \cdot O_3$$

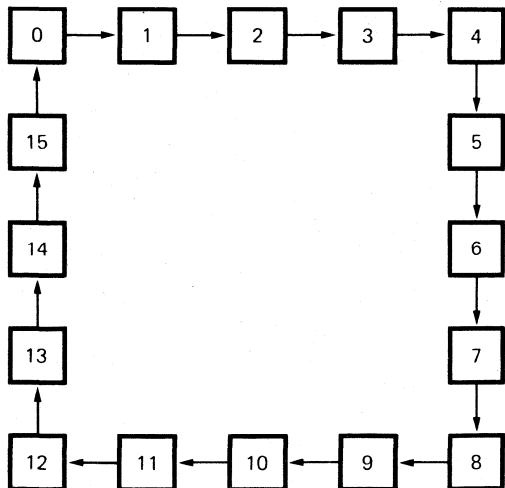


Fig. 4 State diagram.

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A.C. CHARACTERISTICS

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	typical formula for P (μW)	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
Dynamic power dissipation per package (P)	5	$1\,200 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	10	$5\,600 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$16\,000 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

A.C. CHARACTERISTICS

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	symbol	min.	typ.	max.	typical extrapolation formula	
Propagation delays $CP \rightarrow O_n$ HIGH to LOW	5	t _{PHL}		110	220	ns	$83\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10		45	90	ns	$34\text{ ns} + (0,23\text{ ns/pF}) C_L$	
	15		30	60	ns	$22\text{ ns} + (0,16\text{ ns/pF}) C_L$	
LOW to HIGH	5	t _{PLH}		115	230	ns	$88\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10		45	95	ns	$34\text{ ns} + (0,23\text{ ns/pF}) C_L$	
	15		35	65	ns	$27\text{ ns} + (0,16\text{ ns/pF}) C_L$	
$CP \rightarrow TC$ HIGH to LOW	5	t _{PHL}		130	260	ns	$103\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10		55	105	ns	$44\text{ ns} + (0,23\text{ ns/pF}) C_L$	
	15		35	75	ns	$27\text{ ns} + (0,16\text{ ns/pF}) C_L$	
LOW to HIGH	5	t _{PLH}		140	280	ns	$113\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10		55	115	ns	$44\text{ ns} + (0,23\text{ ns/pF}) C_L$	
	15		40	80	ns	$32\text{ ns} + (0,16\text{ ns/pF}) C_L$	
$CET \rightarrow TC$ HIGH to LOW	5	t _{PHL}		105	210	ns	$78\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10		50	100	ns	$39\text{ ns} + (0,23\text{ ns/pF}) C_L$	
	15		35	75	ns	$27\text{ ns} + (0,16\text{ ns/pF}) C_L$	
LOW to HIGH	5	t _{PLH}		90	185	ns	$63\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10		35	70	ns	$24\text{ ns} + (0,23\text{ ns/pF}) C_L$	
	15		25	50	ns	$17\text{ ns} + (0,16\text{ ns/pF}) C_L$	
Output transition times HIGH to LOW	5	t _{THL}		60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$
	10		30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$	
	15		20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$	
LOW to HIGH	5	t _{TLH}		60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$
	10		30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$	
	15		20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$	

A.C. CHARACTERISTICS

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	symbol	min.	typ.	max.	
Minimum clock pulse width; LOW	5	t_{WCPL}	100	50	ns	} see also waveforms Figs 5, 6, 7 and 8
	10		40	20	ns	
	15		30	15	ns	
Set-up times $P_n \rightarrow CP$	5	t_{su}	110	55	ns	
	10		40	20	ns	
	15		30	15	ns	
$\overline{PE} \rightarrow CP$	5	t_{su}	120	60	ns	
	10		40	20	ns	
	15		25	10	ns	
CEP, CET $\rightarrow CP$	5	t_{su}	260	130	ns	
	10		100	50	ns	
	15		70	35	ns	
$\overline{SR} \rightarrow CP$	5	t_{su}	50	25	ns	
	10		20	10	ns	
	15		15	10	ns	
Hold times $P_n \rightarrow CP$	5	t_{hold}	20	-35	ns	
	10		10	-10	ns	
	15		5	-10	ns	
$\overline{PE} \rightarrow CP$	5	t_{hold}	15	-45	ns	
	10		5	-15	ns	
	15		5	-10	ns	
CEP, CET $\rightarrow CP$	5	t_{hold}	25	-105	ns	
	10		15	-35	ns	
	15		10	-25	ns	
$\overline{SR} \rightarrow CP$	5	t_{hold}	15	-10	ns	
	10		5	-5	ns	
	15		5	0	ns	
Maximum clock pulse frequency	5	f_{max}	5	10	MHz	
	10		12	25	MHz	
	15		17	35	MHz	

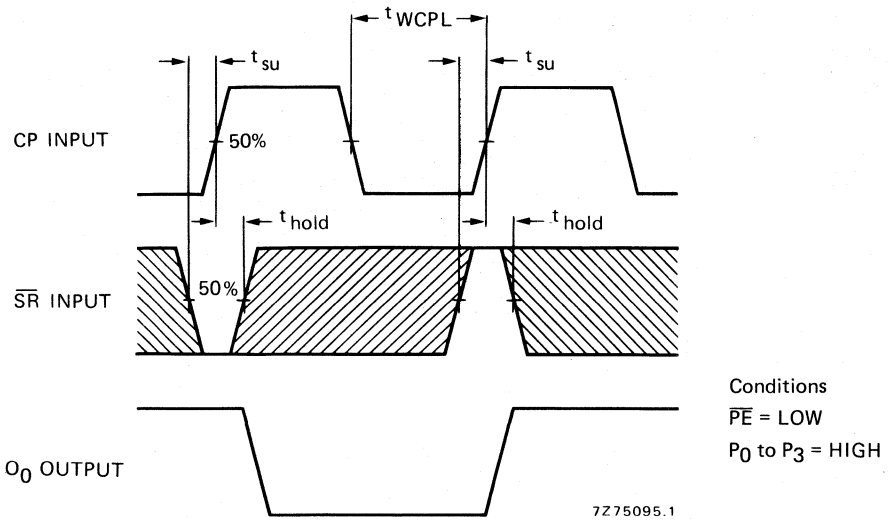


Fig. 5 Waveforms showing set-up and hold times for \overline{SR} input and minimum CP pulse width.

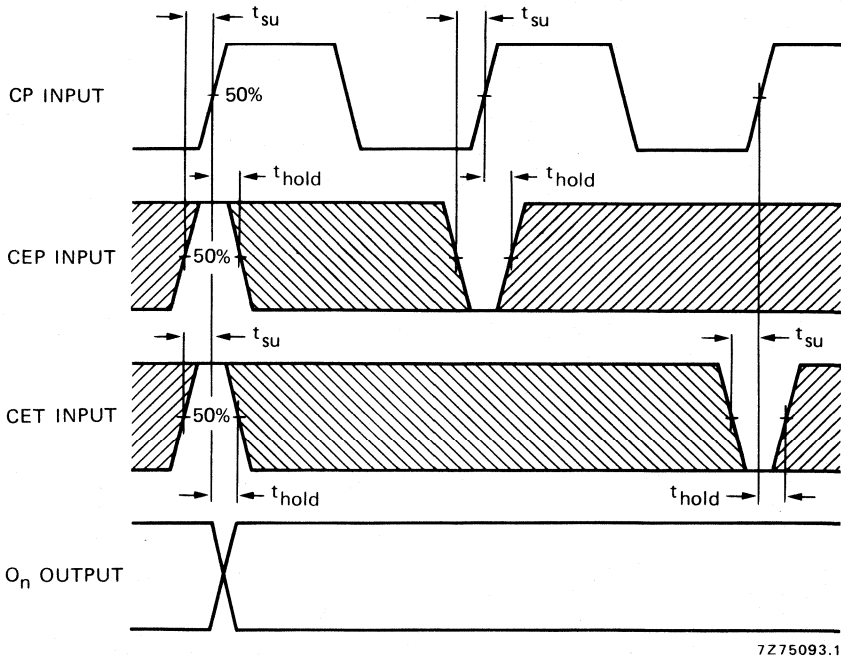
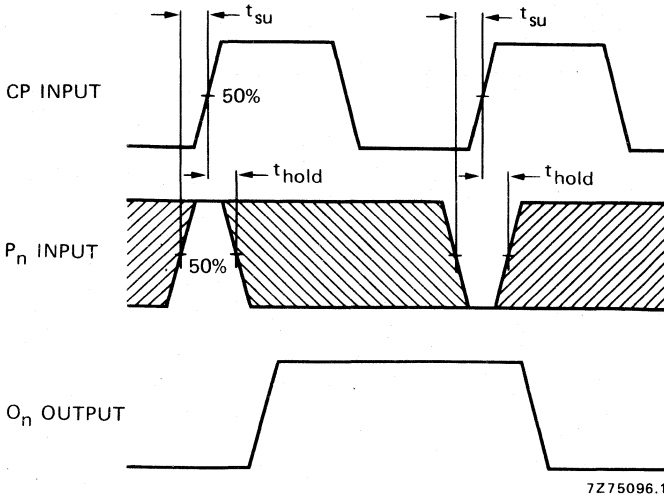


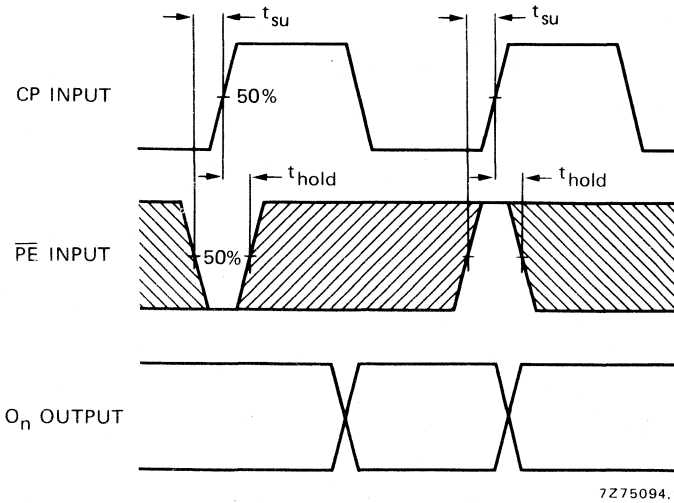
Fig. 6 Waveforms showing set-up times and hold times for CEP and CET inputs.

Condition: $\overline{PE} = \overline{SR} = \text{HIGH}$.



Conditions
 $\overline{PE} = \text{LOW}$
 $\overline{SR} = \text{HIGH}$

Fig. 7 Waveforms showing set-up times and hold times for P_n inputs.



Condition
 $\overline{SR} = \text{HIGH}$

Fig. 8 Waveforms showing set-up times and hold times for \overline{PE} input.

Note

Set-up and hold times are shown as positive values but may be specified as negative values.

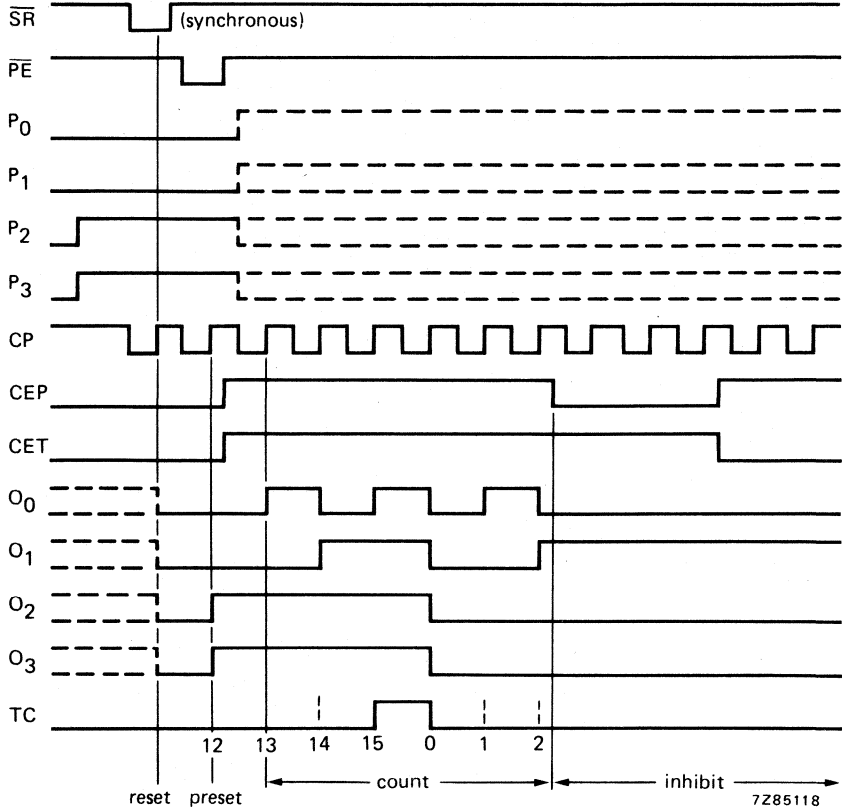
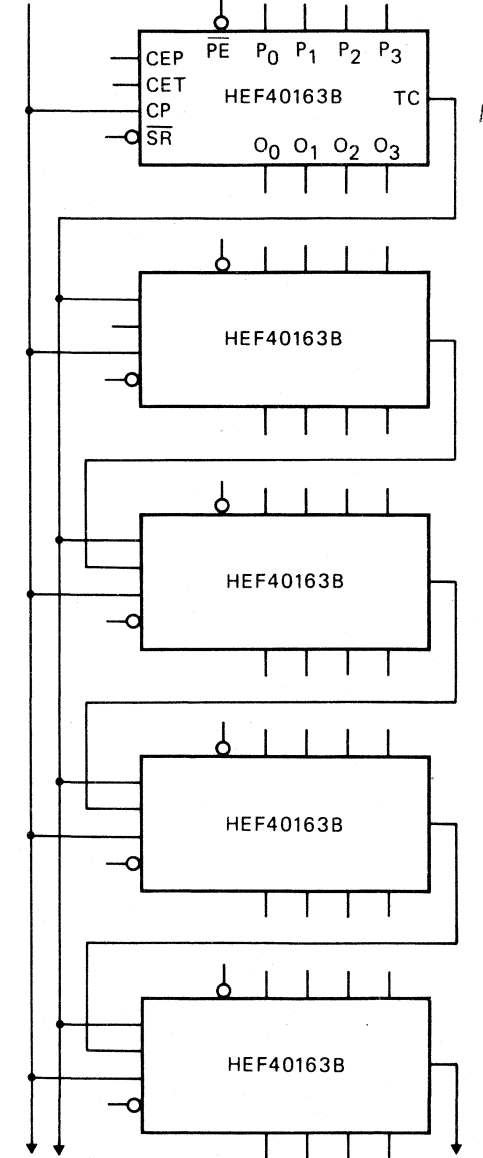


Fig. 9 Timing diagram.

APPLICATION INFORMATION

An example of an application for the HEF40163B is:

- Programmable binary counter.



NOTE

On the TC outputs, glitches can occur during counting. In totally synchronous mode they will not have any adverse affect. However the TC output in asynchronous mode can cause problems.

Fig. 10 Synchronous multi-stage counting scheme.

HEX D-TYPE FLIP-FLOP



The HEF40174B is a hex edge-triggered D-type flip-flop with six data inputs (D_0 to D_5), a clock input (CP), an overriding asynchronous master reset input (\overline{MR}), and six buffered outputs (O_0 to O_5). Information on D_0 to D_5 is transferred to O_0 to O_5 on the LOW to HIGH transition of CP if \overline{MR} is HIGH. When LOW, \overline{MR} resets all flip-flops (O_0 to $O_5 = \text{LOW}$) independent of CP and D_0 to D_5 .

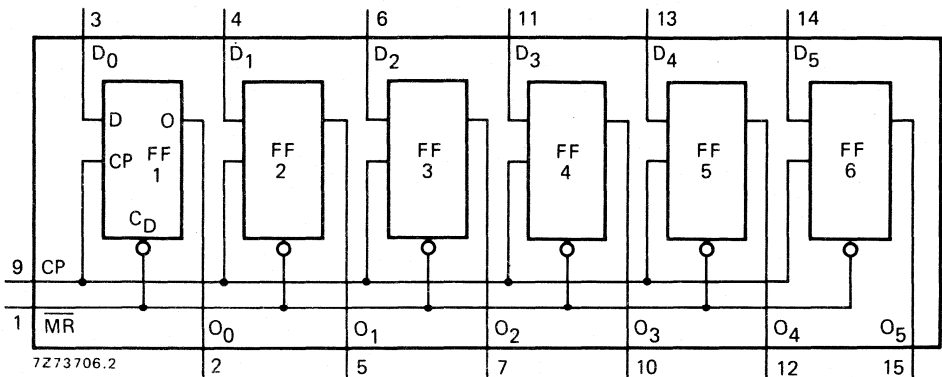


Fig. 1 Functional diagram.

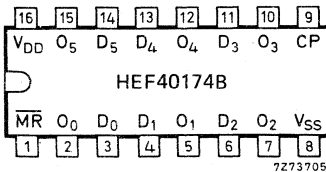


Fig. 2 Pinning diagram.

HEF40174BP: 16-lead DIL; plastic (SOT-38Z).
 HEF40174BD: 16-lead DIL; ceramic (SOT-74).
 HEF40174BT: 16-lead flat pack; plastic (SO-16; SOT-109A).

FAMILY DATA

see Family Specifications

I_{DD} LIMITS category MSI

PINNING

D_0 to D_5 data inputs
 CP clock input (LOW to HIGH; edge-triggered)
 \overline{MR} master reset input (active LOW)
 O_0 to O_5 buffered outputs

FUNCTION TABLE

inputs			output
CP	D	\overline{MR}	O
\nearrow	H	H	H
\nearrow	L	H	L
\searrow	X	H	no change
X	X	L	L

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

X = state is immaterial

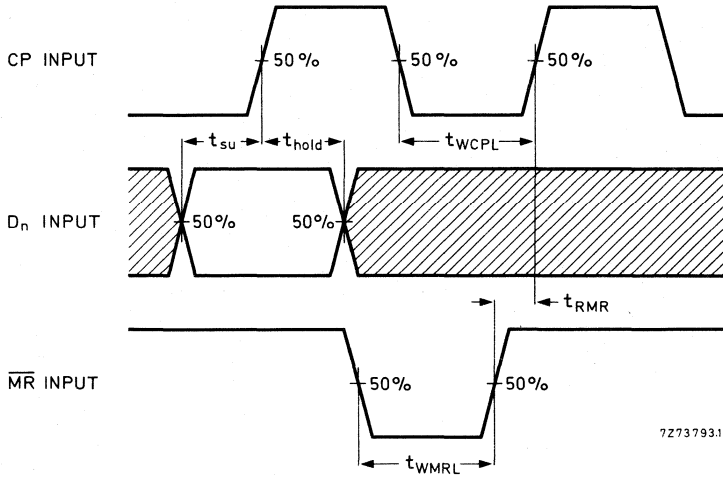
\nearrow = positive-going transition

\searrow = negative-going transition

A.C. CHARACTERISTICS

 $V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	symbol	min.	typ.	max.	typical extrapolation formula	
Propagation delays CP \rightarrow O_n HIGH to LOW	5	t _{PHL}		75	155 ns	48 ns + (0,55 ns/pF) C _L	
	10		30	65 ns	19 ns + (0,23 ns/pF) C _L		
	15		20	45 ns	12 ns + (0,16 ns/pF) C _L		
	LOW to HIGH	5	t _{PLH}		75	155 ns	48 ns + (0,55 ns/pF) C _L
		10		30	65 ns	19 ns + (0,23 ns/pF) C _L	
		15		20	45 ns	12 ns + (0,16 ns/pF) C _L	
	$\overline{MR} \rightarrow O_n$ HIGH to LOW	5	t _{PHL}		85	175 ns	58 ns + (0,55 ns/pF) C _L
		10		35	70 ns	24 ns + (0,23 ns/pF) C _L	
		15		25	50 ns	17 ns + (0,16 ns/pF) C _L	
Output transition times HIGH to LOW	5	t _{THL}		60	120 ns	10 ns + (1,0 ns/pF) C _L	
	10		30	60 ns	9 ns + (0,42 ns/pF) C _L		
	15		20	40 ns	6 ns + (0,28 ns/pF) C _L		
	LOW to HIGH	5	t _{TLH}		60	120 ns	10 ns + (1,0 ns/pF) C _L
		10		30	60 ns	9 ns + (0,42 ns/pF) C _L	
		15		20	40 ns	6 ns + (0,28 ns/pF) C _L	
Set-up time $D_n \rightarrow$ CP	5	t _{su}	20	10	ns	} see also waveforms Fig. 4	
	10		10	5	ns		
	15		10	5	ns		
Hold time $D_n \rightarrow$ CP	5	t _{hold}	10	0	ns		
	10		5	0	ns		
	15		5	0	ns		
Minimum clock pulse width; LOW	5	t _{WCPL}	70	35	ns		
	10		30	15	ns		
	15		20	10	ns		
Minimum \overline{MR} pulse width; LOW	5	t _{WMRL}	70	35	ns		
	10		35	15	ns		
	15		25	10	ns		
Recovery time for \overline{MR}	5	t _{RMR}	45	25	ns		
	10		20	10	ns		
	15		15	5	ns		
Maximum clock pulse frequency	5	f _{max}	5	11	MHz		
	10		15	30	MHz		
	15		20	45	MHz		
	V_{DD} V	typical formula for P (μ W)	where f _i = input freq. (MHz) f _o = output freq. (MHz) C _L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V _{DD} = supply voltage (V)				
Dynamic power dissipation per package (P)	5	3500 f _i + $\Sigma(f_o C_L) \times V_{DD}^2$					
	10	16 000 f _i + $\Sigma(f_o C_L) \times V_{DD}^2$					
	15	42 000 f _i + $\Sigma(f_o C_L) \times V_{DD}^2$					



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Fig. 4 Waveforms showing minimum pulse widths for CP and $\overline{\text{MR}}$, $\overline{\text{MR}}$ to CP recovery time, and set-up time and hold time for D_n to CP. Set-up and hold times are shown as positive values but may be specified as negative values.

APPLICATION INFORMATION

Some examples of applications for the HEF40174B are:

- Shift registers
- Buffer/storage register
- Pattern generator

QUADRUPLE D-TYPE FLIP-FLOP



The HEF40175B is a quadruple edge-triggered D-type flip-flop with four data inputs (D_0 to D_3), a clock input (CP), an overriding asynchronous master reset input (\overline{MR}), four buffered outputs (O_0 to O_3), and four complementary buffered outputs (\overline{O}_0 to \overline{O}_3). Information on D_0 to D_3 is transferred to O_0 to O_3 on the LOW to HIGH transition of CP if \overline{MR} is HIGH. When LOW, \overline{MR} resets all flip-flops (O_0 to $O_3 = \text{LOW}$, \overline{O}_0 to $\overline{O}_3 = \text{HIGH}$), independent of CP and D_0 to D_3 .

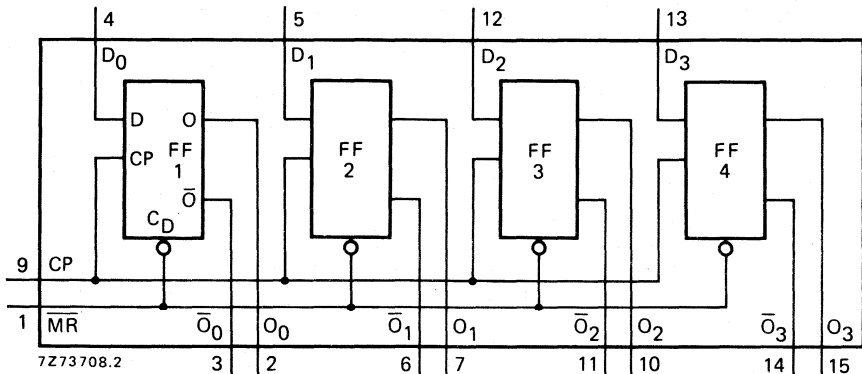


Fig. 1 Functional diagram.

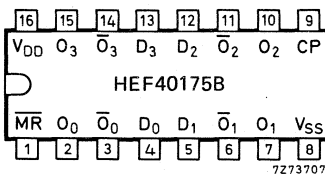


Fig. 2 Pinning diagram.

HEF40175BP: 16-lead DIL; plastic (SOT-38Z).

HEF40175BD: 16-lead DIL; ceramic (SOT-74).

HEF40175BT: 16-lead flat pack; plastic (SO-16; SOT-109A).

PINNING

- D_0 to D_3 data inputs
 CP clock input (LOW to HIGH; edge-triggered)
 \overline{MR} master reset input (active LOW)
 O_0 to O_3 buffered outputs
 \overline{O}_0 to \overline{O}_3 complementary buffered outputs

FUNCTION TABLE

inputs			outputs	
CP	D	\overline{MR}	O	\overline{O}
\nearrow	H	H	H	L
\nearrow	L	H	L	H
\searrow	X	H	no change	no change
X	X	L	L	H

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

X = state is immaterial

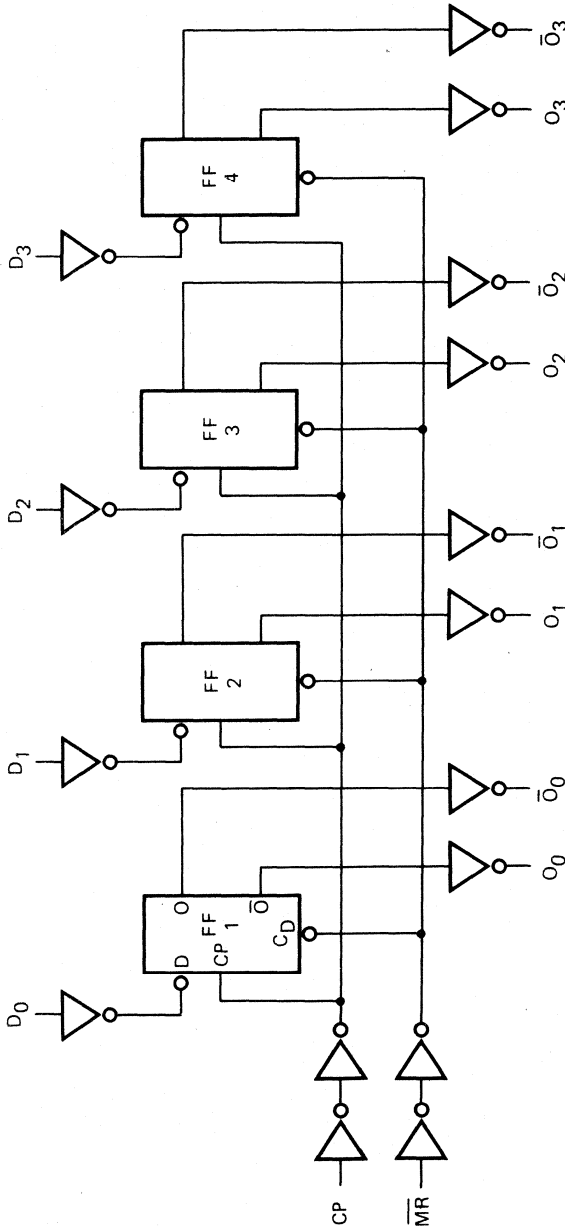
\nearrow = positive-going transition

\searrow = negative-going transition

FAMILY DATA

I_{DD} LIMITS category MSI

see Family Specifications



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Fig. 3 Logic diagram.

A.C. CHARACTERISTICS

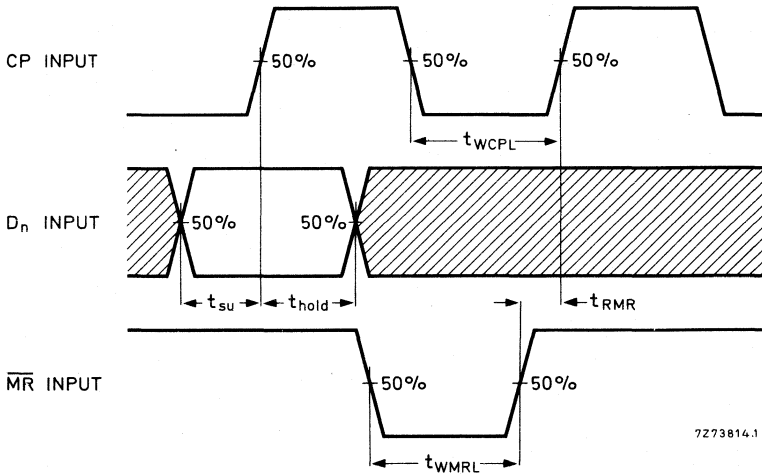
$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^\circ\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	symbol	min.	typ.	max.	typical extrapolation formula	
Propagation delays	CP \rightarrow O_n, \bar{O}_n HIGH to LOW	tPHL	5	80	160	ns	53 ns + (0,55 ns/pF) C_L
			10	35	70	ns	24 ns + (0,23 ns/pF) C_L
			15	25	50	ns	17 ns + (0,16 ns/pF) C_L
	LOW to HIGH	tPLH	5	70	140	ns	43 ns + (0,55 ns/pF) C_L
			10	30	65	ns	19 ns + (0,23 ns/pF) C_L
			15	25	45	ns	17 ns + (0,16 ns/pF) C_L
	$\overline{MR} \rightarrow O_n$ HIGH to LOW	tPHL	5	75	155	ns	48 ns + (0,55 ns/pF) C_L
			10	30	65	ns	19 ns + (0,23 ns/pF) C_L
			15	25	50	ns	17 ns + (0,16 ns/pF) C_L
	$\overline{MR} \rightarrow \bar{O}_n$ LOW to HIGH	tPLH	5	70	140	ns	43 ns + (0,55 ns/pF) C_L
			10	30	65	ns	19 ns + (0,23 ns/pF) C_L
			15	25	50	ns	17 ns + (0,16 ns/pF) C_L
Output transition times	HIGH to LOW	tTHL	5	60	120	ns	10 ns + (1,0 ns/pF) C_L
			10	30	60	ns	9 ns + (0,42 ns/pF) C_L
			15	20	40	ns	6 ns + (0,28 ns/pF) C_L
	LOW to HIGH	tTLH	5	60	120	ns	10 ns + (1,0 ns/pF) C_L
			10	30	60	ns	9 ns + (0,42 ns/pF) C_L
			15	20	40	ns	6 ns + (0,28 ns/pF) C_L
Set-up time $D_n \rightarrow CP$	t _{su}	5	60	30	ns	see also waveforms Fig. 4	
		10	20	10	ns		
		15	15	5	ns		
Hold time $D_n \rightarrow CP$	t _{hold}	5	25	-5	ns		
		10	10	0	ns		
		15	10	0	ns		
Minimum clock pulse width; LOW	tWCPL	5	90	45	ns		
		10	35	15	ns		
		15	25	10	ns		
Minimum \overline{MR} pulse width; LOW	tWMRL	5	80	40	ns		
		10	30	15	ns		
		15	20	10	ns		
Recovery time for \overline{MR}	t _{RMR}	5	0	-30	ns		
		10	0	-20	ns		
		15	0	-15	ns		
Maximum clock pulse frequency	f _{max}	5	5	11	MHz		
		10	15	30	MHz		
		15	20	45	MHz		

A.C. CHARACTERISTICS

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^\circ\text{C}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	typical formula for P (μW)	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
Dynamic power dissipation per package (P)	5	$2000 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	10	$8400 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$22500 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	



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Fig. 4 Waveforms showing minimum pulse widths for CP and MR, MR to CP recovery time, and set-up time and hold time for D_n to CP. Set-up and hold times are shown as positive values but may be specified as negative values.

APPLICATION INFORMATION

Some examples of applications for the HEF40175B are:

- Shift registers
- Buffer/storage register
- Pattern generator



4-BIT UP/DOWN DECADE COUNTER

The HEF40192B is a 4-bit synchronous up/down decade counter. The counter has a count-up clock input (CP_U), a count-down clock input (CP_D), an asynchronous parallel load input (\overline{PL}), four parallel data inputs (P_0 to P_3), an asynchronous master reset input (MR), four counter outputs (O_0 to O_3), an active LOW terminal count-up (carry) output (\overline{TC}_U) and an active LOW terminal count-down (borrow) output (\overline{TC}_D).

The counter outputs change state on the LOW to HIGH transition of either clock input. However, for correct counting, both clock inputs cannot be LOW simultaneously. The outputs \overline{TC}_U and \overline{TC}_D are normally HIGH. When the circuit has reached the maximum count state of '9', the next HIGH to LOW transition of CP_U will cause \overline{TC}_U to go LOW. \overline{TC}_U will stay LOW until CP_U goes HIGH again. Likewise, output \overline{TC}_D will go LOW when the circuit is in the zero state and CP_D goes LOW. When \overline{PL} is LOW, the information on P_0 to P_3 is asynchronously loaded into the counter. A HIGH on MR resets the counter independent of all other input conditions. The counter stages are of a static toggle type flip-flop.

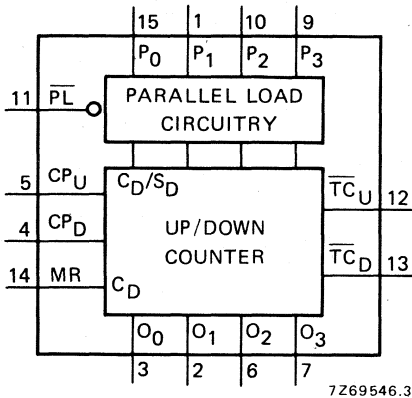


Fig. 1 Functional diagram.

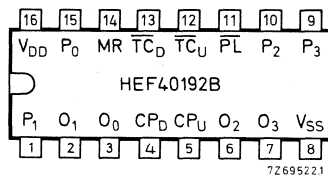


Fig. 2 Pinning diagram.

HEF40192BP: 16-lead DIL; plastic (SOT-38Z).

HEF40192BD: 16-lead DIL; ceramic (SOT-74).

HEF40192BT: 16-lead flat pack; plastic (SO-16; SOT-109A).

PINNING

- \overline{PL} parallel load input (active LOW)
 P_0 to P_3 parallel data inputs
 CP_U count-up clock pulse input (LOW to HIGH, edge-triggered)
 CP_D count-down clock pulse input (LOW to HIGH, edge-triggered)
 MR master reset input (asynchronous)
 \overline{TC}_U buffered terminal count-up (carry) output (active LOW)
 \overline{TC}_D buffered terminal count-down (borrow) output (active LOW)
 O_0 to O_3 buffered counter outputs

FAMILY DATA

} see Family Specifications

IDD LIMITS category MSI

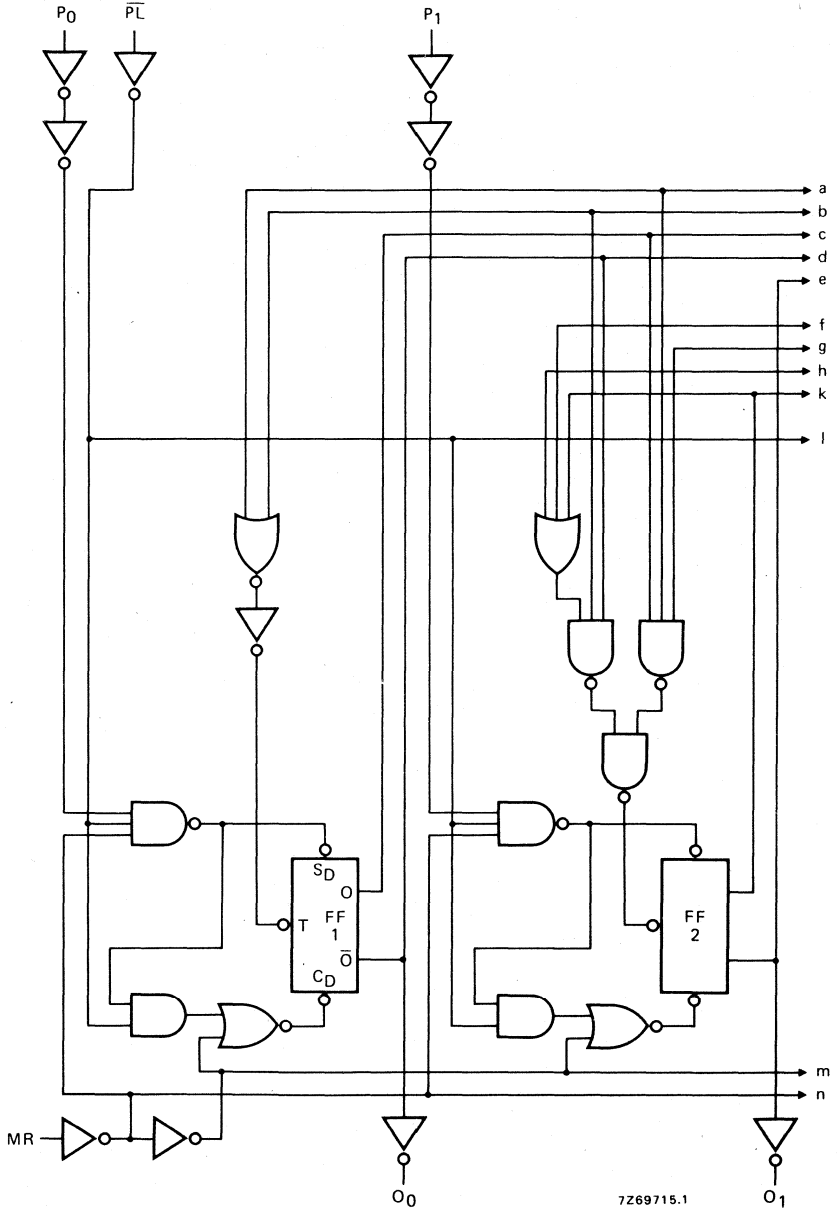


Fig. 3 Logic diagram (continued on next page).

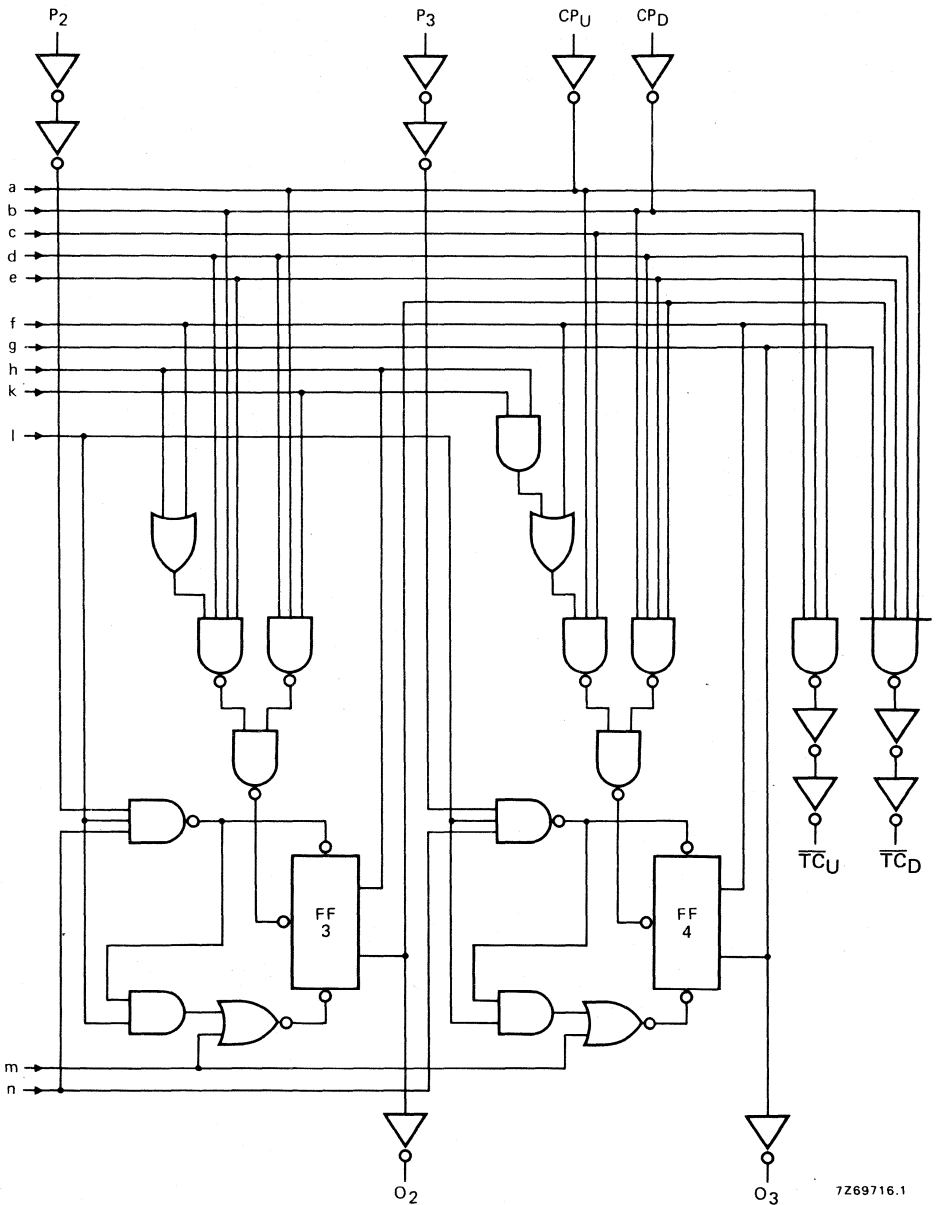
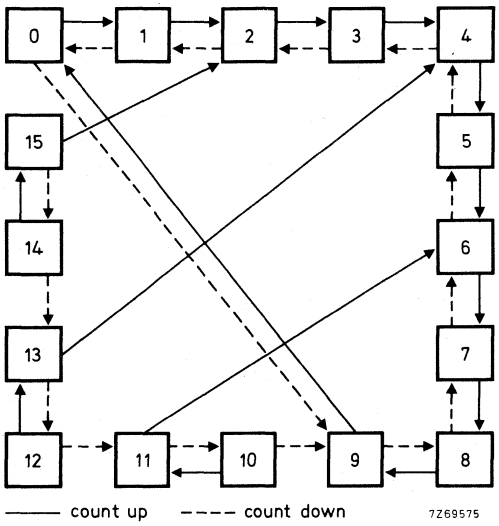


Fig. 3 Logic diagram (continued).

FUNCTION TABLE

MR	\overline{PL}	CP _U	CP _D	mode
H	X	X	X	reset (asyn.)
L	L	X	X	parallel load
L	H	/	H	count-up
L	H	H	/	count-down

H = HIGH state (the more positive voltage)
 L = LOW state (the less positive voltage)
 X = state is immaterial
 / = positive-going transition



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Fig. 4 State diagram.

Logic equations for terminal count:

$$\overline{TC}_U = \overline{O_0 \cdot O_3 \cdot CP_U}$$

$$\overline{TC}_D = \overline{O_0 \cdot \overline{O_1} \cdot \overline{O_2} \cdot \overline{O_3} \cdot CP_D}$$

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ≤ 20 ns

	V _{DD} V	typical formula for P (μW)	where f _i = input freq. (MHz) f _o = output freq. (MHz) C _L = load capacitance (pF) Σ(f _o C _L) = sum of outputs V _{DD} = supply voltage (V)
Dynamic power dissipation per package (P)	5	550 f _i + Σ(f _o C _L) × V _{DD} ²	
	10	2400 f _i + Σ(f _o C _L) × V _{DD} ²	
	15	6500 f _i + Σ(f _o C _L) × V _{DD} ²	

A.C. CHARACTERISTICS

 $V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

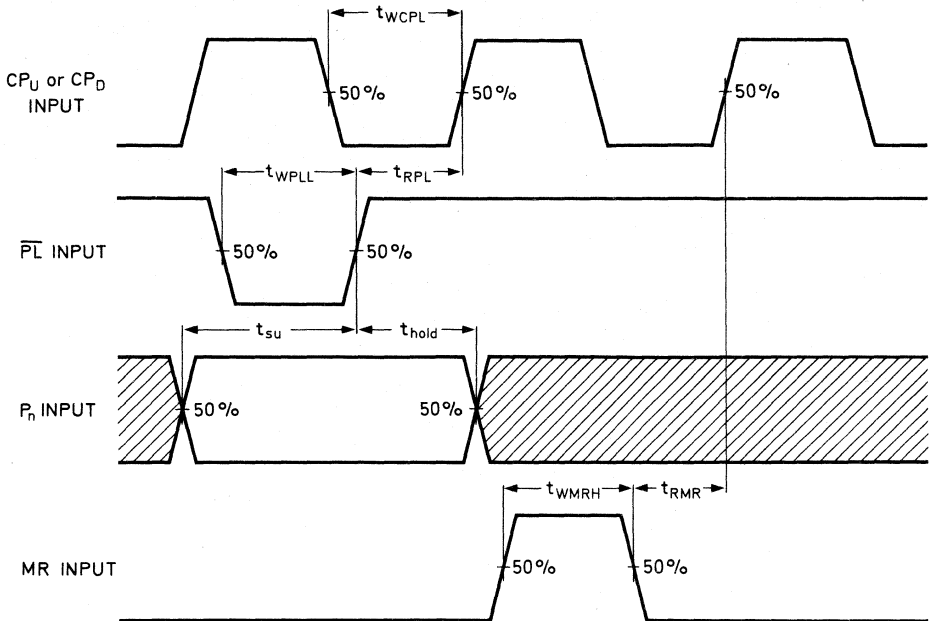
	V_{DD} V	symbol	min.	typ.	max.	typical extrapolation formula	
Propagation delays							
$CP_U \rightarrow O_n$	5			210	415	ns	$183\text{ ns} + (0,55\text{ ns/pF}) C_L$
HIGH to LOW	10	t_{PHL}		85	165	ns	$74\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			60	120	ns	$52\text{ ns} + (0,16\text{ ns/pF}) C_L$
	5			170	340	ns	$143\text{ ns} + (0,55\text{ ns/pF}) C_L$
LOW to HIGH	10	t_{PLH}		70	140	ns	$59\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			50	100	ns	$42\text{ ns} + (0,16\text{ ns/pF}) C_L$
$CP_D \rightarrow O_n$	5			210	420	ns	$183\text{ ns} + (0,55\text{ ns/pF}) C_L$
HIGH to LOW	10	t_{PHL}		85	170	ns	$74\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			65	125	ns	$57\text{ ns} + (0,16\text{ ns/pF}) C_L$
	5			170	340	ns	$143\text{ ns} + (0,55\text{ ns/pF}) C_L$
LOW to HIGH	10	t_{PLH}		70	140	ns	$59\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			50	100	ns	$42\text{ ns} + (0,16\text{ ns/pF}) C_L$
$CP_U \rightarrow \overline{TC}_U$	5			125	250	ns	$98\text{ ns} + (0,55\text{ ns/pF}) C_L$
HIGH to LOW	10	t_{PHL}		50	100	ns	$39\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			35	70	ns	$27\text{ ns} + (0,16\text{ ns/pF}) C_L$
	5			95	185	ns	$68\text{ ns} + (0,55\text{ ns/pF}) C_L$
LOW to HIGH	10	t_{PLH}		40	80	ns	$29\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			30	60	ns	$22\text{ ns} + (0,16\text{ ns/pF}) C_L$
$CP_D \rightarrow \overline{TC}_D$	5			140	280	ns	$113\text{ ns} + (0,55\text{ ns/pF}) C_L$
HIGH to LOW	10	t_{PHL}		55	110	ns	$44\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			40	80	ns	$32\text{ ns} + (0,16\text{ ns/pF}) C_L$
	5			100	195	ns	$73\text{ ns} + (0,55\text{ ns/pF}) C_L$
LOW to HIGH	10	t_{PLH}		40	85	ns	$29\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			30	65	ns	$22\text{ ns} + (0,16\text{ ns/pF}) C_L$
$MR \rightarrow O_n$	5			195	390	ns	$168\text{ ns} + (0,55\text{ ns/pF}) C_L$
HIGH to LOW	10	t_{PHL}		80	160	ns	$69\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			60	120	ns	$52\text{ ns} + (0,16\text{ ns/pF}) C_L$
$MR \rightarrow \overline{TC}_U$	5			145	285	ns	$118\text{ ns} + (0,55\text{ ns/pF}) C_L$
LOW to HIGH	10	t_{PLH}		60	115	ns	$49\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			45	90	ns	$37\text{ ns} + (0,16\text{ ns/pF}) C_L$
$MR \rightarrow \overline{TC}_D$	5			365	730	ns	$338\text{ ns} + (0,55\text{ ns/pF}) C_L$
HIGH to LOW	10	t_{PHL}		130	265	ns	$119\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			100	205	ns	$92\text{ ns} + (0,16\text{ ns/pF}) C_L$
$\overline{PL} \rightarrow O_n$	5			185	360	ns	$158\text{ ns} + (0,55\text{ ns/pF}) C_L$
HIGH to LOW	10	t_{PHL}		75	150	ns	$64\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			55	110	ns	$47\text{ ns} + (0,16\text{ ns/pF}) C_L$
	5			145	290	ns	$118\text{ ns} + (0,55\text{ ns/pF}) C_L$
LOW to HIGH	10	t_{PLH}		60	120	ns	$49\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			45	90	ns	$37\text{ ns} + (0,16\text{ ns/pF}) C_L$

A.C. CHARACTERISTICS

 $V_{SS} = 0 \text{ V}$; $T_{amb} = 25 \text{ }^\circ\text{C}$; $C_L = 50 \text{ pF}$; input transition times $\leq 20 \text{ ns}$

	V_{DD} V	symbol	min.	typ.	max.	typical extrapolation formula		
Output transition times HIGH to LOW	5			60	120	ns	$10 \text{ ns} + (1,0 \text{ ns/pF}) C_L$	
	10	t_{THL}		30	60	ns	$9 \text{ ns} + (0,42 \text{ ns/pF}) C_L$	
	15			20	40	ns	$6 \text{ ns} + (0,28 \text{ ns/pF}) C_L$	
LOW to HIGH	5			60	120	ns	$10 \text{ ns} + (1,0 \text{ ns/pF}) C_L$	
	10	t_{TLH}		30	60	ns	$9 \text{ ns} + (0,42 \text{ ns/pF}) C_L$	
	15			20	40	ns	$6 \text{ ns} + (0,28 \text{ ns/pF}) C_L$	
Set-up time $P_n \rightarrow \overline{P_L}$	5		160	80		ns		
	10	t_{su}		60	30		ns	
	15			50	25		ns	
Hold time $P_n \rightarrow \overline{P_L}$	5			10	-70		ns	
	10	t_{hold}		5	-25		ns	
	15			5	-20		ns	
Minimum CP_U or CP_D pulse width; LOW	5		150	75			ns	
	10	t_{WCPL}		50	25		ns	
	15			35	20		ns	
Minimum MR pulse width; HIGH	5		180	90			ns	
	10	t_{WMRH}		70	35		ns	
	15			60	30		ns	
Minimum $\overline{P_L}$ pulse width; LOW	5		120	60			ns	
	10	t_{WPLL}		45	20		ns	
	15			30	15		ns	
Recovery time for MR	5		125	65			ns	
	10	t_{RMR}		70	35		ns	
	15			50	25		ns	
Recovery time for $\overline{P_L}$	5		90	45			ns	
	10	t_{RPL}		35	15		ns	
	15			25	10		ns	
Maximum clock pulse frequency	5		3	6			MHz	
	10	f_{max}		9	18		MHz	
	15			13	26		MHz	

see also waveforms
Fig. 5



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Fig. 5 Waveforms showing recovery times for \overline{PL} and MR, minimum pulse widths for CP_U , CP_D , \overline{PL} and MR, and set-up and hold times for P to \overline{PL} . Set-up times and hold times are shown as positive values but may be specified as negative values.



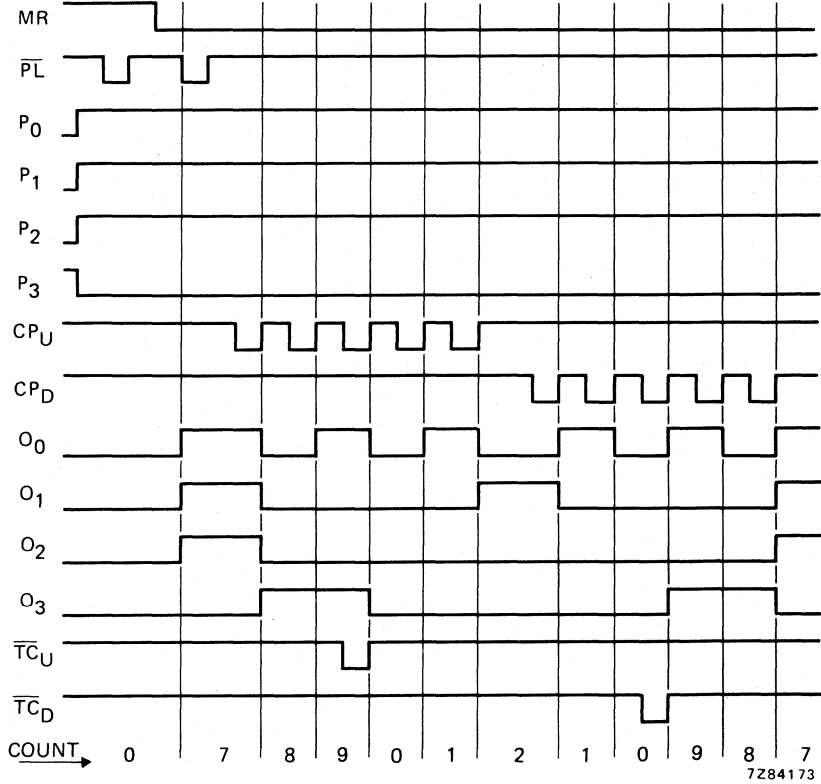


Fig. 6 Timing diagram.

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APPLICATION INFORMATION

Some examples of applications for the HEF40192B are:

- Up/down difference counting
- Multistage ripple counting
- Multistage synchronous counting.

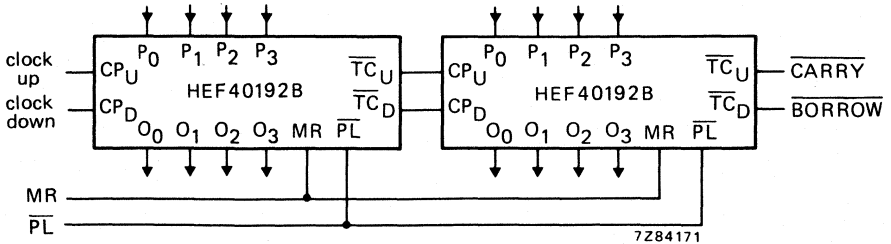


Fig. 7 Example of cascaded HEF40192B ICs.

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4-BIT UP/DOWN BINARY COUNTER

The HEF40193B is a 4-bit synchronous up/down binary counter. The counter has a count-up clock input (CP_U), a count-down clock input (CP_D), an asynchronous parallel load input (\overline{PL}), four parallel data inputs (P_0 to P_3), an asynchronous master reset input (MR), four counter outputs (O_0 to O_3), an active LOW terminal count-up (carry) output (\overline{TC}_U) and an active LOW terminal count-down (borrow) output (\overline{TC}_D).

The counter outputs change state on the LOW to HIGH transition of either clock input. However, for correct counting, both clock inputs cannot be LOW simultaneously. The outputs \overline{TC}_U and \overline{TC}_D are normally HIGH. When the circuit has reached the maximum count state of '15', the next HIGH to LOW transition of CP_U will cause \overline{TC}_U to go LOW. \overline{TC}_U will stay LOW until CP_U goes HIGH again. Likewise, output \overline{TC}_D will go LOW when the circuit is in the zero state and CP_D goes LOW. When \overline{PL} is LOW, the information on P_0 to P_3 is asynchronously loaded into the counter. A HIGH on MR resets the counter independent of all other input conditions. The counter stages are of a static toggle type flip-flop.

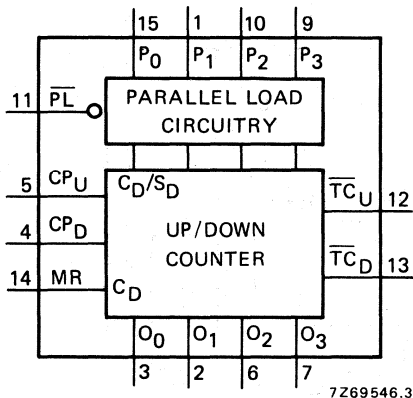


Fig. 1 Functional diagram.

PINNING

\overline{PL}	parallel load input (active LOW)
P_0 to P_3	parallel data inputs
CP_U	count-up clock pulse input (LOW to HIGH, edge-triggered)
CP_D	count-down clock pulse input (LOW to HIGH, edge-triggered)
MR	master reset input (asynchronous)
\overline{TC}_U	buffered terminal count-up (carry) output (active LOW)
\overline{TC}_D	buffered terminal count-down (borrow) output (active LOW)
O_0 to O_3	buffered counter outputs

FAMILY DATA

IDD LIMITS category MSI

} see Family Specifications

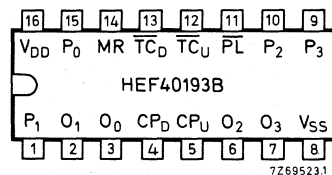


Fig. 2 Pinning diagram.

HEF40193BP: 16-lead DIL; plastic (SOT-38Z).
 HEF40193BD: 16-lead DIL; ceramic (SOT-74).
 HEF40193BT: 16-lead flat pack; plastic (SO-16; SOT-109A).

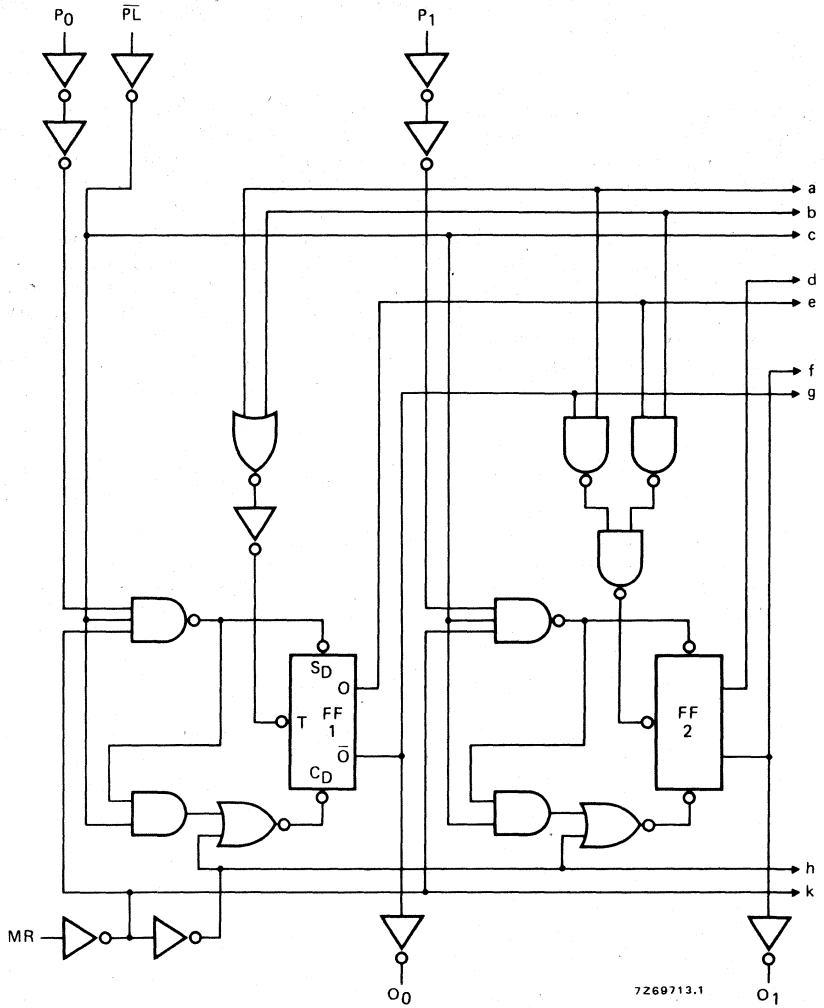
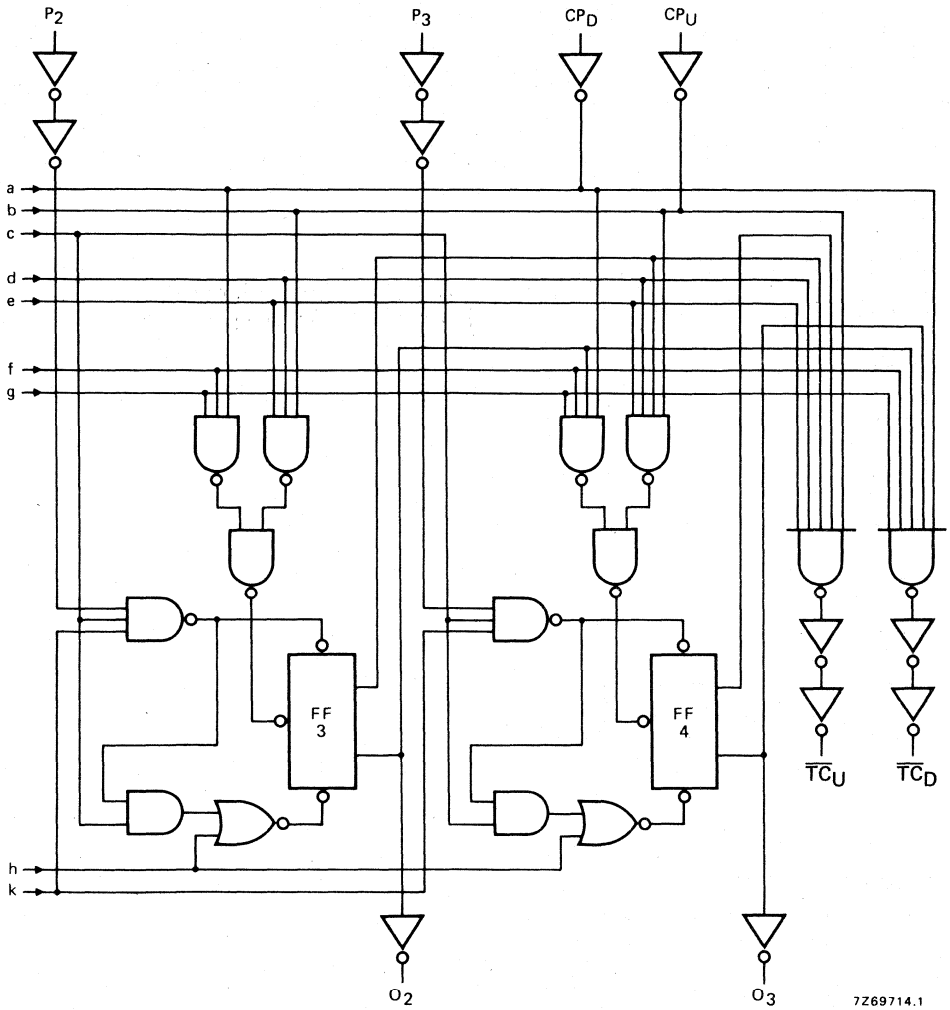


Fig. 3 Logic diagram (continued on next page).



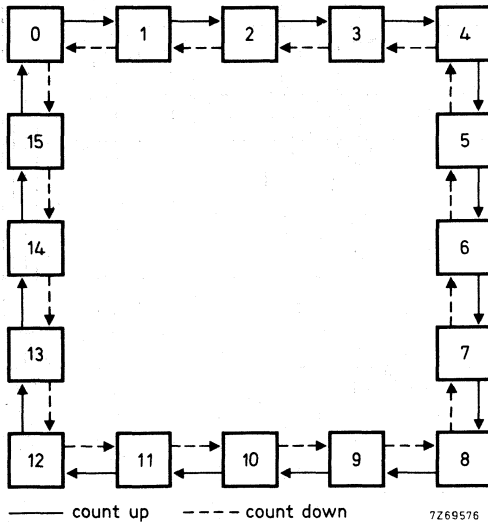
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Fig. 3 Logic diagram (continued).

FUNCTION TABLE

MR	\overline{PL}	CP _U	CP _D	mode
H	X	X	X	reset (asyn.)
L	L	X	X	parallel load
L	H	\nearrow	H	count-up
L	H	H	\searrow	count-down

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
 \nearrow = positive-going transition



Logic equations for terminal count:

$$\overline{TC}_U = \overline{O_0 \cdot O_1 \cdot O_2 \cdot O_3 \cdot CP_U}$$

$$\overline{TC}_D = \overline{\overline{O_0} \cdot \overline{O_1} \cdot \overline{O_2} \cdot \overline{O_3} \cdot \overline{CP_D}}$$

Fig. 4 State diagram.

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ≤ 20 ns

	V _{DD} V	typical formula for P (μW)	where f _i = input freq. (MHz) f _o = output freq. (MHz) C _L = load capacitance (pF) Σ(f _o C _L) = sum of outputs V _{DD} = supply voltage (V)
Dynamic power dissipation per package (P)	5	600 f _i + Σ(f _o C _L) × V _{DD} ²	
	10	2700 f _i + Σ(f _o C _L) × V _{DD} ²	
	15	7500 f _i + Σ(f _o C _L) × V _{DD} ²	

A.C. CHARACTERISTICS

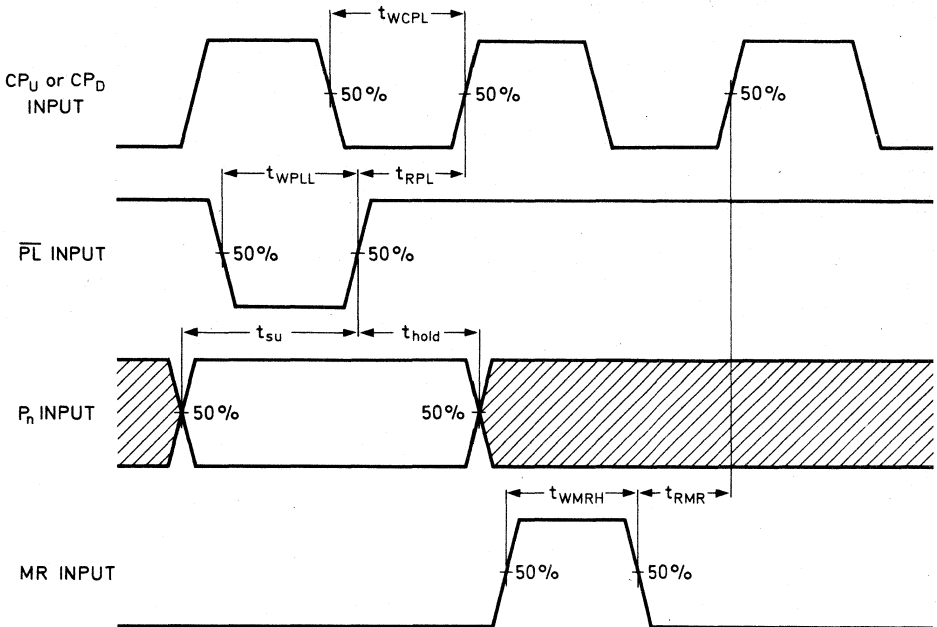
 $V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	symbol	min.	typ.	max.	typical extrapolation formula
Propagation delays						
$CP_U \rightarrow O_n$	5			210	415 ns	$183\text{ ns} + (0,55\text{ ns/pF}) C_L$
HIGH to LOW	10	t_{PHL}		85	165 ns	$74\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			60	120 ns	$52\text{ ns} + (0,16\text{ ns/pF}) C_L$
	5			170	340 ns	$143\text{ ns} + (0,55\text{ ns/pF}) C_L$
LOW to HIGH	10	t_{PLH}		70	140 ns	$59\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			50	100 ns	$42\text{ ns} + (0,16\text{ ns/pF}) C_L$
$CP_D \rightarrow O_n$	5			210	425 ns	$183\text{ ns} + (0,55\text{ ns/pF}) C_L$
HIGH to LOW	10	t_{PHL}		85	170 ns	$74\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			60	125 ns	$57\text{ ns} + (0,16\text{ ns/pF}) C_L$
	5			170	340 ns	$143\text{ ns} + (0,55\text{ ns/pF}) C_L$
LOW to HIGH	10	t_{PLH}		70	140 ns	$59\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			50	100 ns	$42\text{ ns} + (0,16\text{ ns/pF}) C_L$
$CP_U \rightarrow \overline{TC}_U$	5			125	250 ns	$98\text{ ns} + (0,55\text{ ns/pF}) C_L$
HIGH to LOW	10	t_{PHL}		50	100 ns	$39\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			35	70 ns	$27\text{ ns} + (0,16\text{ ns/pF}) C_L$
	5			95	185 ns	$68\text{ ns} + (0,55\text{ ns/pF}) C_L$
LOW to HIGH	10	t_{PLH}		40	80 ns	$29\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			30	60 ns	$22\text{ ns} + (0,16\text{ ns/pF}) C_L$
$CP_D \rightarrow \overline{TC}_D$	5			140	280 ns	$113\text{ ns} + (0,55\text{ ns/pF}) C_L$
HIGH to LOW	10	t_{PHL}		55	110 ns	$44\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			40	80 ns	$32\text{ ns} + (0,16\text{ ns/pF}) C_L$
	5			100	195 ns	$73\text{ ns} + (0,55\text{ ns/pF}) C_L$
LOW to HIGH	10	t_{PLH}		40	85 ns	$29\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			30	65 ns	$22\text{ ns} + (0,16\text{ ns/pF}) C_L$
$MR \rightarrow O_n$	5			195	390 ns	$168\text{ ns} + (0,55\text{ ns/pF}) C_L$
HIGH to LOW	10	t_{PHL}		80	160 ns	$69\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			60	120 ns	$52\text{ ns} + (0,16\text{ ns/pF}) C_L$
$MR \rightarrow \overline{TC}_U$	5			145	285 ns	$118\text{ ns} + (0,55\text{ ns/pF}) C_L$
LOW to HIGH	10	t_{PLH}		60	115 ns	$49\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			45	90 ns	$37\text{ ns} + (0,16\text{ ns/pF}) C_L$
$MR \rightarrow \overline{TC}_D$	5			365	730 ns	$338\text{ ns} + (0,55\text{ ns/pF}) C_L$
HIGH to LOW	10	t_{PHL}		130	265 ns	$119\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			100	205 ns	$92\text{ ns} + (0,16\text{ ns/pF}) C_L$
$\overline{PL} \rightarrow O_n$	5			185	360 ns	$158\text{ ns} + (0,55\text{ ns/pF}) C_L$
HIGH to LOW	10	t_{PHL}		75	150 ns	$64\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			55	110 ns	$47\text{ ns} + (0,16\text{ ns/pF}) C_L$
	5			145	290 ns	$118\text{ ns} + (0,55\text{ ns/pF}) C_L$
LOW to HIGH	10	t_{PLH}		60	120 ns	$49\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			45	90 ns	$37\text{ ns} + (0,16\text{ ns/pF}) C_L$

A.C. CHARACTERISTICS

 $V_{SS} = 0 \text{ V}$; $T_{amb} = 25 \text{ }^\circ\text{C}$; $C_L = 50 \text{ pF}$; input transition times $\leq 20 \text{ ns}$

	V_{DD} V	symbol	min.	typ.	max.	typical extrapolation formula	
Output transition times HIGH to LOW	5	t_{THL}		60	120	ns	$10 \text{ ns} + (1,0 \text{ ns/pF}) C_L$ $9 \text{ ns} + (0,42 \text{ ns/pF}) C_L$ $6 \text{ ns} + (0,28 \text{ ns/pF}) C_L$
	10			30	60	ns	
	15			20	40	ns	
LOW to HIGH	5	t_{TLH}		60	120	ns	$10 \text{ ns} + (1,0 \text{ ns/pF}) C_L$ $9 \text{ ns} + (0,42 \text{ ns/pF}) C_L$ $6 \text{ ns} + (0,28 \text{ ns/pF}) C_L$
	10			30	60	ns	
	15			20	40	ns	
Set-up time $P_n \rightarrow \overline{PL}$	5	t_{su}	160	80		ns	
	10		60	30		ns	
	15		50	25		ns	
Hold time $P_n \rightarrow \overline{PL}$	5	t_{hold}	10	-70		ns	
	10		5	-25		ns	
	15		5	-20		ns	
Minimum CP_U or CP_D pulse width; LOW	5	t_{WCPL}	150	75		ns	
	10		50	25		ns	
	15		35	20		ns	
Minimum MR pulse width; HIGH	5	t_{WMRH}	180	90		ns	see also waveforms Fig. 5
	10		70	35		ns	
	15		60	30		ns	
Minimum \overline{PL} pulse width; LOW	5	t_{WPLL}	120	60		ns	
	10		45	20		ns	
	15		30	15		ns	
Recovery time for MR	5	t_{RMR}	125	65		ns	
	10		70	35		ns	
	15		50	25		ns	
Recovery time for \overline{PL}	5	t_{RPL}	90	45		ns	
	10		35	15		ns	
	15		25	10		ns	
Maximum clock pulse frequency	5	f_{max}	3	5		MHz	
	10		9	18		MHz	
	15		13	26		MHz	



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Fig. 5 Waveforms showing recovery times for \overline{PL} and MR, minimum pulse widths for CP_U, CP_D, \overline{PL} and MR, and set-up and hold times for P to \overline{PL} . Set-up times and hold times are shown as positive values but may be specified as negative values.

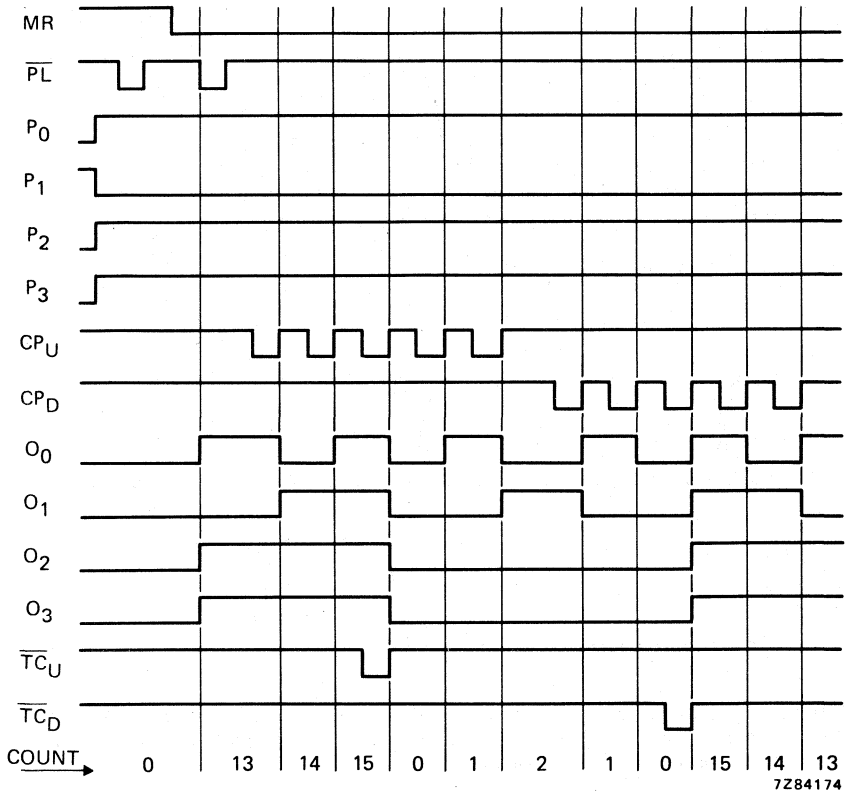


Fig. 6 Timing diagram.

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APPLICATION INFORMATION

Some examples of applications for the HEF40193B are:

- Up/down difference counting
- Multistage ripple counting
- Multistage synchronous counting

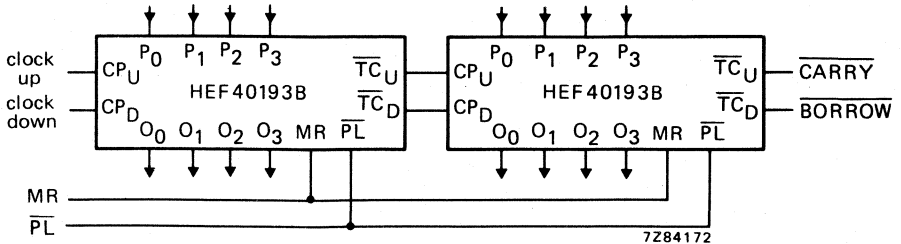


Fig. 7 Example of cascaded HEF40193B ICs.

7Z84172

4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER



The HEF40194B is a 4-bit bidirectional shift register with two mode control inputs (S_0 and S_1), a clock input (CP), a serial data shift left input (D_{SL}), a serial data shift right input (D_{SR}), four parallel data inputs (P_0 to P_3), an overriding asynchronous master reset input (\overline{MR}), and four buffered parallel outputs (O_0 to O_3). When LOW, \overline{MR} resets all stages and forces O_0 to O_3 LOW, overriding all other input conditions. When \overline{MR} is HIGH, the operation mode is controlled by S_0 and S_1 as shown in the function table.

Serial and parallel operation are edge-triggered on the LOW to HIGH transition of CP. The inputs at which the data are to be entered and S_0 , S_1 must be stable for a set-up time before the LOW to HIGH transition of CP.

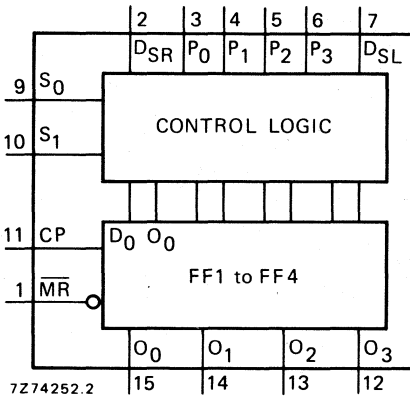


Fig. 1 Functional diagram.

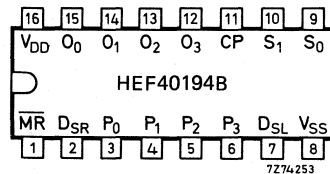


Fig. 2 Pinning diagram.

HEF40194BP: 16-lead DIL; plastic (SOT-38Z).
 HEF40194BD: 16-lead DIL; ceramic (SOT-74).
 HEF40194BT: 16-lead flat pack; plastic (SO-16; SOT-109A).

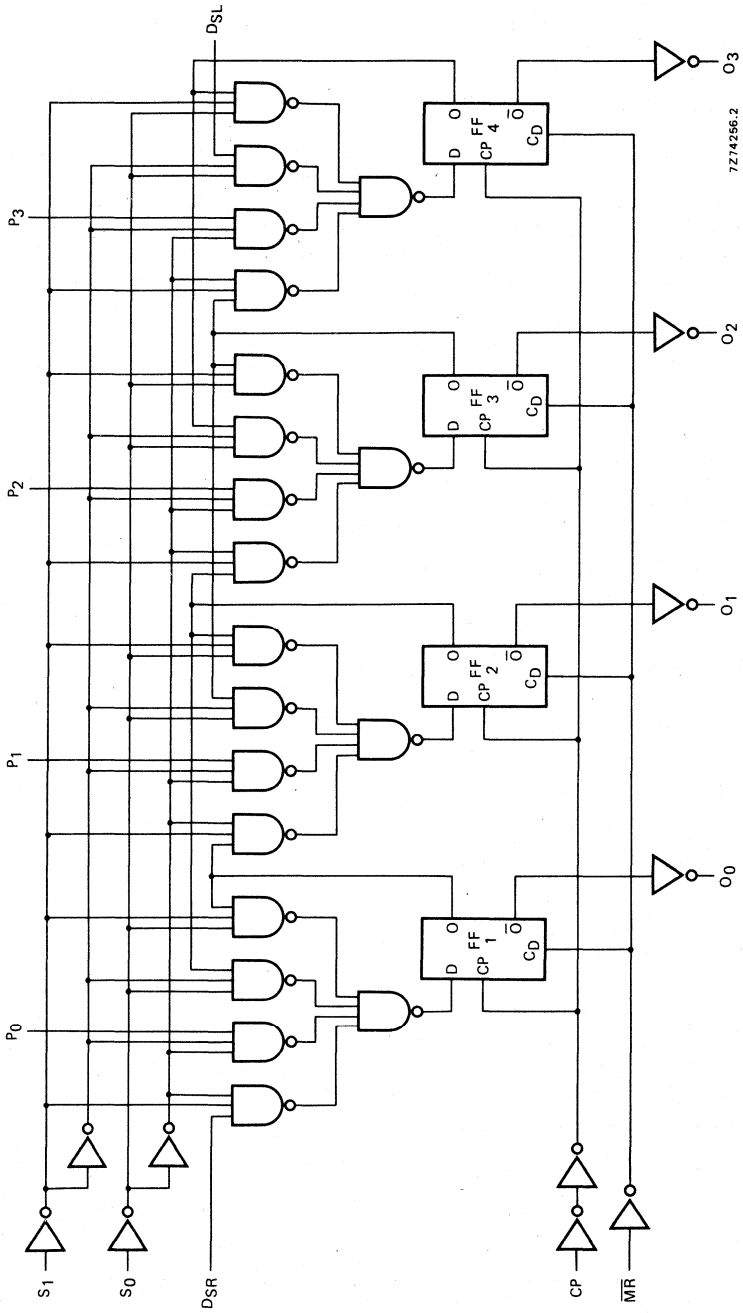
PINNING

S_0 , S_1	mode control inputs
P_0 to P_3	parallel data inputs
D_{SR}	serial data shift right input
D_{SL}	serial data shift left input
CP	clock input (LOW to HIGH edge-triggered)
\overline{MR}	master reset input (active LOW)
O_0 to O_3	buffered parallel outputs

FAMILY DATA

I_{DD} LIMITS category MSI

see Family Specifications



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Fig. 3 Logic diagram.

FUNCTION TABLE

operating mode	inputs ($\overline{MR} = \text{HIGH}$)					outputs at $t_n + 1$			
	S ₁	S ₀	D _{SR}	D _{SL}	P ₀ to P ₃	O ₀	O ₁	O ₂	O ₃
hold	L	L	X	X	X	O ₀	O ₁	O ₂	O ₃
shift left	H	L	X	L	X	O ₁	O ₂	O ₃	L
	H	L	X	H	X	O ₁	O ₂	O ₃	H
shift right	L	H	L	X	X	L	O ₀	O ₁	O ₂
	L	H	H	X	X	H	O ₀	O ₁	O ₂
parallel load	H	H	X	X	L	L	L	L	L
	H	H	X	X	H	H	H	H	H

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

X = state is immaterial

$t_n + 1$ = state after next LOW to HIGH transition of CP

A.C. CHARACTERISTICS

$V_{SS} = 0 \text{ V}$; $T_{amb} = 25 \text{ }^\circ\text{C}$; input transition times $\leq 20 \text{ ns}$

	V_{DD} V	typical formula for P (μW)	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load cap. (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
Dynamic power dissipation per package (P)	5	$1\,500 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	10	$6\,900 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$18\,900 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

A.C. CHARACTERISTICS

 $V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	symbol	min.	typ.	max.	typical extrapolation formula
Propagation delays CP \rightarrow O_n HIGH to LOW	5	tPHL	100	205	ns	$73\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10		40	85	ns	$29\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15		30	60	ns	$22\text{ ns} + (0,16\text{ ns/pF}) C_L$
LOW to HIGH	5	tPLH	80	165	ns	$53\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10		35	70	ns	$24\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15		25	55	ns	$17\text{ ns} + (0,16\text{ ns/pF}) C_L$
$\overline{\text{MR}} \rightarrow O_n$ HIGH to LOW	5	tPHL	85	175	ns	$58\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10		40	80	ns	$29\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15		30	60	ns	$22\text{ ns} + (0,16\text{ ns/pF}) C_L$
Output transition times HIGH to LOW	5	tTHL	60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$
	10		30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$
	15		20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$
LOW to HIGH	5	tTLH	60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$
	10		30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$
	15		20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$
Set-up times $P_n, D_{SR}, D_{SL} \rightarrow CP$	5	t _{su}	80	40	ns	} see also waveforms Figs 4 and 5
	10		30	15	ns	
	15		20	10	ns	
$S_n \rightarrow CP$	5	t _{su}	140	70	ns	
	10		60	30	ns	
	15		40	20	ns	
Hold times $P_n, D_{SR}, D_{SL} \rightarrow CP$	5	t _{hold}	10	-30	ns	
	10		5	-10	ns	
	15		5	-5	ns	
$S_n \rightarrow CP$	5	t _{hold}	25	-45	ns	
	10		15	-15	ns	
	15		10	-10	ns	
Minimum clock pulse width; LOW	5	tWCPL	50	25	ns	
	10		20	10	ns	
	15		20	10	ns	
Minimum $\overline{\text{MR}}$ pulse width; LOW	5	tWMRL	80	40	ns	
	10		40	20	ns	
	15		30	15	ns	
Recovery time for MR	5	tRMR	30	10	ns	
	10		15	5	ns	
	15		15	5	ns	
Maximum clock pulse frequency	5	f _{max}	6	12	MHz	
	10		15	30	MHz	
	15		20	40	MHz	

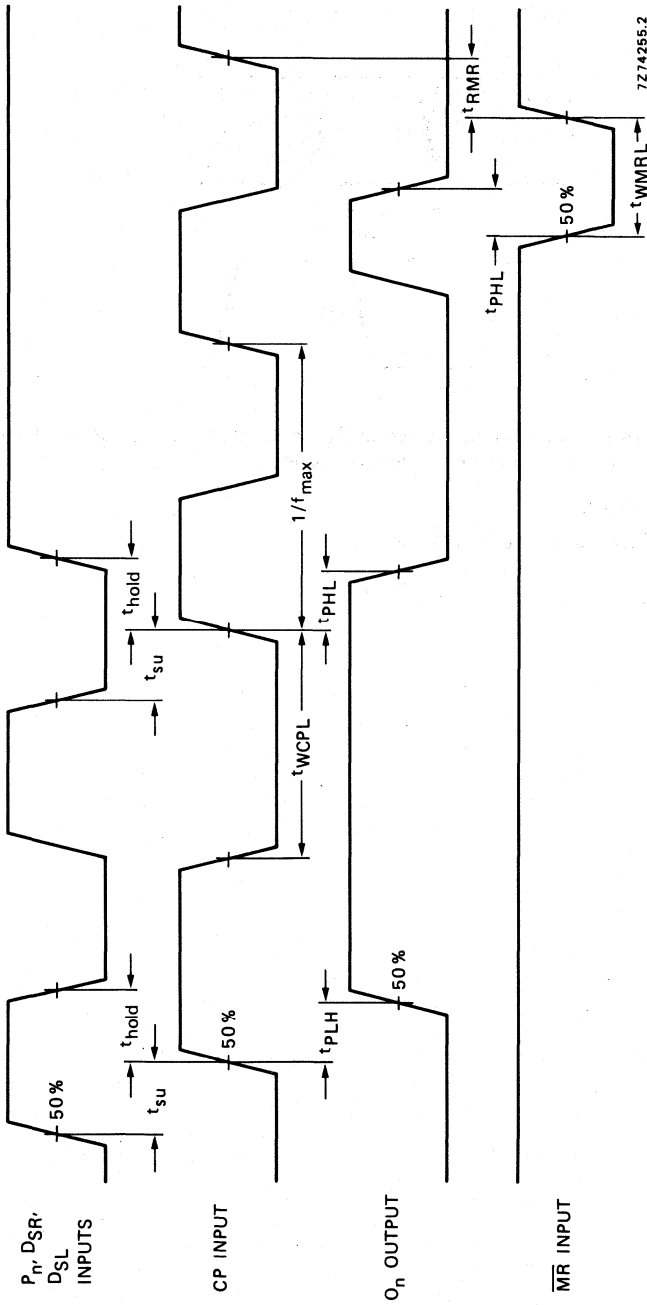


Fig. 4 Waveforms showing set-up times, hold times for DSR , DSL and P_n inputs; minimum \overline{MR} pulse width, \overline{MR} to output delays and \overline{MR} to CP recovery time; minimum CP pulse width and CP to output delays. Set-up and hold times are shown as positive values but may be specified as negative values.



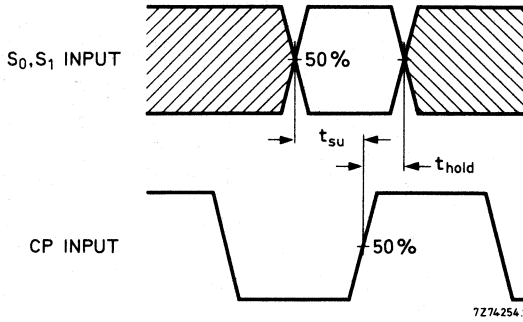


Fig. 5 Waveforms showing set-up times and hold times for S_0 and S_1 inputs. Set-up and hold times are shown as positive values but may be specified as negative values.

APPLICATION INFORMATION

Some examples of applications for the HEF40194B are:

- Arithmetic unit register
- Serial/parallel converter.



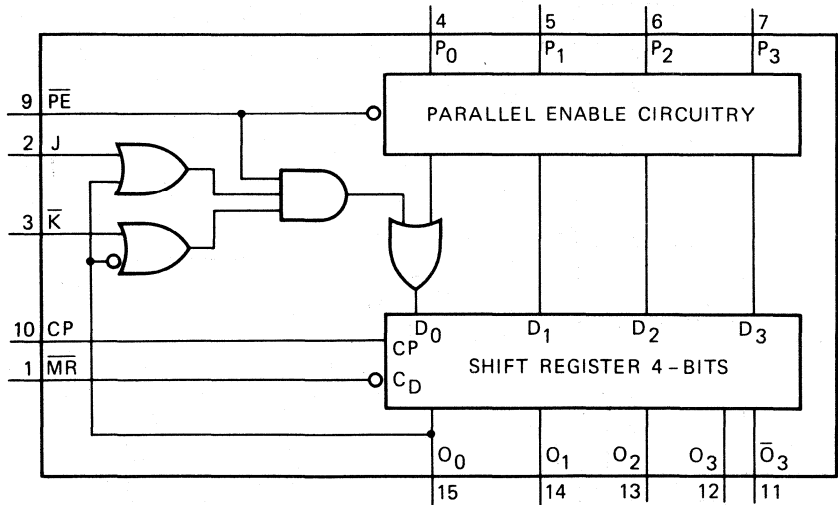
4-BIT UNIVERSAL SHIFT REGISTER

The HEF40195B is a fully synchronous edge-triggered 4-bit shift register with a clock input (CP), four synchronous parallel data inputs (P_0 to P_3), two synchronous serial data inputs (J, \bar{K}), a synchronous parallel enable input (\overline{PE}), buffered parallel outputs from all 4-bit positions (O_0 to O_3), a buffered inverted output from the last bit position (\bar{O}_3) and an overriding asynchronous master reset input (\overline{MR}). Each register stage is of a D-type master-slave flip-flop.

Operation is synchronous (except for \overline{MR}) and is edge-triggered on the LOW to HIGH transition of the CP input. When \overline{PE} is LOW, data are loaded into the register from P_0 to P_3 on the LOW to HIGH transition of CP. When \overline{PE} is HIGH, data are shifted into the first register position from J and \bar{K} and all the data in the register are shifted one position to the right on the LOW to HIGH transition of CP. D-type entry is obtained by interconnecting J and \bar{K} .

When J is HIGH and \bar{K} is LOW, the first stage is in the toggle mode. When J is LOW and \bar{K} is HIGH, the first stage is in the hold mode.

A LOW on \overline{MR} resets all four bit positions (O_0 to $O_3 = \text{LOW}$, $\bar{O}_3 = \text{HIGH}$) independent of all other input conditions.



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Fig. 1 Functional diagram.

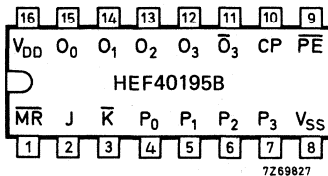


Fig. 2 Pinning diagram.

HEF40195BP: 16-lead DIL; plastic (SOT-38Z).

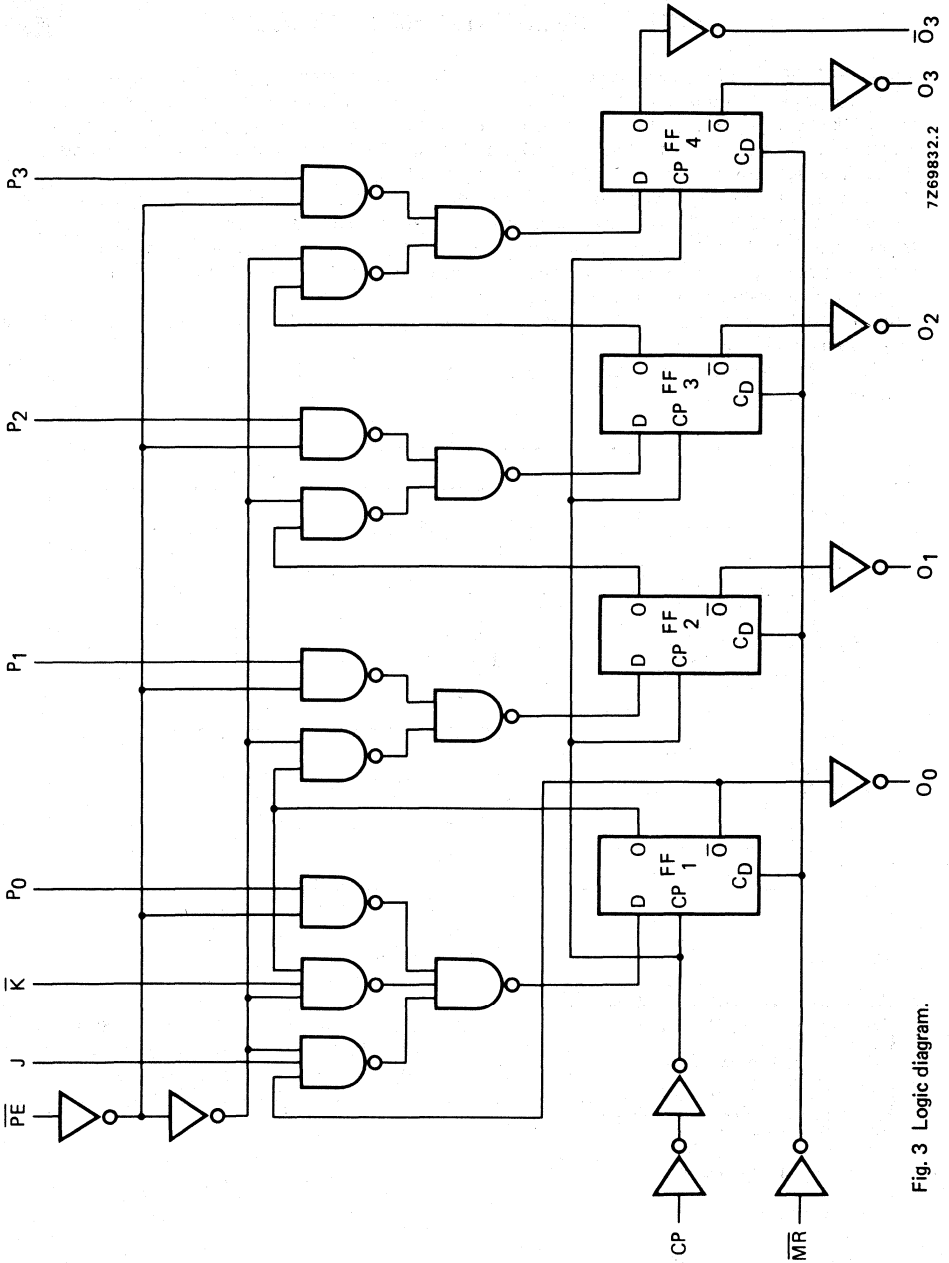
HEF40195BD: 16-lead DIL; ceramic (SOT-74).

HEF40195BT: 16-lead flat pack; plastic (SO-16; SOT-109A).

FAMILY DATA

IDD LIMITS category MSI

see Family Specifications



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Fig. 3 Logic diagram.

PINNING

\overline{PE}	parallel enable input (active LOW)
P_0 to P_3	parallel data inputs
J	first stage J-input (active HIGH)
\overline{K}	first stage K-input (active LOW)
CP	clock input (LOW to HIGH edge triggered)
\overline{MR}	master reset input (active LOW)
O_0 to O_3	buffered parallel outputs
\overline{O}_3	buffered inverted output from last stage

FUNCTION TABLE

operating mode	inputs ($\overline{MR} = \text{HIGH}$)							outputs at $t_n + 1$				
	\overline{PE}	J	\overline{K}	P_0	P_1	P_2	P_3	O_0	O_1	O_2	O_3	\overline{O}_3
shift mode	H	L	L	X	X	X	X	L	O_0	O_1	O_2	\overline{O}_2
	H	L	H	X	X	X	X	O_0	O_0	O_1	O_2	\overline{O}_2
	H	H	L	X	X	X	X	\overline{O}_0	O_0	O_1	O_2	\overline{O}_2
	H	H	H	X	X	X	X	H	O_0	O_1	O_2	\overline{O}_2
parallel entry mode	L	X	X	L	L	L	L	L	L	L	L	H
	L	X	X	H	H	H	H	H	H	H	H	L

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

X = state is immaterial

 $t_n + 1$ = state after next LOW to HIGH transition of CP

A.C. CHARACTERISTICS

 $V_{SS} = 0 \text{ V}$; $T_{amb} = 25 \text{ }^\circ\text{C}$; $C_L = 50 \text{ pF}$; input transition times $\leq 20 \text{ ns}$

	V_{DD} V	symbol	min.	typ.	max.	typical extrapolation formula	
Propagation delays							
CP \rightarrow O_n	5			105	215	ns	78 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t _{PHL}		50	95	ns	39 ns + (0,23 ns/pF) C_L
	15			35	65	ns	27 ns + (0,16 ns/pF) C_L
	5			90	180	ns	63 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t _{PLH}		45	85	ns	34 ns + (0,23 ns/pF) C_L
	15			30	60	ns	22 ns + (0,16 ns/pF) C_L
CP \rightarrow \bar{O}_3	5			125	255	ns	98 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t _{PHL}		50	100	ns	39 ns + (0,23 ns/pF) C_L
	15			35	70	ns	27 ns + (0,16 ns/pF) C_L
	5			120	240	ns	93 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t _{PLH}		50	105	ns	39 ns + (0,23 ns/pF) C_L
	15			35	75	ns	27 ns + (0,16 ns/pF) C_L
MR \rightarrow O_n	5			100	205	ns	73 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t _{PHL}		45	90	ns	34 ns + (0,23 ns/pF) C_L
	15			30	65	ns	22 ns + (0,16 ns/pF) C_L
	5			125	235	ns	98 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t _{PLH}		55	115	ns	44 ns + (0,23 ns/pF) C_L
	15			40	85	ns	32 ns + (0,16 ns/pF) C_L
Output transition times							
HIGH to LOW	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
	10	t _{THL}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t _{TLH}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V _{DD} V	symbol	min.	typ.	max.	
Set-up times J, \bar{K} → CP	5	t _{su}	70	35	ns	see also waveforms Figs 4 and 5
	10		20	10	ns	
	15		10	5	ns	
P _n → CP	5	t _{su}	85	40	ns	
	10		25	10	ns	
	15		10	5	ns	
$\bar{P}\bar{E}$ → CP	5	t _{su}	115	55	ns	
	10		45	20	ns	
	15		30	15	ns	
Hold times J, \bar{K} → CP	5	t _{hold}	15	-20	ns	
	10		5	-5	ns	
	15		0	-5	ns	
P _n → CP	5	t _{hold}	20	-25	ns	
	10		10	-5	ns	
	15		0	-5	ns	
$\bar{P}\bar{E}$ → CP	5	t _{hold}	10	-50	ns	
	10		5	-20	ns	
	15		5	-10	ns	
Minimum clock pulse width; LOW	5	t _{WCPL}	60	30	ns	
	10		25	10	ns	
	15		20	10	ns	
Minimum $\bar{M}\bar{R}$ pulse width; HIGH	5	t _{WMRL}	100	50	ns	
	10		40	20	ns	
	15		30	15	ns	
Recovery time for $\bar{M}\bar{R}$	5	t _{RMRL}	30	10	ns	
	10		15	5	ns	
	15		15	5	ns	
Maximum clock pulse frequency	5	f _{max}	5	10	MHz	
	10		14	28	MHz	
	15		19	39	MHz	

	V _{DD} V	typical formula for P (μW)	where f _i = input freq. (MHz) f _o = output freq. (MHz) C _L = load capacitance (pF) Σ(f _o C _L) = sum of outputs V _{DD} = supply voltage (V)
Dynamic power dissipation per package (P)	5	1900 f _i + Σ(f _o C _L) × V _{DD} ²	
	10	8300 f _i + Σ(f _o C _L) × V _{DD} ²	
	15	22 800 f _i + Σ(f _o C _L) × V _{DD} ²	

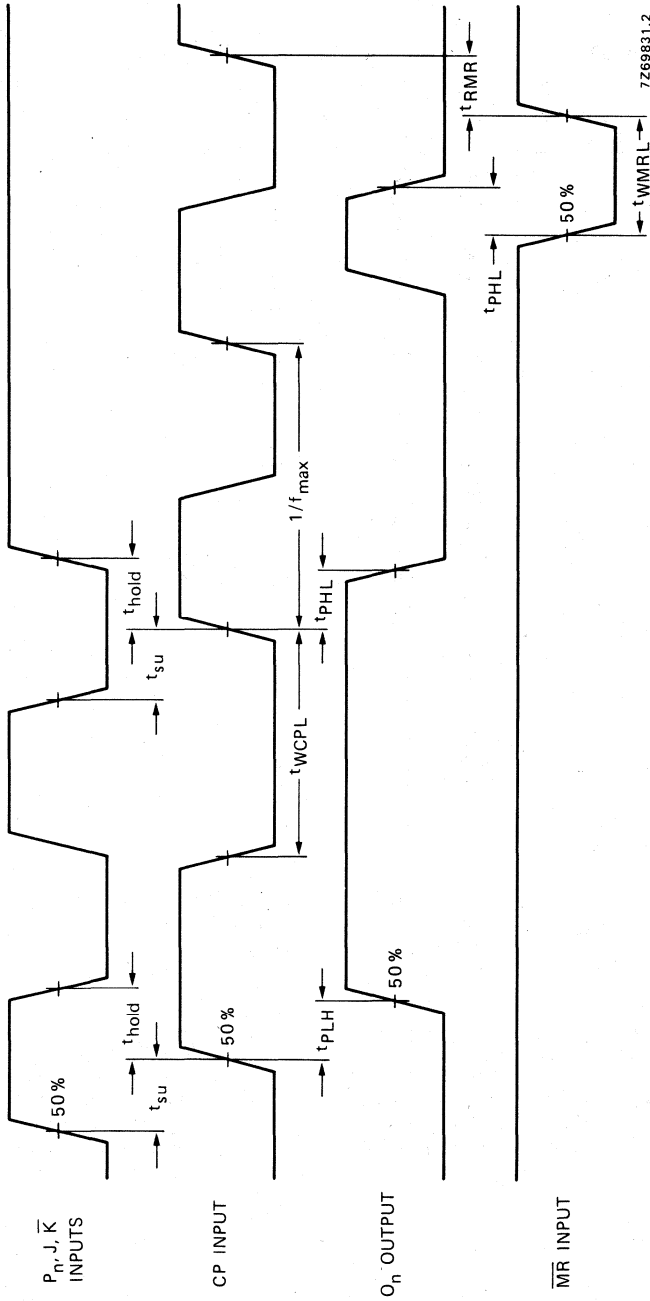


Fig. 4 Waveforms showing set-up times, hold times for J, \bar{K} and P_n inputs; minimum \overline{MR} pulse width, \overline{MR} to output delays and \overline{MR} to CP recovery time; minimum CP pulse width and CP to output delays. Set-up and hold times are shown as positive values but may be specified as negative values.

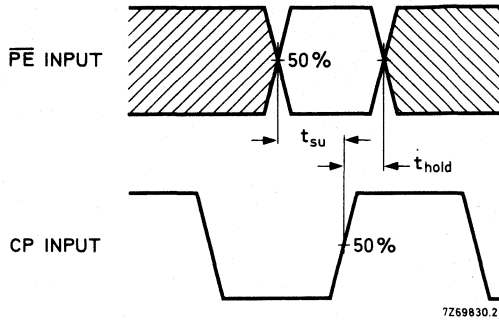


Fig. 5 Waveforms showing set-up and hold times for \overline{PE} input. Set-up and hold times are shown as positive values but may be specified as negative values.

APPLICATION INFORMATION

Some examples of applications for the HEF40195B are:

- Serial data transfer
- Parallel data transfer
- Serial to parallel data transfer
- Parallel to serial data transfer

DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

HEF40244B
MSI

OCTAL BUFFERS WITH 3-STATE OUTPUTS

The HEF40244B is an octal non-inverting buffer with 3-state outputs. It features output stages with high current output capability suitable for driving highly capacitive loads.

The 3-state outputs are controlled by the output enable inputs \overline{EO}_A and \overline{EO}_B . A HIGH on \overline{EO} causes the outputs to assume a high impedance OFF-state. The device also features hysteresis on all inputs to improve noise immunity.

The HEF40244B is pin and functionally compatible with the TTL '244' device.

Supply voltage range: 3 to 15 V.

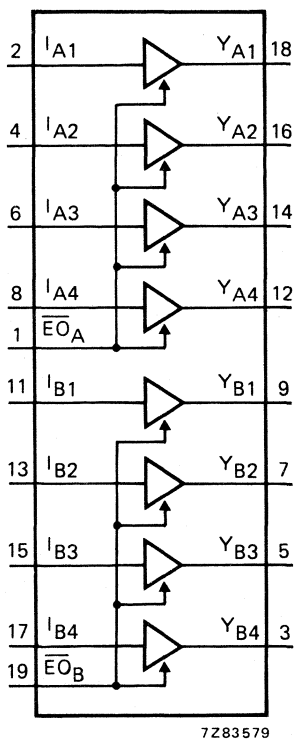


Fig. 1 Functional diagram.

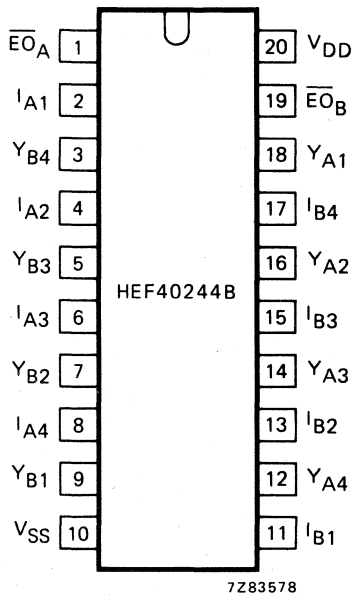


Fig. 2 Pinning diagram.

PINNING

- | | |
|------------------------------------|-------------------------------------|
| I_{A1} to I_{A4} | } inputs |
| I_{B1} to I_{B4} | |
| Y_{A1} to Y_{A4} | } bus outputs |
| Y_{B1} to Y_{B4} | |
| $\overline{EO}_A, \overline{EO}_B$ | } output enable inputs (active LOW) |

DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

HEF40245B

MSI

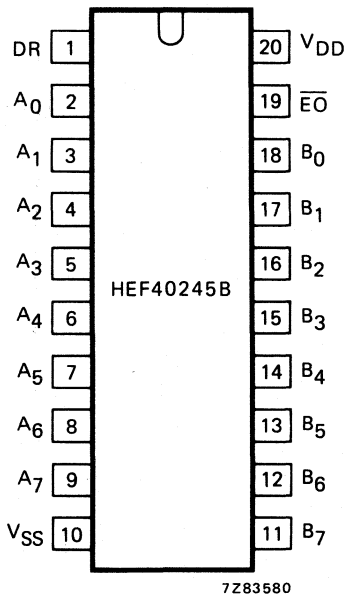
OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

The HEF40245B is an octal bus transmitter/receiver designed for 8-line asynchronous, 2-way data communication between data buses. It features output stages with high current output capability suitable for driving highly capacitive loads.

The direction input (DR) controls transmission of data from bus A to bus B, or bus B to bus A, depending on its logic level. The 3-state outputs are controlled by the enable input \overline{EO} . A HIGH on \overline{EO} causes the outputs to assume a high impedance OFF-state. The device also features hysteresis on all inputs to improve noise immunity.

The HEF40245B is pin and functionally compatible with the TTL '245' device.

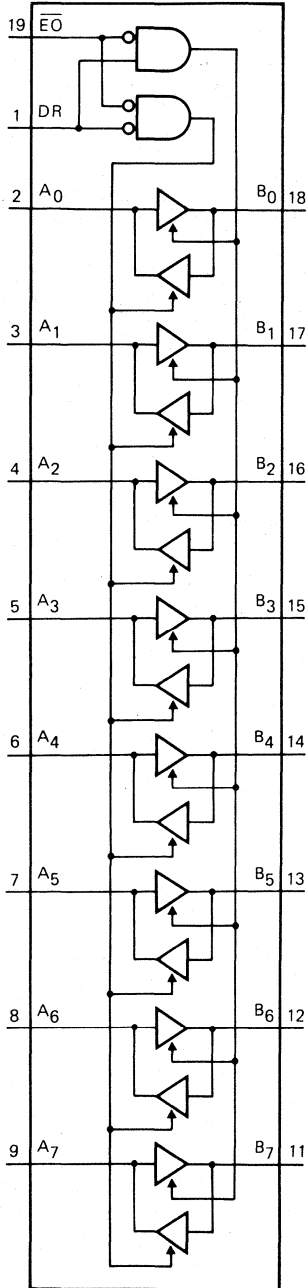
Supply voltage range: 3 to 15 V.



PINNING

A ₀ to A ₇	data input/output
B ₀ to B ₇	data input/output
DR	direction input
\overline{EO}	output enable input

Fig. 1 Pinning diagram.



FUNCTION TABLE

inputs		inputs/outputs	
\overline{EO}	DR	A_n	B_n
L	L	A = B	input
L	H	input	B = A
H	X	Z	Z

H = HIGH state (the more positive voltage)
 L = LOW state (the less positive voltage)
 X = state is immaterial
 Z = high impedance OFF-state

Fig. 2 Functional diagram.

7283581

DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

HEF40373B

MSI

OCTAL TRANSPARENT LATCH WITH 3-STATE OUTPUTS

The HEF40373B is an 8-bit transparent latch with 3-state buffered outputs. The output stages have high current output capability suitable for driving highly capacitive loads. The latch outputs follow the data inputs when the latch enable (E) is HIGH. When E is LOW, the data that meets the set-up times is latched. The 3-state outputs are controlled by the output enable input \overline{EO} . A HIGH on \overline{EO} causes the outputs to assume a high impedance OFF-state. The device features hysteresis on the E input.

The HEF40373B is pin and functionally compatible with the TTL '373' device.

Supply voltage range: 3 to 15 V.

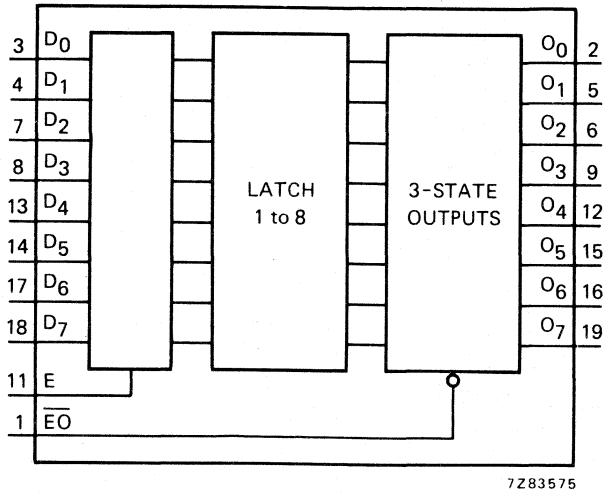


Fig. 1 Functional diagram.

PINNING

- | | |
|----------------------------------|----------------------------------|
| D ₀ to D ₇ | data inputs |
| E | latch enable input |
| \overline{EO} | output enable input (active LOW) |
| O ₀ to O ₇ | 3-state buffered outputs |

HEF40373B

MSI

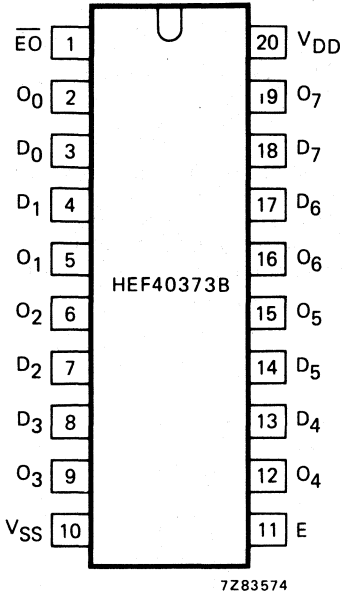


Fig. 2 Pinning diagram.

FUNCTION TABLE

operating modes	inputs			internal register	outputs O ₀ to O ₇
	\overline{EO}	E	D _n		
enable & read register	L	H	L	L	L
	L	H	H	H	H
latch & read register	L	L	l	L	L
	L	L	h	H	H
latch register & disable outputs	H	L	l	L	Z
	H	L	h	H	Z

H = HIGH state (the more positive voltage)

h = HIGH state (one set-up time prior to the HIGH-to-LOW enable transition)

L = LOW state (the less positive voltage)

l = LOW state (one set-up time prior to the HIGH-to-LOW enable transition)

Z = high impedance OFF-state

DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

HEF40374B

MSI

OCTAL D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

The HEF40374B is an octal D-type flip-flop with 3-state buffered outputs. The device is used primarily as an 8-bit positive edge-triggered storage register for interfacing with a 3-state bus. Data on the D-inputs is transferred to storage during the LOW-to-HIGH transition of the clock (CP) input. The 3-state output buffers are controlled by an active LOW output enable input (\overline{EO}). A HIGH on \overline{EO} forces the eight outputs to a high impedance OFF-state. When \overline{EO} is LOW, the data in the register appears at the outputs.

The output stages have high current output capability suitable for driving highly capacitive loads. The device features hysteresis on the CP input.

The HEF40374B is pin and functionally compatible with the TTL '374' device.

Supply voltage range: 3 to 15 V.

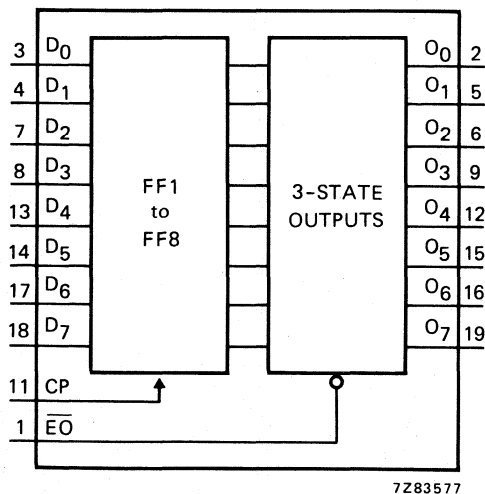


Fig. 1 Functional diagram.

PINNING

- D₀ to D₇ data inputs
- CP clock input
- \overline{EO} output enable input (active LOW)
- O₀ to O₇ 3-state buffered outputs

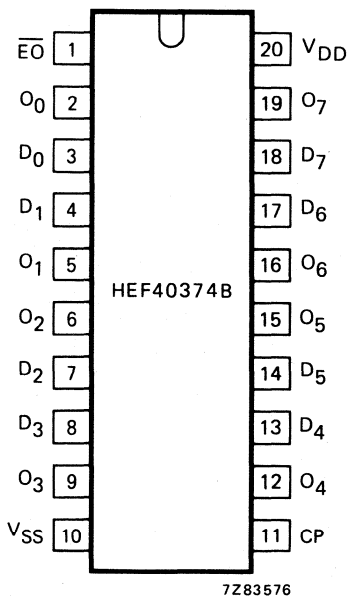


Fig. 2 Pinning diagram.

FUNCTION TABLE

operating modes	inputs			internal register	outputs O ₀ to O ₇
	\overline{EO}	CP	D _n		
load & read register	L	\nearrow	l	L	L
	L	\nearrow	h	H	H
load register & disable outputs	H	\nearrow	l	L	Z
	H	\nearrow	h	H	Z

H = HIGH state (the more positive voltage)

h = HIGH state (one set-up time prior to the LOW-to-HIGH clock transition)

L = LOW state (the less positive voltage)

l = LOW state (one set-up time prior to the LOW-to-HIGH clock transition)

Z = high impedance OFF-state

\nearrow = LOW-to-HIGH clock transition

DIGITAL INTEGRATED CIRCUITS — LOC MOS



FUNCTIONAL AND NUMERICAL INDEX



GENERAL




PACKAGE OUTLINES



FUNCTIONAL DIAGRAMS



PIN DESIGNATIONS



HE4000B FAMILY - INTRODUCTION



FAMILY SPECIFICATIONS



DEVICE DATA

Electronic components and materials for professional, industrial and consumer uses from the world-wide Philips Group of Companies

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- United States:** (Active devices & Materials) AMPEREX SALES CORP., Providence Pike, SLATERSVILLE, R.I. 02876, Tel. (401) 762-9000.
(Passive devices) MEPCO/ELECTRA INC., Columbia Rd., MORRISTOWN, N.J. 07960, Tel. (201) 539-2000.
(IC Products) SIGNETICS CORPORATION, 811 East Arques Avenue, SUNNYVALE, California 94086, Tel. (408) 739-7700.
- Uruguay:** LUZILECTRON S.A., Avda Rondeau 1576, piso 5, MONTEVIDEO, Tel. 91 43 21.
- Venezuela:** IND. VENEZOLANAS PHILIPS S.A., Elcoma Dept., A. Ppal de los Ruices, Edif. Centro Colgate, CARACAS, Tel. 36 05 11.